

## Getting Started with the AD-DAC-FMC-ADP Adapter Board

### INTRODUCTION

The ADC-DAC-FMC-ADP adapter board allows any of Analog Devices' DPG2-compatible High-Speed DAC Evaluation Boards to be used on a Xilinx® evaluation board with a FMC connector. The adapter board uses the Low Pin Count (LPC) version of the FMC connector, so it can be used on either LPC or HPC hosts (such as the ML605 or SP605).

A list of DPG2-compatible evaluation boards can be found at <http://www.analog.com/dpg>

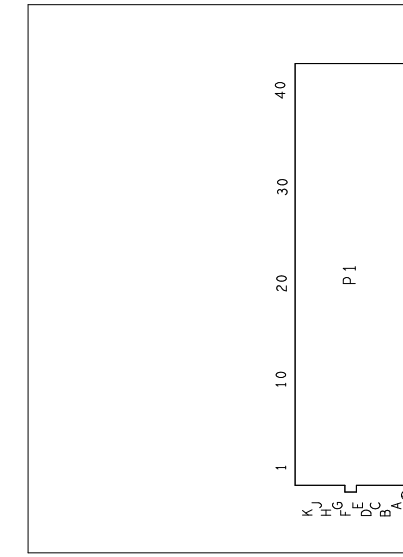
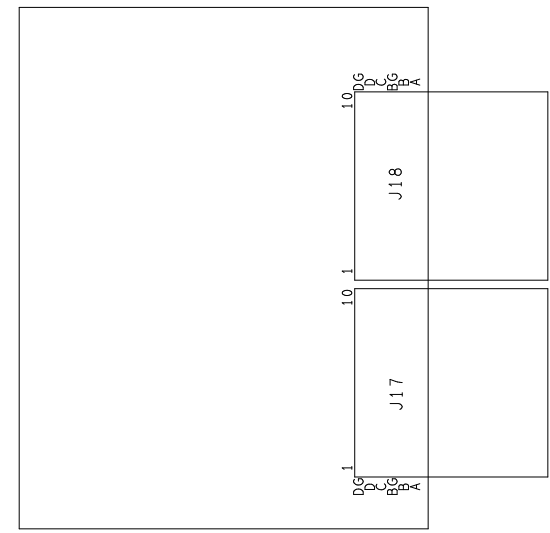
The schematic and layout are included in the following pages of this document. In addition, example UCF files for both the ML605 and SP605 are included as a starting point.

### CLOCKING

Every DPG2-compatible evaluation board provides two LVDS clocks to the host. These two clocks are always identical in both frequency and phase. On DACs using an LVDS interface, the host is then expected to output two LVDS clocks that are phase aligned to the data. It is very important that these clocks be generated the same way as the data, so that any delays inside the FPGA are matched. Therefore, this clock should be considered another data bit with a fixed "10101" pattern.




REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	16AUG10	J.C.



PRIMARY SIDE

SECONDARY SIDE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX ±.010 ±1/32 ±.2 .XXX ±.005 ±.2	ASSEMBLY		 HSC DIVISION 804 WOBURN STREET WILMINGTON, MA 01887
	APPROVAL	DATE	
MATERIAL	DRAWN BY W.D.B.	16AUG10	VITA57 TO DPGA ADAPTER BOARD (AD-DAC-FMC-ADP)
FINISH	DESIGNED		SIZE FSCM NO DRAWING NUMBER REV C HSC 10033 A
	CHECKED		
DO NOT SCALE DWG	APPROVED		SCALE 1/1 SHEET 1 OF 1
	MFG ENGINEER		

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	16AUG10	J.C.

NOTES:

MATERIALS; FR-4, IN ACCORDANCE WITH IPC-L-130 (LATEST REV.). GLASS FABRIC BASE, EPOXY RESIN, FIRE RESISTANT.

BONDING AGENT; PREIMPREGNATED B STAGE EPOXY GLASS CLOTH IN ACCORDANCE WITH IPC-L-109 (LATEST REV.).

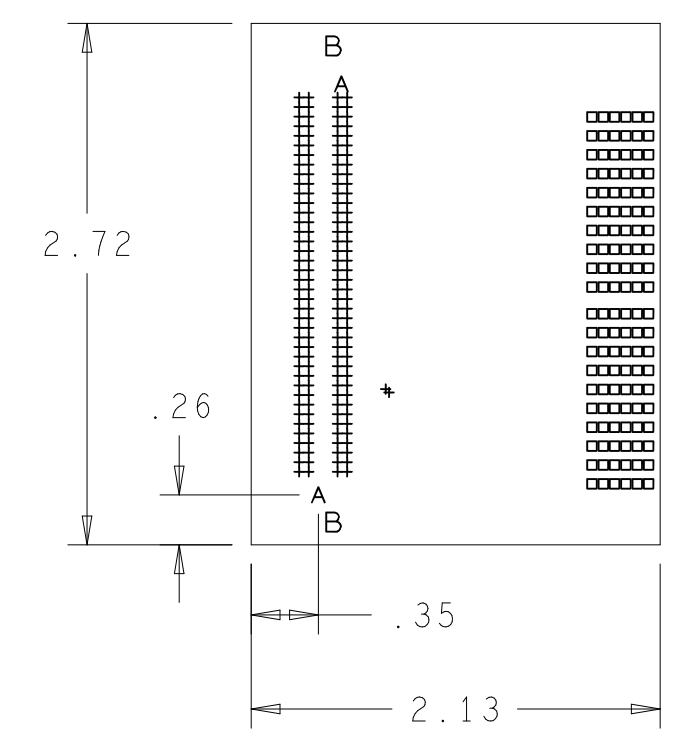
CLADDING; EXTERNAL LAYERS 1/4 OZ. COPPER, OVERPLATE TO 1 OZ. INTERNAL PLANE LAYERS 2 OZ. COPPER.

SOLDER MASK; SHALL BE BLUE LIQUID PHOTOIMAGABLE (LPI) APPLIED ON BOTH SIDES OVER BARE COPPER AND SHALL MEET IPC-SM-840 (LATEST REV.) CLASS 3.

SILK SCREEN; SHALL BE PERMANENT NON-CONDUCTIVE EPOXY INK, COLOR WHITE.

U.L. RATING; 94VO MINIMUM.

- FABRICATION:
- REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
  - UNDIMENSIONED HOLES TO BE LOCATED WITHIN +/- .005 OF THEIR TRUE POSITION WITH RESPECT TO ARTWORK.
  - PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN .001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
  - HOLE DIAMETERS APPLY AFTER PLATING.
  - FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL, INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
  - MINIMUM DESIGN LINE WIDTH IS .008 INCH.
  - MINIMUM DESIGN SPACING IS .005 INCH.
  - BOARD/PANEL MUST MEET IPC-A-600 (LATEST REV.) CLASS 2 FOR FLATNESS.
  - MFGR. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED;
    - A. U.L. CODE
    - B. DATE CODE (STAMP)
    - C. FLAMMABILITY RATING
    - D. MFGR. LOGO
    - E. SUCCESSFUL ELECTRICAL BOARD TEST.
  - NON-FUNCTIONAL PADS MAY BE REMOVED FROM INNER SIGNAL LAYERS AT MFGR. DISCRETION.
  - IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFGR. MAY TEAR DROP PADS TO MAINTAIN ANNULAR RING AT PAD TO CIRCUIT INTERFACE ONLY AND MUST INSURE ELECTRICAL INTEGRITY.
  - REPAIRS PER IPC-R-700 ARE ALLOWED.
  - MODIFICATIONS TO THE ARTWORK, OTHER THAN THOSE DESCRIBED ON THE FABRICATION DRAWING, ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
  - FINISH: SURFACES SHALL HAVE ENIG FINISH PLATED WITH 2-6 MICROINCHES OF IMMERSION GOLD OVER 100-200 MICROINCHES OF ELECTROLESS NICKEL.



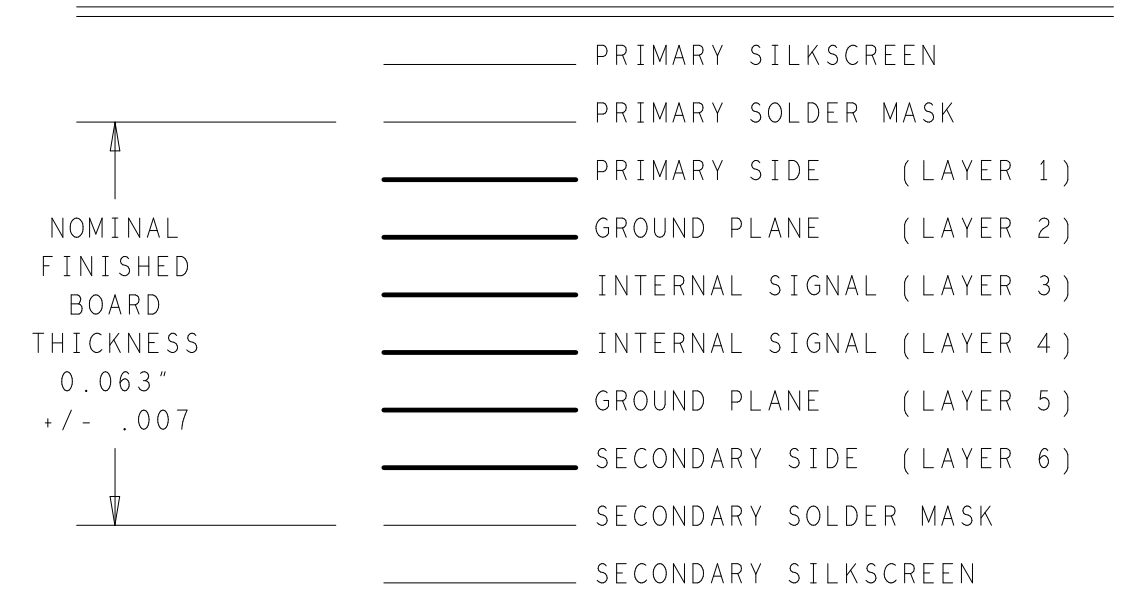
PRIMARY SIDE

HOLE TOLERANCE

UNLESS SPECIFIED  
 PLATED: +/- .003  
 NON PLATED: +/- .001

FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
+	10.0	PLATED	162	
□	24.0	PLATED	120	
A	50.0	NON-PLATED	2	
B	105.0	NON-PLATED	2	

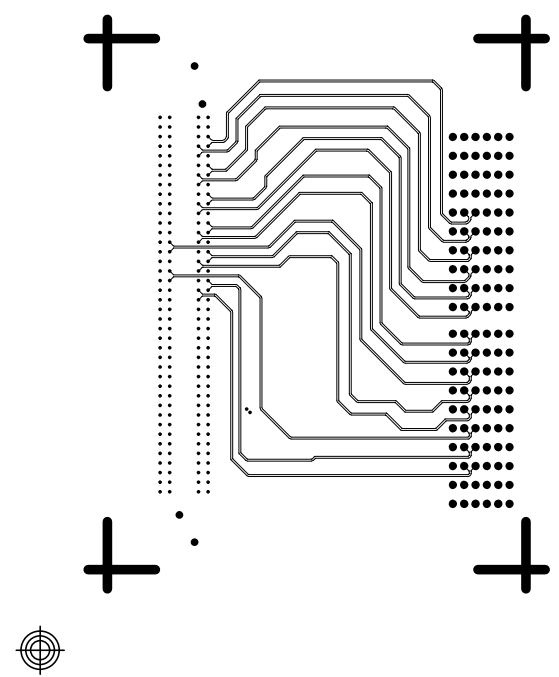
6 LAYER STACKUP



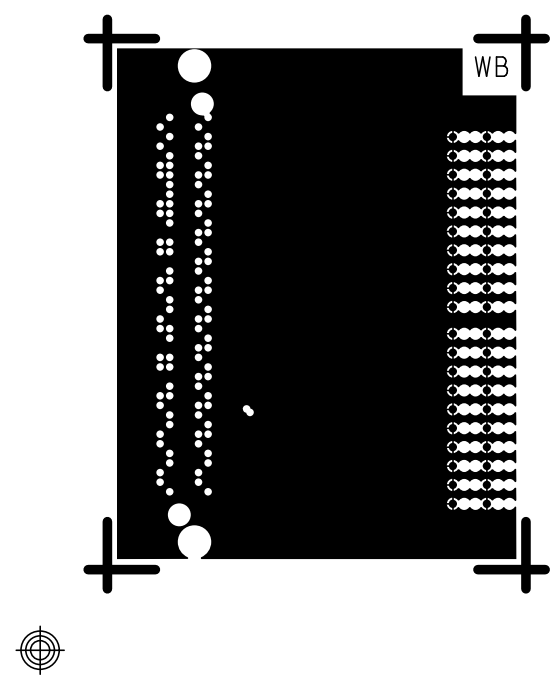
DIFFERENTIAL IMPEDANCE = 100 OHMS +/- 10%  
 ARTWORK LINE WIDTH FOR  
 IMPEDANCE CONTROLLED LINES = 0.005"

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XX +/- .010 +/- 1/32 +/- 2 .XXX +/- .005	NCDRILL				HSC DIVISION 804 WOBURN STREET WILMINGTON, MA 01887	
	APPROVAL	DATE	TITLE			
	DRAWN BY W.D.B.	16AUG10	VITA57 TO DPGA ADAPTER BOARD (AD-DAC-FMC-ADP)			
MATERIAL	DESIGNED	CHECKED	APPROVED	DATE	SIZE	FSCM NO
FINISH	MFG ENGINEER				C	
DO NOT SCALE DWG			SCALE	1/1	DRAWING NUMBER	REV
					HSC 10033	A
			SHEET 1 OF 1			

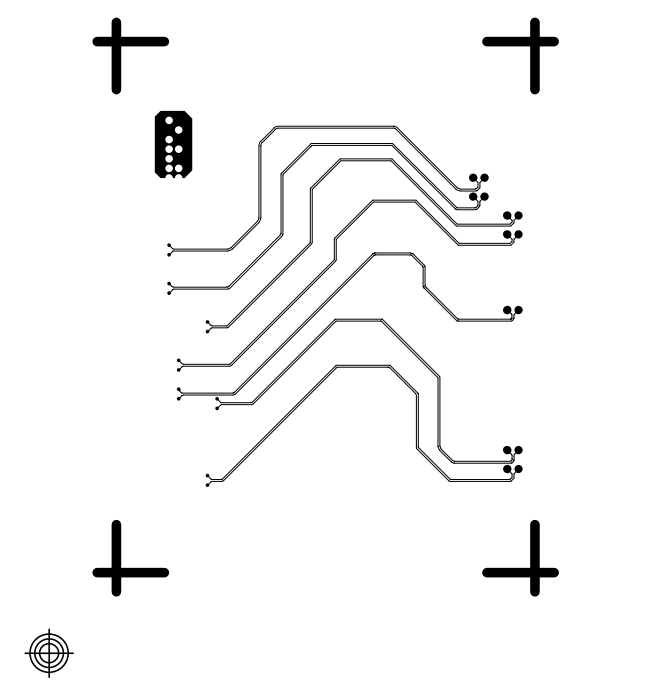
L1 PRIMARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



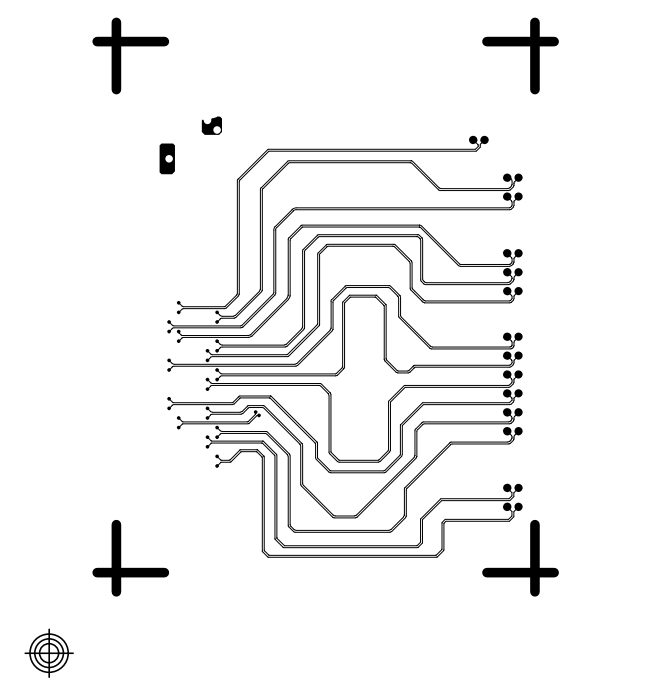
L2\_GROUND  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



L3\_SIGNAL  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A

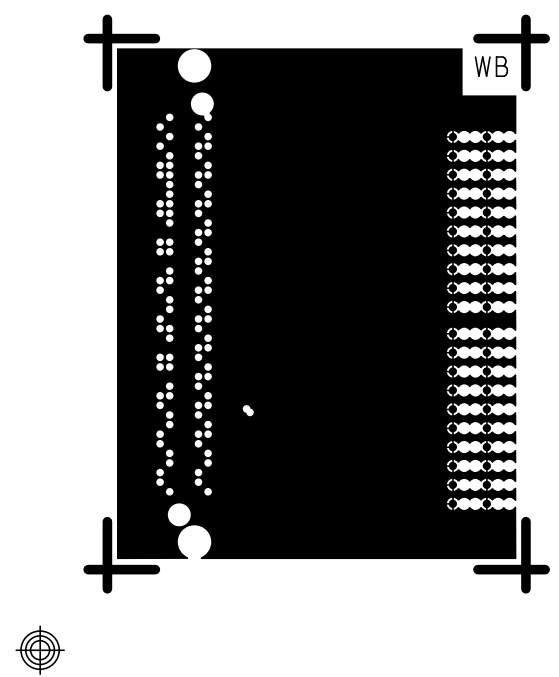


L4\_SIGNAL  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A

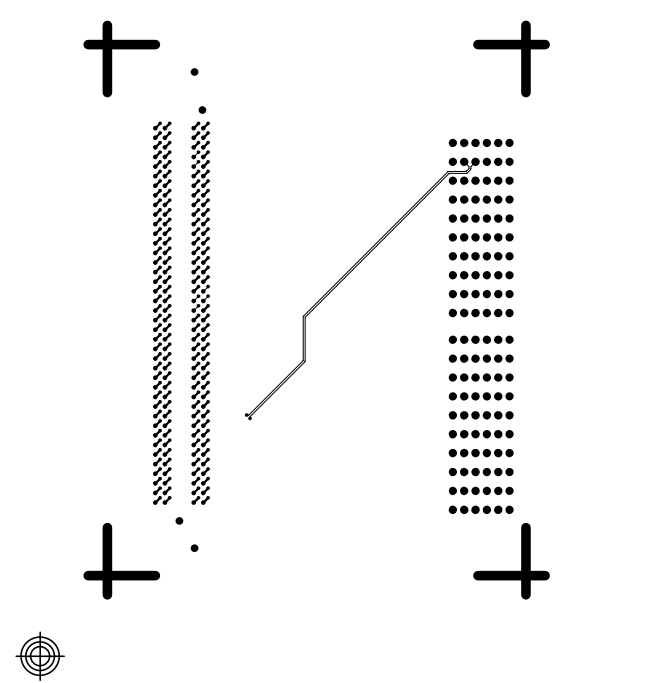




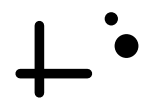
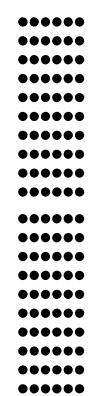
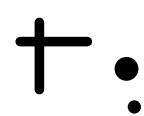
L5\_GROUND  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



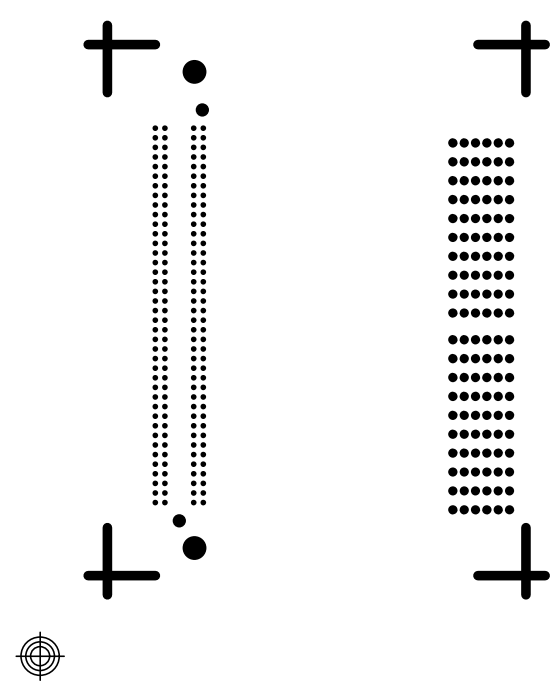
L6 SECONDARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



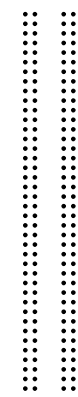
SOLDERMASK PRIMARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



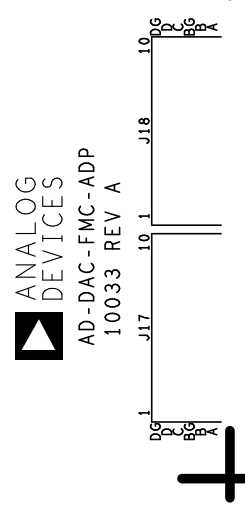
SOLDERMASK SECONDARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



PASTEMASK SECONDARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



SILKSCREEN PRIMARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A



SILKSCREEN SECONDARY  
VITA57-DPG2 ADAPTER BRD  
HSC 10033  
REV A

