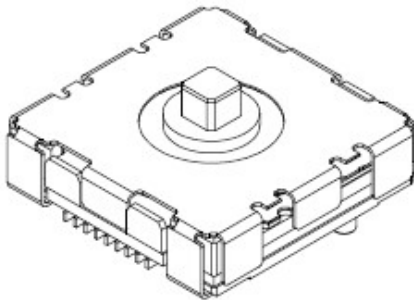


EasyPoint™ N40P112 Navigation Module

1 General Description

EasyPoint™ N40P112 is a miniature joystick module concept based on contact-less, magnetic movement detection. The integrated two-dimensional linear encoder monitors the movement of the magnet incorporated in the knob and provides directly the x and y coordinates via I²C output. An integrated mechanical push button built in the module provides a "select" function.

Figure 1. N40P112-xxxxx-H



2 Key Features

- XY coordinates direct read with 8-bit resolution
- 2.7V to 3.6V operating voltage
- Down to 1.7V I/O voltage
- Lateral magnet movement radius up to 1.0mm
- High-speed I²C interface
- Configurable interrupt output for motion detection
- Push button feature

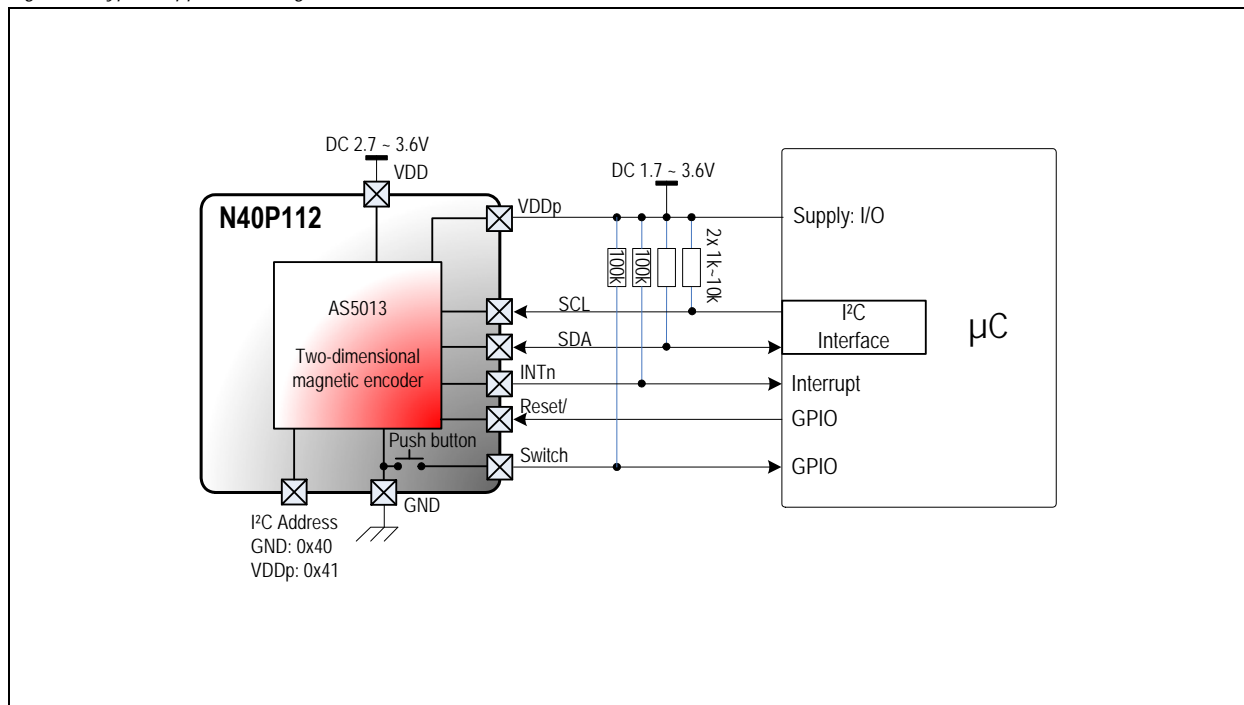
3 Applications

The EasyPoint™ N40P112 is ideal for small form-factor manual input devices in battery operated equipment, such as Mobile phones, MP3 players, PDAs, GPS receivers, Gaming consoles and Analog joystick replacement.

4 Benefits

- High reliability due to magnetic non-contact sensing
- Low power consumption
- Two operating modes
 - Idle mode
 - Low Power mode

Figure 2. Typical Application Diagram



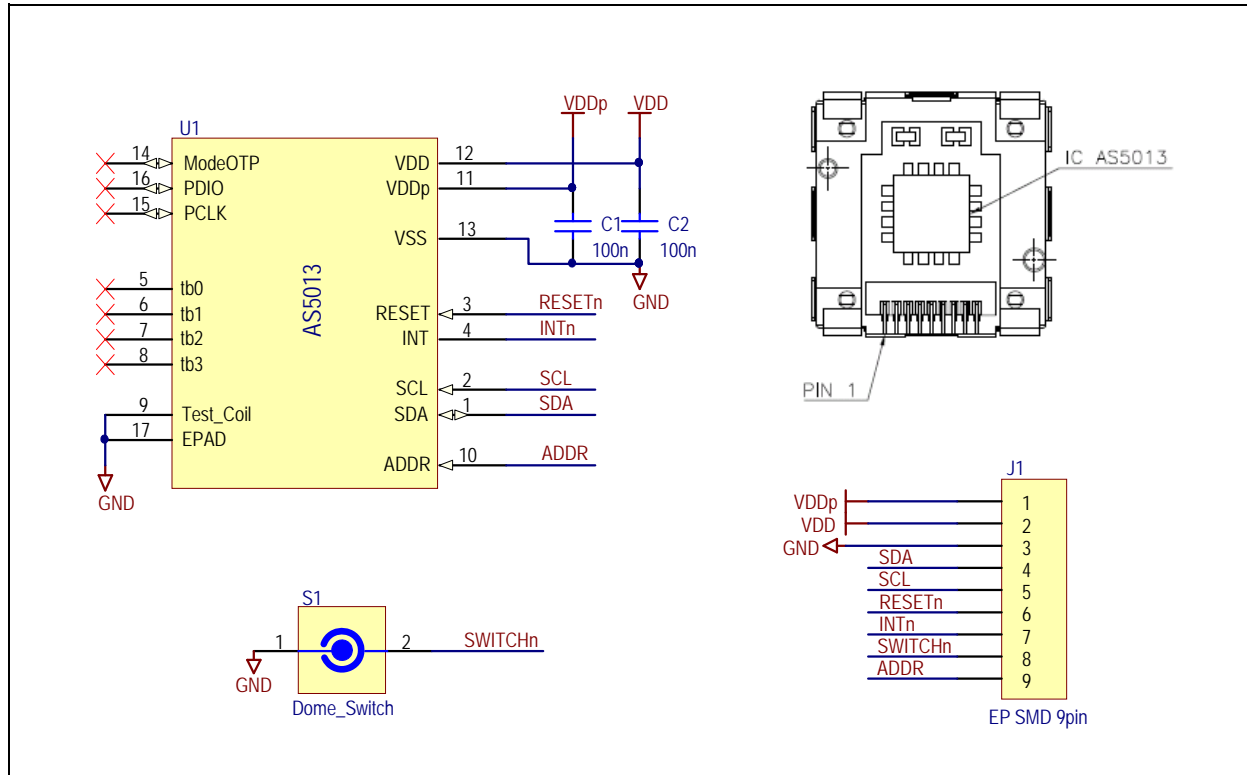
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5 Pin Assignments

Figure 3. N40P112-xxxxx-H Schematics



5.1 Pin Descriptions

Table 1. Pin Descriptions

| Connector Pin # | Pin Type | Description |
|-----------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 1 | Power | VDDp : IO power supply for SCL, SDA, INTn, 1.7V ~ 3.6V |
| 2 | Power | VDD : Core power supply, 2.7V ~ 3.6V |
| 3 | Power | GND |
| 4 | Bi-directional | SDA : I ² C bus data, open drain |
| 5 | Input | SCL : I ² C bus clock |
| 6 | Input | RESEIn : Reset input, active LOW 0: GND → Reset, all registers return to their reset value 1: VDDp → Normal operation mode |
| 7 | Open drain | INTn : Interrupt output, open drain: Active: LOW Inactive: Hi-Z |
| 8 | Output | SWITChn : Push button signal output: Not pushed: Open Pushed: GND |
| 9 | Input | ADDR : I ² C Address selection input: 0: GND → 0x40 1: VDDp → 0x41 |

6 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 6](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Notes |
|-------------------|----------------------------------|------|---------------------------------------|-------|---------------------------------------|
| V _{DD} | DC supply voltage | -0.3 | 5 | V | |
| V _{DDp} | Peripheral supply voltage | -0.3 | ⁵ V _{DD} + 0.3 | V | SCL, SDA, RESETn, ADDR |
| V _{IN} | Input pin voltage | -0.3 | V _{DDp} + 0.3 | V | SCL, SDA, RESETn, ADDR |
| | | - | 3.6 | | |
| I _{SCR} | Input current (latchup immunity) | -100 | 100 | mA | Norm: JEDEC 78 |
| ESD | Electrostatic discharge | - | ±2 | kV | All pins, Norm: MIL 883 E method 3015 |
| T _{Strg} | Storage temperature | -40 | 85 | °C | |
| | Humidity non-condensing | 5 | 85 | % | |
| | Degrees of protection | IP5X | | | Norm: IEC 60529 |

7 Electrical Characteristics

7.1 Operating Conditions

$T_{AMB} = -20$ to $+70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V}$

Table 3. Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|-------------------|-----------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| VDD | Core Supply voltage | 2.7 | | 3.6 | V | |
| VDDp | Peripheral Supply voltage | 1.7 | | VDD | V | Input: RESETn Open drain outputs: SCL, SDA, INTn. External I ² C pull up resistor to be connected to VDDp. |
| IDD _S | Maximal average current consumption on VDD, Pulsed peaks = IDD _f depends on the sampling time ts[ms] | 3+3760/ts [ms] | | | μA | TAMB = -20 to +50 °C |
| | | 10+3760/ts [ms] | | | | TAMB = 50 to +70 °C |
| IDD _I | Current consumption on core supply, Idle mode, no readout (ts = infinite) | | | 3 | μA | TAMB = -20 to +50 °C |
| | | | | 10 | | TAMB = 50 to +70 °C |
| IDD _f | Current consumption on core supply, Full Power mode | | | 10 | mA | Continuous current pin VDD Maximum sampling ts = 450μs |
| T _{pu} | Power up time analog | | | 1000 | μs | Step on VDD to Data_Ready |
| T _{conv} | Conversion time | | | 450 | μs | Read X/Y coordinate I ² C STOP condition to Data_Ready |
| t _{p,w} | Nominal wakeup time | 20 | | 320 | ms | |
| T _{AMB} | Ambient temperature range | -20 | | +70 | °C | |
| | Resolution of XY displacement | | 8 | | | Over 2*dx and 2*dy axis |

7.2 Digital IO Pads DC/AC Characteristics

Table 4. Digital IO Pads DC/AC Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
|---------------------------------------|---------------------------|-------------|-------------|-------|-----------------------------------------------|
| Inputs: SCL, SDA | | | | | |
| V _{IH} | High level input voltage | 0.7 * VDDp | | V | I ² C |
| V _{IL} | Low level input voltage | | 0.3 * VDDp | V | I ² C |
| I _{LEAK} | Input leakage current | | 1 | μA | VDDp = 3.6V |
| Inputs: ADDR, RESETn (JEDEC76) | | | | | |
| V _{IH} | High level input voltage | 0.65 * VDDp | | V | JEDEC |
| V _{IL} | Low level input voltage | | 0.35 * VDDp | V | JEDEC |
| I _{LEAK} | Input leakage current | | 1 | μA | VDDp = 3.6V |
| Outputs: SDA | | | | | |
| V _{OH} | High level output voltage | Open drain | | | Leakage current 1μA High level output voltage |

Table 4. Digital IO Pads DC/AC Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
|--------------------------------|---------------------------|------------|------------|-------|----------------------------------------------|
| V _{OL1} | Low level output voltage | | VSS + 0.4 | V | -6mA; VDDp > 2V; fast mode |
| V _{OL3} | | | VDDp * 0.2 | V | -6mA; VDDp ≤ 2V; fast mode |
| V _{OL1} | | | VSS + 0.4 | V | -3mA; VDDp > 2V; high speed |
| V _{OL3} | | | VDDp * 0.2 | V | -3mA; VDDp ≤ 2V; high speed |
| CL | Capacitive load | | 400 | pF | standard mode (100 kHz) |
| | | | 400 | pF | fast mode (400 kHz) |
| | | | 100 | pF | high speed mode (3.4 MHz) |
| Outputs: INTn (JEDEC76) | | | | | |
| V _{OH} | High level output voltage | Open drain | | 1μA | Leakage current High level output voltage |
| V _{OL} | Low level output voltage | | VSS + 0.2 | V | -100μA |
| | | | VSS + 0.45 | | -2mA |
| CL | Capacitive load | | 30 | pF | standard mode (100 kHz) |

7.3 Switch Characteristics

Table 5. Switch Characteristics

| Parameter | Min | Max | Units | Notes |
|-----------------------------------|-----|-----|-------|--------------------------|
| Contact resistance of dome switch | | 500 | mΩ | Norm: EIA-364-23 |
| Dielectric withstanding voltage | 100 | | Vac | Norm: EIA-364-20 |
| Insulation resistance | 100 | | mΩ | Norm: EIA-364-21, 100Vdc |
| Bouncing (On/Off) | | 5 | ms | Rate: 2 times/sec. |

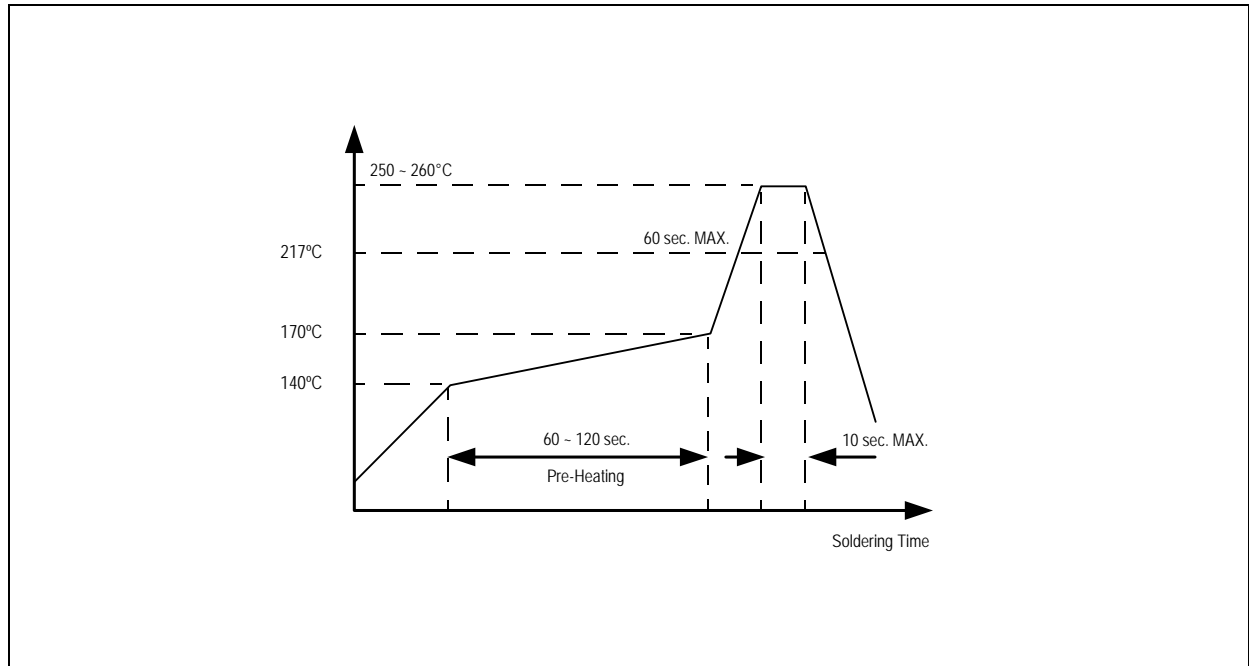
7.4 Mechanical Specifications

Table 6. Mechanical Specifications

| Parameter | Note |
|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Number of operating shafts | Single shaft |
| Shaft material | LCP |
| Housing material | LCP & PA46 |
| Shell material | Stainless Steel or Copper alloy |
| Travel (XY operation) | ±1.00mm (±10%) |
| Travel (Z push operation) | 0.22mm (±0.05mm) |
| Directional operating force (XY direction) | N40P112-000X1-H: 0.35N (±0.10N) N40P112-000X2-H: 0.55N (±0.15N) |
| Push operating force (Z direction) | 1.80N (±15%) |
| Vibration | 10-500-10Hz 15 minutes, 12 cycles, 3 axes (total 36 cycles) |
| Operating life – XY direction | Each direction > 1 million cycles |
| Operating life – Push Z direction | > 1 million cycles |
| Shaft strength (XYZ direction) | > 5.0 kgf |
| Free fall | Dispensing Glue 40 drops (2X6 sides + 1X12 edges + 2X8 corners) @ 1.5m drop height to concrete surface, module is assembled to phone mechanics. |
| Over force | Dispensing Glue 1.5kgf, > 100k cycles |

7.5 Recommended Reflow Temperature Profile

Figure 4. Reflow Temperature Profile



8 Using the N40P112 Module

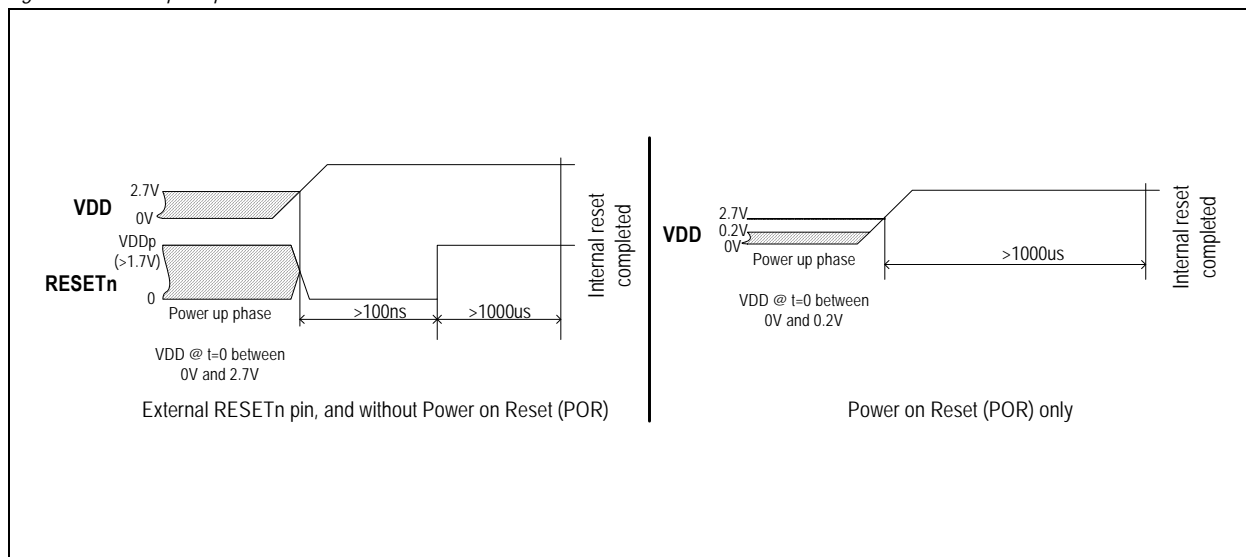
8.1 Powering up the Module

The N40P112 module has a Power ON Reset (POR) cell to monitor the VDD voltage at startup and reset all the internal registers. After the internal reset is completed, the POR cell is disabled in order to save current during normal operation.

If VDD drops below 2.7V down to 0.2V, the POR cell will not be enabled back, and the registers will not be correctly reseted or can get random values.

Note: It is highly recommended to control the external RESETn signal by applying a LOW pulse of >100ns once VDD has reached 2.7V and VDDp reached 1.7V.

Figure 5. Power-up Sequence



8.2 Registers Initialization

After Power Up, the following sequence must be performed:

1. VDD and VDDp Power up, and reached their nominal values (VDD>2.7V, VDDp>1.7V).
2. **Initialization:**
 - a. RESETn pulse LOW during >100ns, then RESETn HIGH
 - b. Loop check register [0Fh] until the value F0h or F1h is present (reset finished, registers to default values)
 - c. Write value 0Dh into register [2Dh] → Configure T_ctrl scaling factor for 1.0mm knob displacement
3. Perform an **Offset Calibration** (X and Y coordinate compensation for zero position)
4. Configure the **Dead Zone Area** for Wake-up function (if needed)
5. Configure the wanted Power Mode and INT function into register [0Fh] (Idle mode / Low Power Mode with Timebase configuration, INT for Wake-up or Coordinates ready)
6. X Y coordinates are ready to be read.

8.3 C Source Code Example

8.3.1 Initialization

```
void EasyPoint_init (void)
{
    unsigned char Reset_status = 0;

    RESETEn = 0; Delay_ms(1); // RESETEn pulse after power up
    RESETEn = 1; Delay_ms(1);

    while (Reset_status != 0xF0) // Check the reset has been done
    {
        Reset_status = I2C_Read8(0x40, 0x0F) & 0xFE;
    }

    I2C_Write8(0x40, 0x2d, 0x0D); // Scaling factor for N40 (1.0mm knob travel)
}
```

8.3.2 Offset Calibration

```
void Offset_Calibrate (void)
{
    char i;
    int x_cal=0, y_cal=0;

    EA = 0; // Disable the MCU interrupts

    I2C_Write8(0x40, 0x0F, 0x00); // Low Power Mode 20ms

    Delay_ms(1);

    I2C_Read8(0x40, 0x11); // Flush an unused Y_reg to reset the interrupt

    for (i=0; i<16; i++) // Read 16 times the coordinates and then average
    {
        while (INTn); // Wait until next interrupt (new coordinates)
        x_cal += (signed char) I2C_Read8(0x40, 0x10); // Read X position
        y_cal += (signed char) I2C_Read8(0x40, 0x11); // Read Y position
    }

    // offset_X and offset_Y are global variables, used for each coordinate readout
    // in the interrupt routine
    offset_X = -(x_cal>>4); // Average X: divide by 16
    offset_Y = -(y_cal>>4); // Average Y: divide by 16

    EA = 1; // Enable the MCU interrupts
}
```

8.3.3 Dead Zone area

The dead zone area is set around the zero position of the module. The zero position is known after the offset calibration. The dead zone area is a square with a width of $2 \cdot \text{center_threshold}$, around the calibrated zero position.

```
void Interrupt_Calibrate (center_threshold)
{
    EA = 0; // Disable the MCU interrupts
    I2C_Write8(0x40, 0x12, center_threshold - offset_X ); // Xp register
    I2C_Write8(0x40, 0x13, -center_threshold - offset_X); // Xn register
    I2C_Write8(0x40, 0x14, center_threshold - offset_Y); // Yp register
    I2C_Write8(0x40, 0x15, -center_threshold - offset_Y); // Yn register
    EA = 1; // Enable the MCU interrupts
}
```

8.3.4 Interrupt Routine

```
void EasyPoint_interrupt (void) interrupt 0
{
    int X_temp, Y_temp;

    EA=0;// Disable MCU interrupts

    /* OPTIONAL: If the module is in a slow power mode (e.g. Wakeup mode
    INT_function=1 with 320ms rate), configure to a higher rate with INTn for new
    coordinates ready (e.g. INT_function = 0 with 20ms rate) */

    x_reg = I2C_Read8(0x40, 0x10); // Read X position
    y_reg = I2C_Read8(0x40, 0x11); // Read Y position with interrupt reset

    // Add the X and Y offset for correct recentering
    X_temp = x_reg + offset_X;
    Y_temp = y_reg + offset_Y;

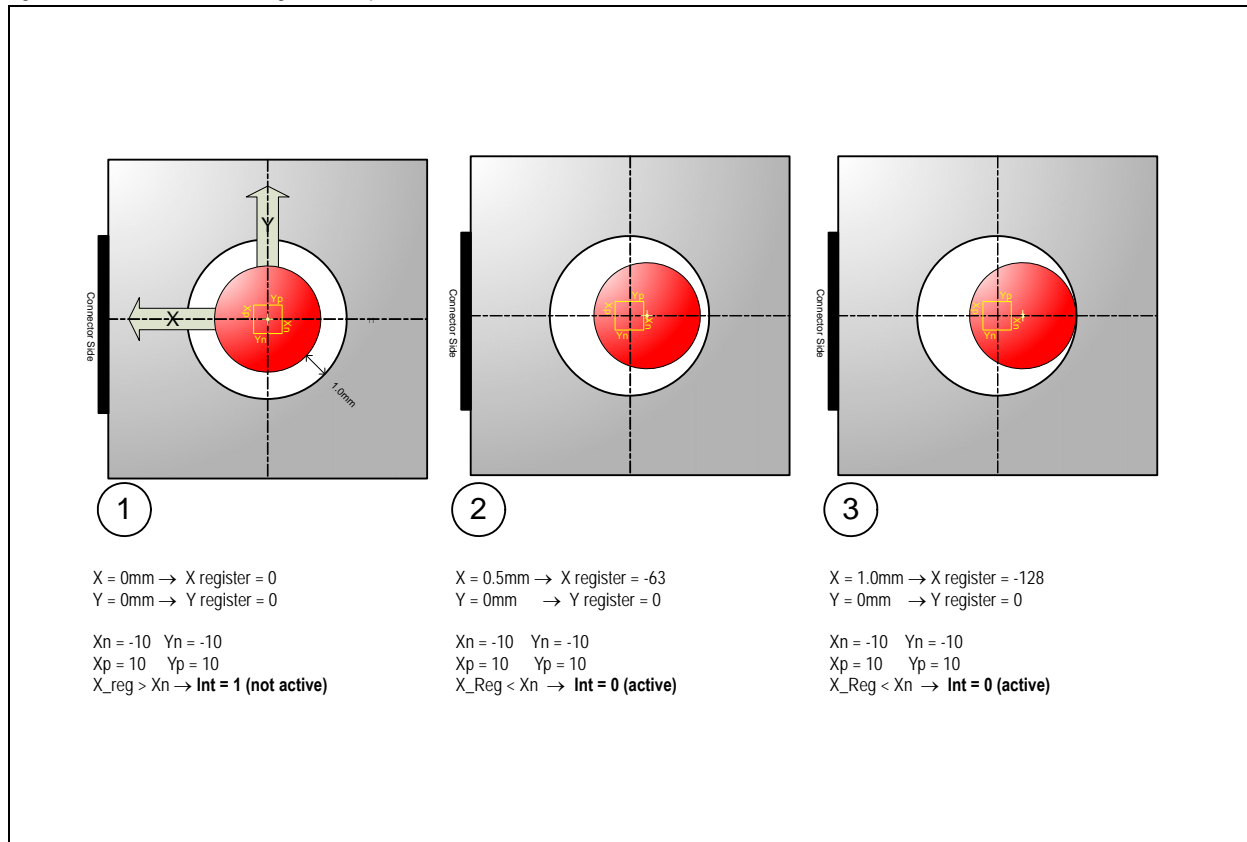
    /* OPTIONAL: If X_temp and Y_temp are near the center since a few interrupts,
    meaning the knob has been released, the module can be put back in a slow power
    mode (e.g. Wakeup mode INT_function=1 with 320ms rate) */

    EA = 1; // Enable the MCU interrupts
}
```

9 XY Coordinates Interpretation

9.1 EasyPoint Operating Principle

Figure 6. Mechanical to XY Register Interpretation



In the following example, the interrupt threshold values X_p , X_n , Y_p , Y_n (see I²C Registers on page 23) have been set by the user to $X_p=10$, $X_n = -10$, $Y_p = 10$, $Y_n = -10$. The four registers are programmable independently for the four directions.

When $INT_function$ (Reg 0Fh [2]) = 1, if the knob's coordinates remains in the area delimited by X_p X_n Y_p Y_n , INT_n interrupt output remains high (not active). Once the knob moves over this limit, INT_n goes LOW (active). For example, this feature can wake up a microcontroller from sleep mode.

Note: Due to the mechanical tolerance, the coordinates read on X and Y_res_int output registers can show a small offset on both directions. To avoid this offset, a calibration function should be implemented in the microcontroller, for example at power up of the system. The values X and Y_res_int represented in this datasheet are compensated values.

For further information, please see chapters 8.2 and 8.3 or refer to the austriamicrosystems N40P112 encoder application notes: <http://www.austriamicrosystems.com/eng/Products/Magnetic-Encoders/EasyPoint-Joystick-Encoder/AS5013>

Knob on Position 1.

The knob is released and on its initial position (0,0). The EasyPoint module is configured with $INT_function$ (Reg 0Fh [2]) = 1. X_reg and Y_reg register values are (0,0), and the interrupt is not active.

Knob on Position 2.

The center of the magnet has been moved upon the horizontal wakeup threshold X_p . The EasyPoint module sets INTn LOW (active). At this point, the microcontroller can configure the module with INT_function (Reg 0Fh [2]) = 0 and change the Low Power timebase Reg 0Fh [6:4] for a faster reaction time. In this interrupt mode, the interrupt output goes LOW (active) each time a new X and Y value is ready to be read by the microcontroller. The interrupt is reset HIGH (not active) once the register Y_res_int has been read (see I²C Registers on page 23).

Knob on Position 3.

The magnet has been moved to the maximum distance from the center (+1.0mm). The maximum X value is -128 decimal.

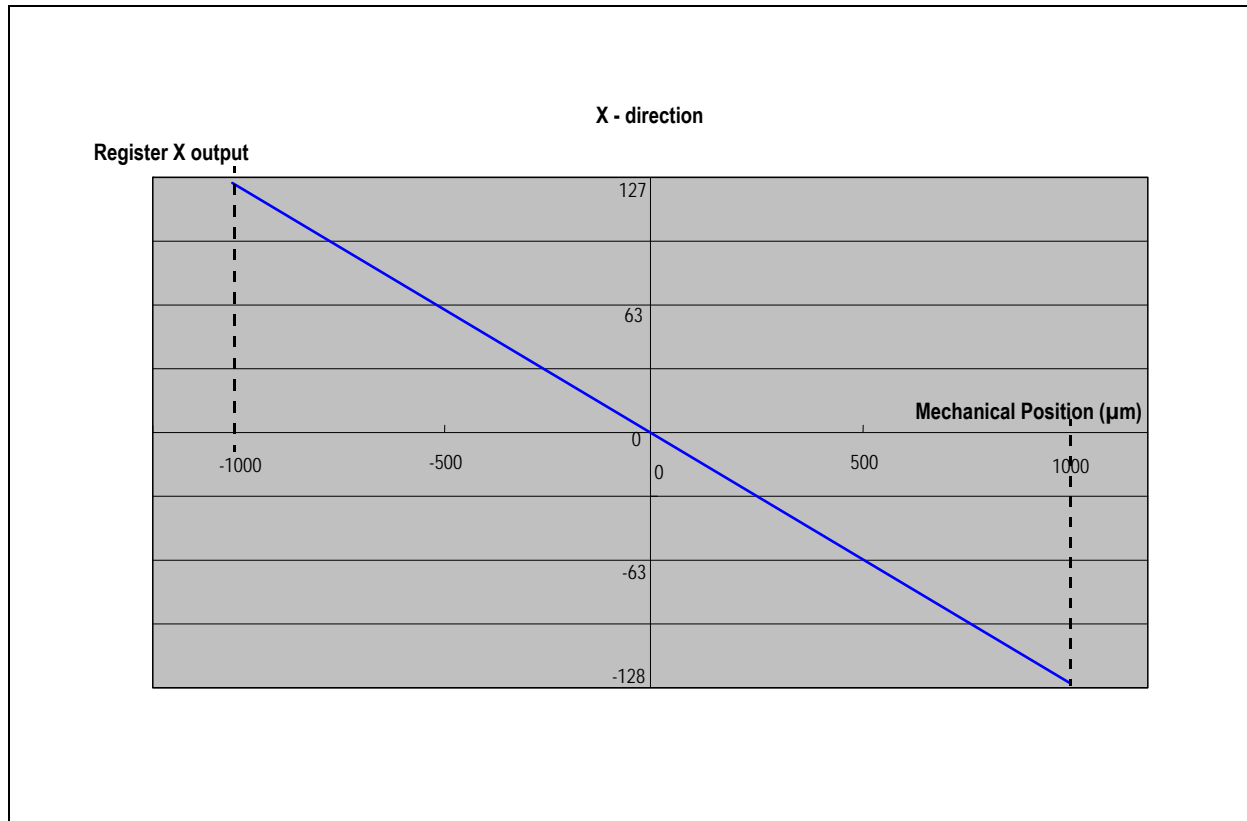
9.1.1 Knob Displacement and Register Value Relation

Figure 7 shows the relation between the X register value and the physical X coordinate of the central knob (± 1.0 mm horizontal displacement, 0.0mm is the center of the module, when the knob is released).

The Y axis measurements are the same as the X axis ones. Positive X register values are the left side knob movements, positive Y register values are the upper side knob movements.

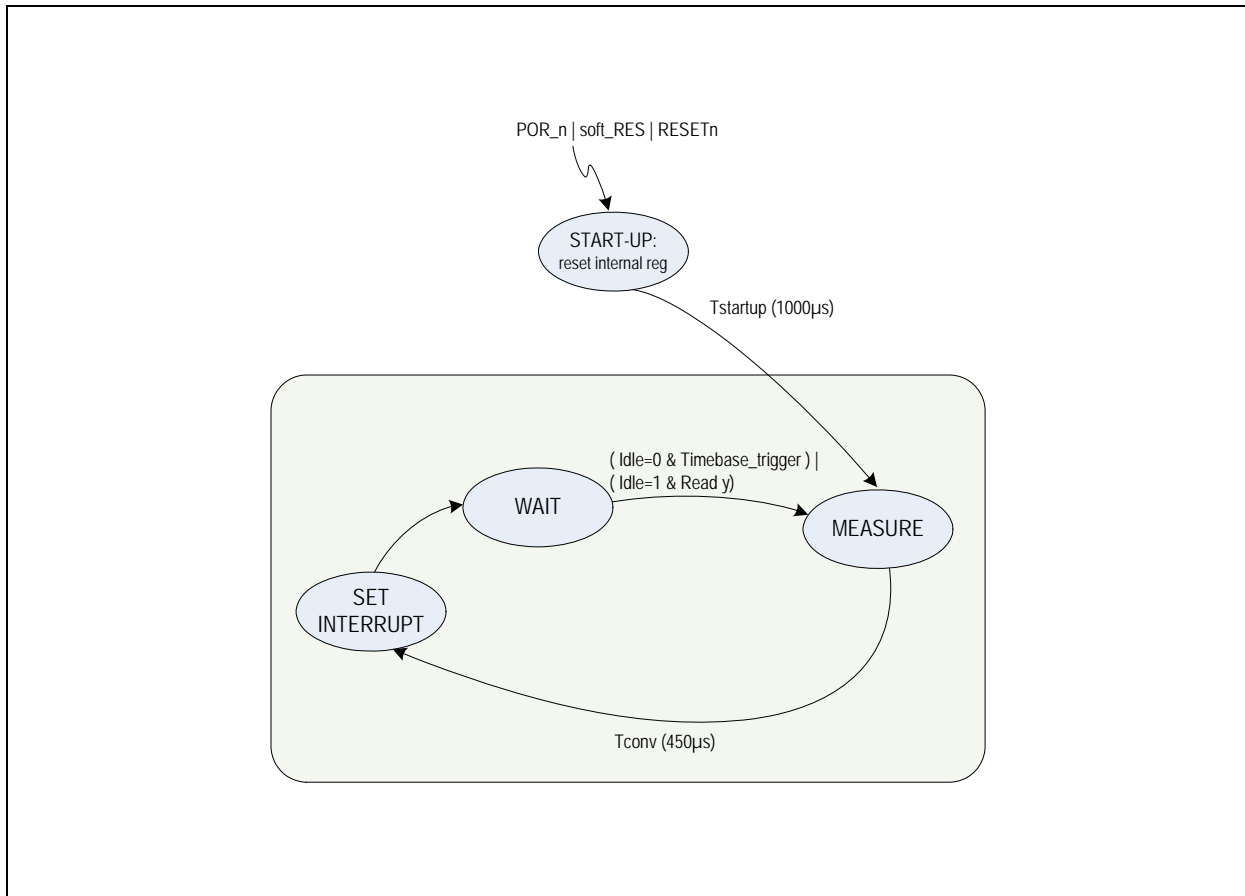
Those values are in an ideal condition, where the knob takes place over the center position of the N40P112 sensor once released. The zero position may vary between two N40 modules, and an offset must be applied to X and Y in order to compensate the X,Y coordinates to 0,0 once the knob is released. More information can be found in chapters 8.2 and 8.3.

Figure 7. X Register / X Displacement ($Y=0\mu\text{m}$)



9.2 Operation Principle

Figure 8. Operation Principle



START-UP:

After power up and after applying a soft reset (Reg 0Fh [1]) or hardware reset (RESETn input, LOW pulse >100ns), N40P112 enters the START-UP state. During this state the internal registers are loaded with their reset values. Then the N40P112 will perform one measurement and switches automatically into the WAIT state.

MEASURE:

The hall element data are measured, x/y coordinates are calculated and available in registers 10h and 11h after $T_{conv} = 450\mu\text{s}$ max.

SET INTERRUPT:

The INTn output is set, depending on the interrupt mode configured in the control register Reg 0Fh [2] and Reg 0Fh [3]

WAIT:

The module is now in waiting status. A new measurement will occur depending on the power mode (Reg 0Fh [7] Idle = 0 or 1) and the Timebase Reg 0Fh [6:4]

10 I²C interface

The N40P112 supports the 2-wire high-speed I²C protocol in device mode, according to the NXP specification UM10204.

The host MCU (master) has to initiate the data transfers. The 7-bit device address of the N40P112 depends on the state at the pin ADDR.

ADDR = 0 → Slave address = '1000 000' (40h)

ADDR = 1 → Slave address = '1000 001' (41h)

For other I²C addresses, please contact *austriamicrosystems*.

Supported modes (slave mode):

- Random/Sequential Read
- Byte/Page Write
- Standard mode : 0 to 100 kHz clock frequency
- Fast Mode : 0 to 400 kHz clock frequency
- High Speed : 0 to 3.4 MHz clock frequency

The SDA signal is bidirectional and is used to read and write the serial data. The SCL signal is the clock generated by the host MCU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 3.4MHz, data are triggered on the rising edge of SCL.

10.1 Interface Operation

Figure 9. I²C Timing Diagram for FS-mode

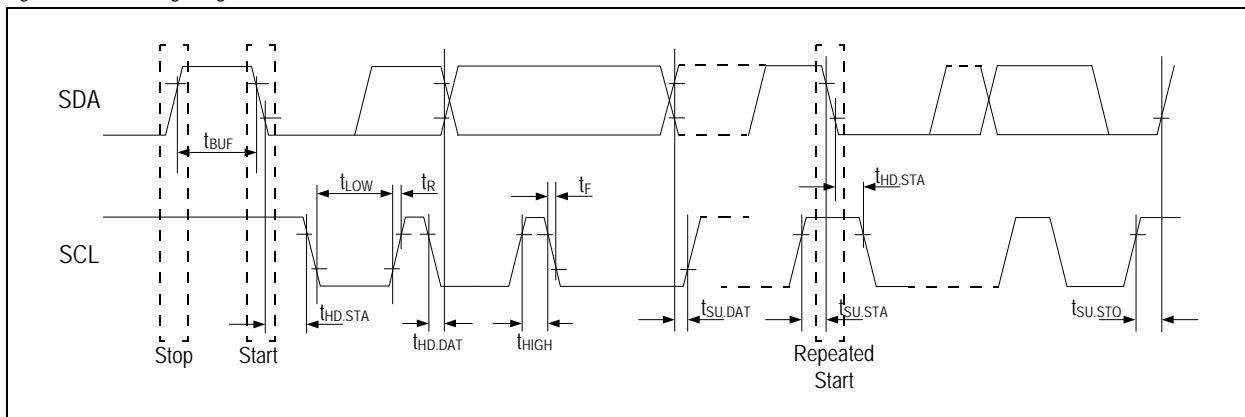
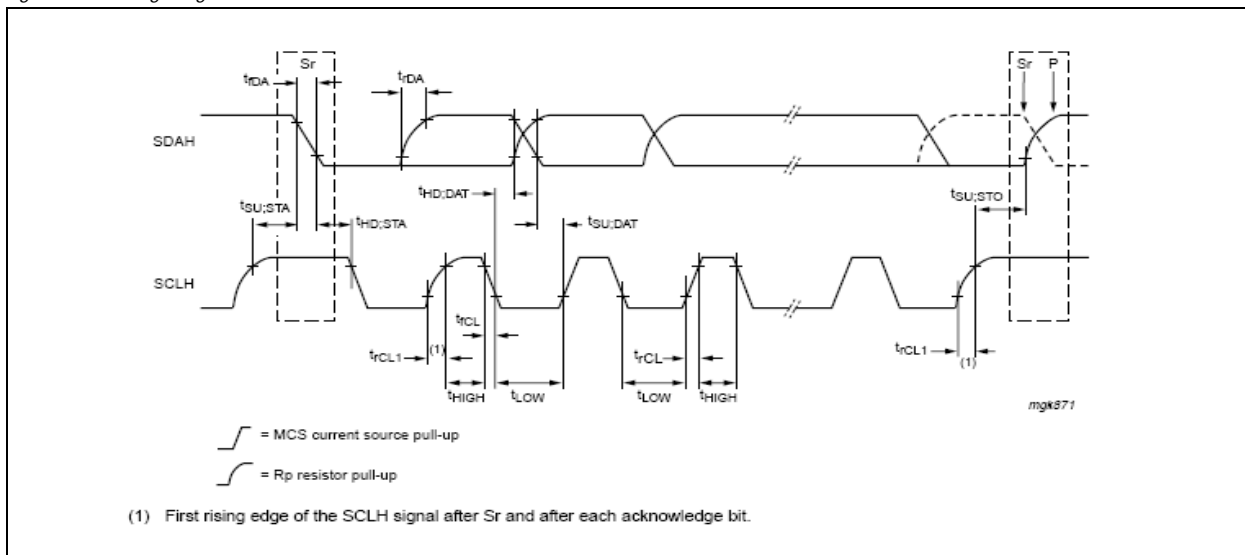


Figure 10. Timing Diagram for HS-mode



10.2 I²C Electrical Specification

Standard-mode, Fast-mode, High Speed-mode

| Symbol | Parameter | Condition | Min | Max | Unit |
|------------------|-----------------------------------------------------------------------------|------------------------------------------------|---------|-------------------------|------|
| V _{IL} | LOW-Level Input Voltage | | -0.5 | 0.3VDDp | V |
| V _{IH} | HIGH-Level Input Voltage | | 0.7VDDp | VDDp + 0.5 ¹ | V |
| V _{hys} | Hysteresis of Schmitt Trigger Inputs | VDDp < 2V | 0.1VDDp | - | V |
| V _{OL} | LOW-Level Output Voltage (open-drain or open-collector) at 3mA Sink Current | VDDp < 2V | - | 0.2VDDp | V |
| I _{CS} | Pull-up current of SCLH current source | SCLH output levels between 0.3VDDp and 0.7VDDp | 3 | 12 | mA |
| t _{SP} | Pulse Width of Spikes that must be suppressed by the Input Filter | | - | 10 | ns |
| I _i | Input Current at each I/O Pin | Input Voltage between 0.1VDDp and 0.9VDDp | - | 10 | μA |
| C _B | Total Capacitive Load for each Bus Line | | - | 400 | pF |
| C _{I/O} | I/O Capacitance (SDA, SCL) ² | | - | 10 | pF |

1. Maximum V_{IH} = VDDpmax + 0.5V or 5.5V, which ever is lower.

2. For capacitive bus loads between 100pF and 400pF, the timing parameters must be linearly interpolated.

10.3 I²C Timing

| Symbol | Parameter | Condition | FS-mode | | HS-mode C _B =100pF | | HS-mode C _B =400pF ¹ | | Unit |
|---------------------|--------------------------------------------------------------------------------------|--------------------------------------------------|----------------------|-----|-------------------------------|------|--------------------------------------------|------|------|
| | | | Min | Max | Min | Max | Min | Max | |
| fSCLK | SCL clock Frequency | | - | 400 | - | 3400 | - | 1700 | kHz |
| t _{BUF} | Bus Free Time; time between STOP and START condition | | 500 | - | 500 | - | 500 | - | ns |
| t _{HD;STA} | Hold time; (Repeated) START condition ² | | 600 | - | 160 | - | 160 | - | ns |
| t _{LOW} | LOW period of SCL clock | | 1300 | - | 160 | - | 320 | - | ns |
| t _{HIGH} | HIGH period of SCL clock | | 600 | - | 60 | - | 120 | - | ns |
| t _{SU;STA} | Setup time for a repeated START condition | | 600 | - | 160 | - | 160 | - | ns |
| t _{HD;DAT} | Data Hold Time ³ | | 0 | 900 | 0 | 70 | 0 | 150 | ns |
| t _{SU;DAT} | Data Setup Time ⁴ | | 100 | - | 10 | - | 10 | - | ns |
| t _{rCL} | Rise time of SCLH signal | External pull-up source of 3mA | - | - | 10 | 40 | 20 | 80 | ns |
| t _{rCL1} | Rise time of SCLH signal after repeated START condition and after an acknowledge bit | External pull-up source of 3mA | - | - | 10 | 80 | 20 | 160 | ns |
| t _R | Rise time of SDA and SCL signals | | 20+0.1C _B | 120 | - | - | - | - | ns |
| t _F | Fall time of SDA and SCL signals | | 20+0.1C _B | 120 | - | - | - | - | ns |
| t _{SU;STO} | Setup time for STOP condition | | 600 | - | 160 | - | 160 | - | ns |
| V _{nL} | Noise margin at LOW level | For each connected device (including hysteresis) | 0.1VDDp | - | 0.1VDDp | - | 0.1VDDp | - | V |
| V _{nH} | Noise margin at HIGH level | | 0.2VDDp | - | 0.2VDDp | - | 0.2VDDp | - | V |

1. For bus line loads C_b between 100 and 400 pF, the timing parameters must be linearly interpolated.
2. After this time the first clock is generated.
3. A device must internally provide a minimum hold time (300ns for Fast-mode, 80ns / max 150ns for High-speed mode) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
4. A fast-mode device can be used in standard-mode system, but the requirement t_{SU;DAT} = 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{Rmax} + t_{SU;DAT} = 1000 + 250 = 1250ns before the SCL line is released.

10.4 I²C Modes

The N40P112 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The N40P112 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

10.4.1 Automatic Increment of Address Pointer

The N40P112 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

10.4.2 Invalid Addresses

If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

10.4.3 Reading

When reading from a wrong address, the N40P112 slave data returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

10.4.4 Writing

A write to a wrong address is not acknowledged by the N40P112 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as start or stop signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy.

Both data and clock lines remain HIGH.

Start Data Transfer.

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer.

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid.

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

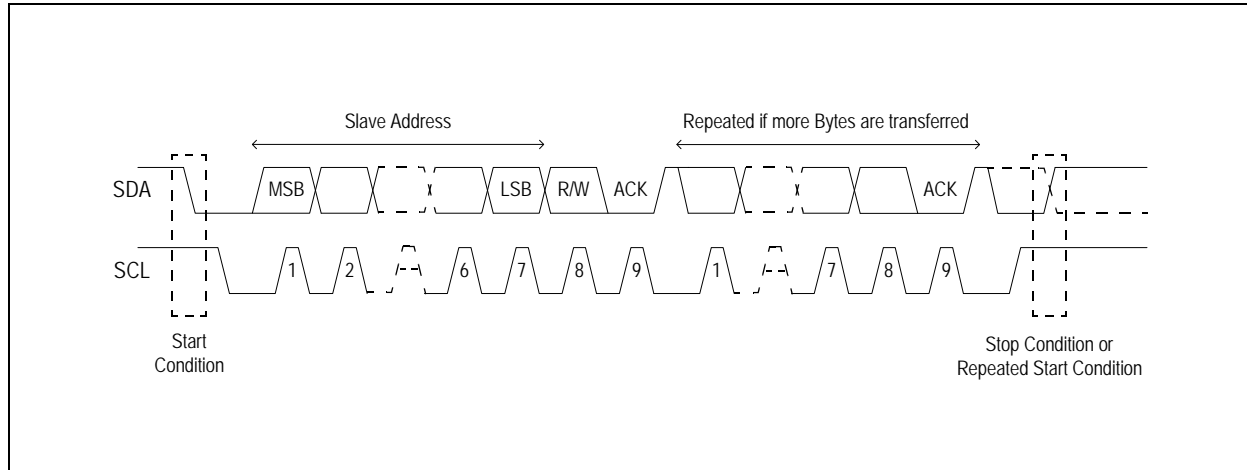
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge.

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of READ access to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 11. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



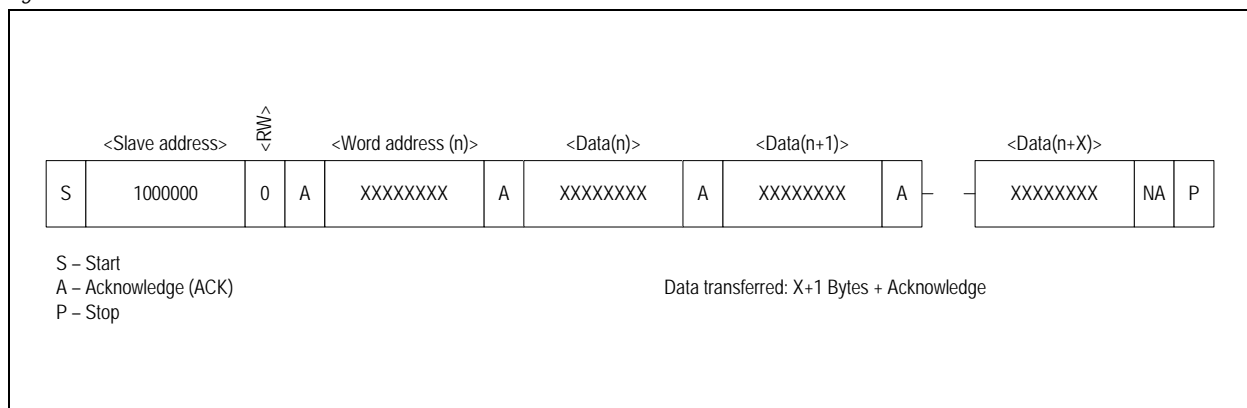
Depending upon the state of the R/W bit, two types of data transfer are possible:

- Data transfer from a master transmitter to a slave receiver:** The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a "not acknowledge". Data is transferred with the most significant bit (MSB) first.
- Data transfer from a slave transmitter to a master receiver:** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The N40P112 can operate in the following two modes:

- Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit (or by a not acknowledge depending on the address-pointer pointing to a valid position). START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 12). The slave address byte is the first byte received after the START condition. The slave address byte contains the 7-bit N40P112 address, which is stored in the OTP memory. The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA. After the N40P112 acknowledges the slave address + write bit, the master transmits a register address to the N40P112. This sets the address pointer on the N40P112. If the address is a valid readable address the N40P112 answers by sending an acknowledge. If the address-pointer points to an invalid position a "not acknowledge" is sent. The master may then transmit zero or more bytes of data. In case of the address pointer pointing to an invalid address the received data are not stored. The address pointer will increment after each byte transferred independent from the address being valid. If the address-pointer reaches a valid position again, the N40P112 answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the data write.

Figure 12. Data Write - Slave Receiver Mode



- Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the N40P112 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit N40P112 address. The default address is 80h. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The N40P112 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The N40P112 must receive a "not acknowledge" to end a read.

Figure 13. Data Read (from Current Pointer Location) - Slave Transmitter Mode

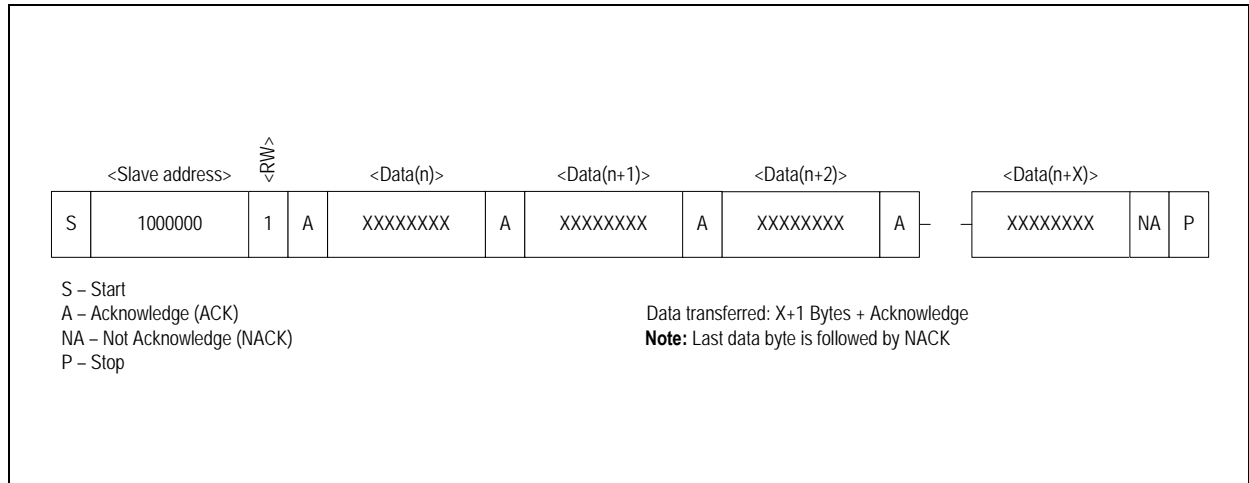
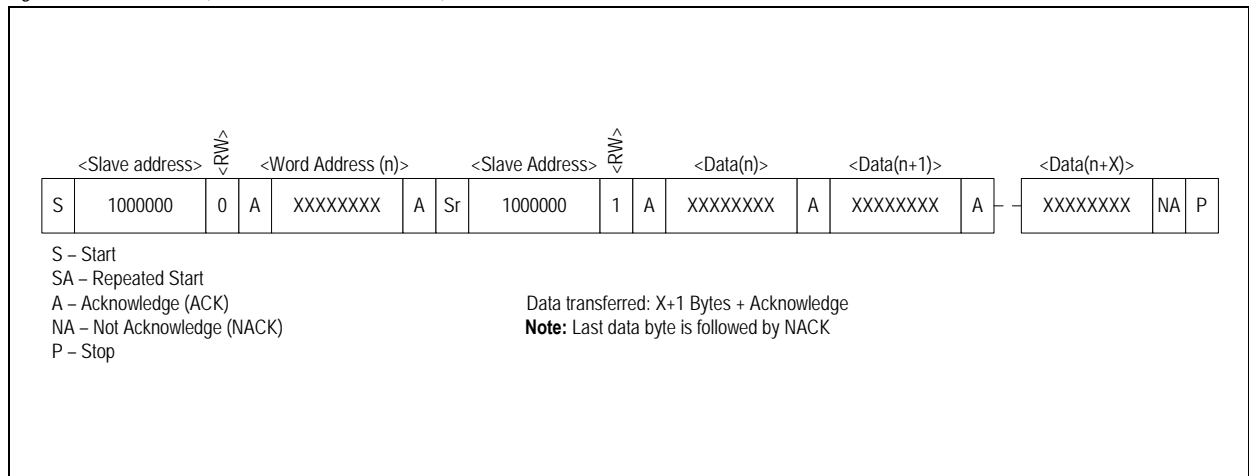


Figure 14. Data Read (from New Pointer Location) - Slave Transmitter Mode



10.4.5 High Speed Mode

The N40P112 is capable to work in HS-mode.

For switching to HS-mode the Master has to send the sequence: START, MASTER CODE, NACK. This sequence is sent in FS-mode. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge. After a device receives the master code it has to switch from FS-settings to HS-settings within $t_{SU,STA}$ which is 160ns for HS-mode. The device stays in HS-mode as long as it does not receive a STOP command. After receiving a STOP command it has to switch back from HS-settings to FS-settings, which has to be completed within the minimum bus free time t_{BUF} which is 500ns.

When switching to HS-mode the slave has to

- Adapt the SDAH and SCLH input filters according to the spike suppression requirement required in HS-mode. In HS-mode spikes up to 10ns, in FS-mode spikes up to 50ns have to be suppressed.
- Adapt the setup and hold times according to the HS-mode requirement. In HS-mode an internal hold time for SDA for START/STOP detection of 80ns (max. 150ns), in FS-mode an internal hold time of 160ns (max. 250ns) has to be provided.
- Adapt the slope control for SDAH output stage.

Figure 15. Data Transfer Format in HS-mode

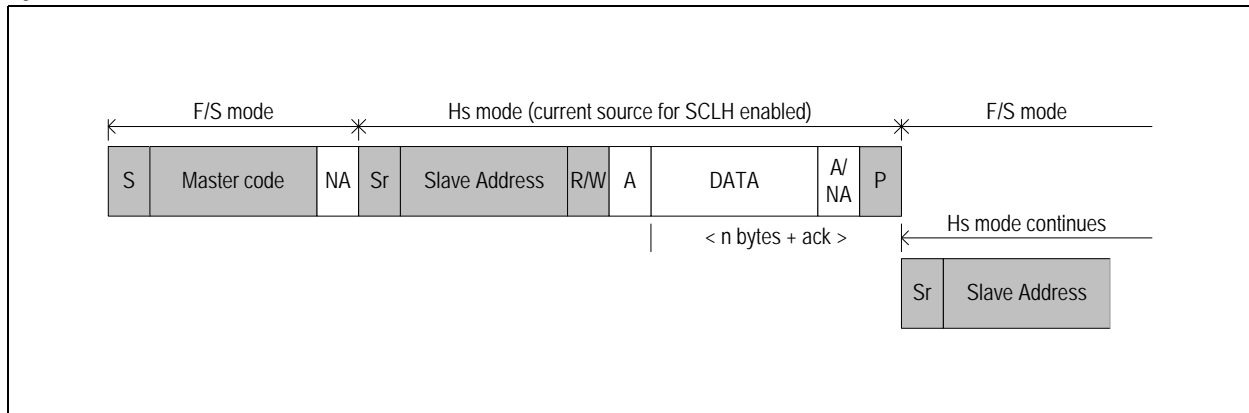
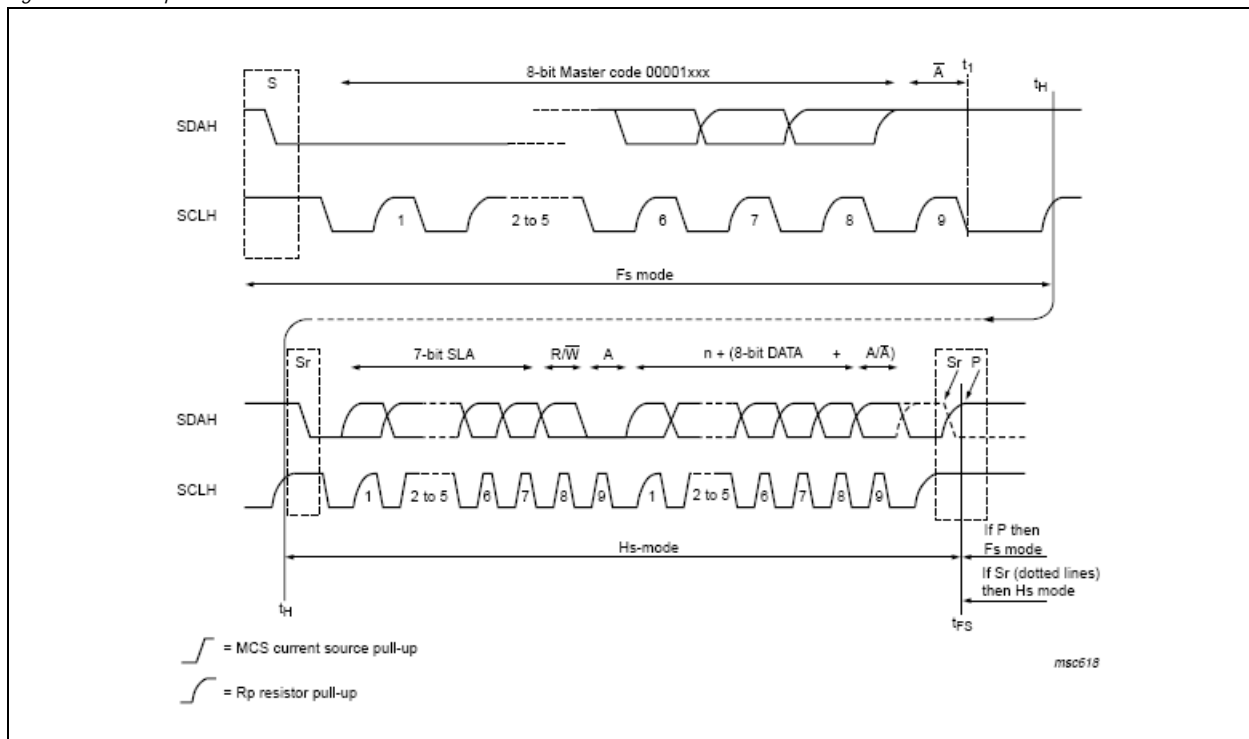


Figure 16. A Complete HS-mode Transfer



10.4.6 Automatic Increment of Address Pointer

The N40P112 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

10.4.7 Invalid Addresses

If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading: When reading from a wrong address, the N40P112 slave returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Writing: A write to a wrong address is not acknowledged by the N40P112 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

10.5 SDA, SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50ns. Furthermore, the SDA line is delayed by 120ns to provide an internal hold time for Start/Stop detection to bridge the undefined region of the falling edge of SCL. The delay needs to be smaller than $t_{HD,STA}$ 260ns.

For Standard-mode and Fast-mode an internal hold time of 300ns is required, which is not covered by the N40P112 slave.

11 I²C Registers

11.1 Control Register 1 (0Fh)

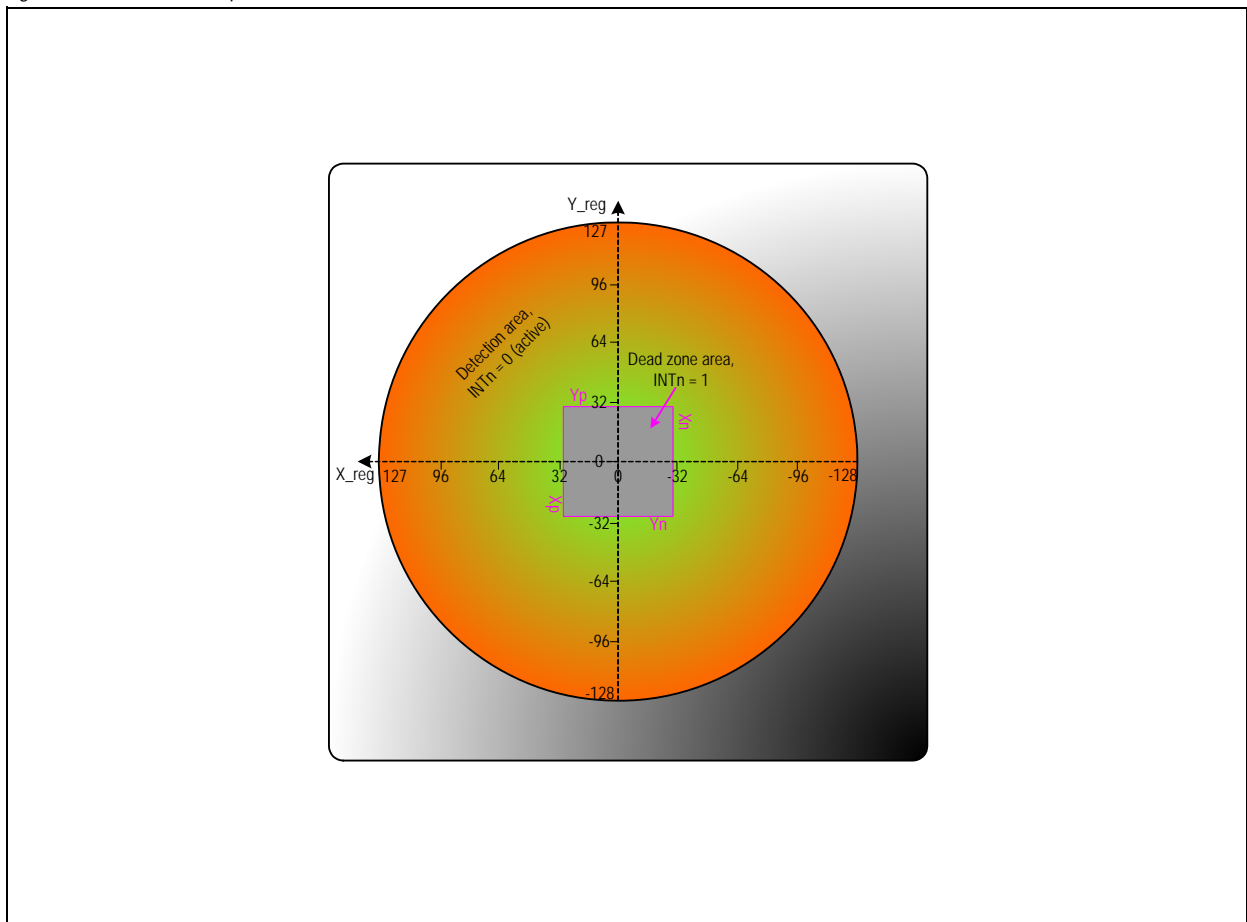
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|------------------|------------------|------------------|-------------|--------------|----------|------------|
| Idle | Time base bit[2] | Time base bit[1] | Time base bit[0] | INT_disable | INT_function | Soft_rst | Data_valid |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |
| Reset value: 1111 0000 | | | | | | | |

| Bit | Bit Description |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 | 0 = Low Power Mode The measurements are triggered with an internal low power oscillator – the user can select between 8 different timings by setting the low power timebase (Control Register 1 [6:4]) |
| | 1 = Idle Mode (default) A new measurement cycle is started after the I ² C ACK bit following the read out of the Y-coordinate 11h. The readout rate and thus the power consumption is externally controlled by the host MCU. |
| 6:4 | Low Power time base Configure the time base of the automatic wakeup in Low Power Mode (see Table 7). |
| 3 | 0 = Interrupt output INTn is enabled (default) |
| | 1 = Interrupt output INTn is disabled and is fixed to '1' (Hi-Z) |
| 2 | 0 = Interrupt output INTn is active '0' after each measurement (default): <ul style="list-style-type: none"> - Automatically triggered in Low Power mode, depending on the time base chosen - 450µs after Y readout in Idle mode The interrupt is cleared after the I ² C ACK bit following the read out of the Y-coordinate 11h. In block read mode, the several other bytes could be transferred before the interrupt is cleared. |
| | 1 = Interrupt output INTn is active '0' when the movement of the magnet exceeds the Dead Zone area (see Figure 17). The Dead Zone area is set by registers Xp (Reg 12h), Xn (Reg 13h), Yp (Reg 14h), Yn (Reg 15h). The interrupt is cleared after the I ² C ACK bit following the read out of the Y-coordinate 11h, and will be active '0' at the next measurement if the magnet is still in the Detection Area. In block read mode, several other bytes can be transferred before the interrupt is cleared. It is recommended to use this mode with the Low Power mode (Idle = 0), in order to wake up automatically a system when the magnet has been moved away from the center. The polling time is the Low Power time base bit [6:4]. |
| 1 | 0 = Normal mode (default) |
| | 1 = Reset mode. All the internal registers are loaded with their reset value. The Control Register 1 is loaded as well with the value 1111 0000, then the Soft_rst bit goes back to 0 once the internal reset sequence is finished. |
| 0 | 0 = Conversion of new coordinates ongoing, no valid coordinate is present in the X and Y_res_int registers. Reading those registers at that moment can give wrong values. |
| | 1 = New coordinate values are ready in X and Y_res_int registers. |

Table 7. Configuration

| Low Power time base CONFIG_REG1 0Fh [6:4] | $\Delta t_{\text{timebase}}$ | |
|----------------------------------------------|------------------------------|------|
| | Value | Unit |
| 000b | 20 | ms |
| 001b | 40 | ms |
| 010b | 80 | ms |
| 011b | 100 | ms |
| 100b | 140 | ms |
| 101b | 200 | ms |
| 110b | 260 | ms |
| 111b (default) | 320 | ms |

Figure 17. Dead Zone Representation with INT_function=1



Note: The values in Control Register 1, X_register and Y_res_int register are frozen when the I²C address pointer is set to 0Fh, 10h or 11h. This ensures that the Data_valid bit, X and Y values are taken at the same time. In order to get updated values from those registers, set the address pointer to any other address.

11.2 X Register (10h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| X[7] | X[6] | X[5] | X[4] | X[3] | X[2] | X[1] | X[0] |
| R | R | R | R | R | R | R | R |

Reset value: 0000 0000

| Bit | Bit Description |
|-----|-------------------------------------------------------------------------------------------------------------------|
| 7:0 | X coordinate, Two's complement format (signed -128 ~ +127). Positive X values represent left side knob movements. |

11.3 Y_res_int Register (11h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Y[7] | Y[6] | Y[5] | Y[4] | Y[3] | Y[2] | Y[1] | Y[0] |
| R | R | R | R | R | R | R | R |

Reset value: 0000 0000

| Bit | Bit Description |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Y coordinate, Two's complement format (signed -128~+127). Reading this register will reset the INTn output to Hi-Z, after the ACK bit of Y_res_int register readback. |

11.4 Xp Register (12h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Xp[7] | Xp[6] | Xp[5] | Xp[4] | Xp[3] | Xp[2] | Xp[1] | Xp[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value: 0000 0101 (5d)

| Bit | Bit Description |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Xp range value, Two's complement (signed: -128 ~ +127). Determines the LEFT threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register 1 (0Fh) on page 23). |

11.5 Xn Register (13h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Xn[7] | Xn[6] | Xn[5] | Xn[4] | Xn[3] | Xn[2] | Xn[1] | Xn[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset value: 1111 1011 (-5d)

| Bit | Bit Description |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Xn range value, Two's complement (signed: -128 ~ +127). Determines the RIGHT threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register 1 (0Fh) on page 23). |

11.6 Yp Register (14h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Yp[7] | Yp[6] | Yp[5] | Yp[4] | Yp[3] | Yp[2] | Yp[1] | Yp[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| <i>Reset value: 0000 0101 (5d)</i> | | | | | | | |

| Bit | Bit Description |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Yp range value, Two's complement (signed: -128 ~ +127). Determines the TOP threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register 1 (0Fh) on page 23). |

11.7 Yn Register (15h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Yn[7] | Yn[6] | Yn[5] | Yn[4] | Yn[3] | Yn[2] | Yn[1] | Yn[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| <i>Reset value: 1111 1011 (-5d)</i> | | | | | | | |

| Bit | Bit Description |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Yn range value, Two's complement (signed: -128 ~ +127). Determines the BOTTOM threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register 1 (0Fh) on page 23). |

11.8 M_ctrl Register (2Bh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| M_ctrl[7] | M_ctrl[6] | M_ctrl[5] | M_ctrl[4] | M_ctrl[3] | M_ctrl[2] | M_ctrl[1] | M_ctrl[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| <i>Reset value: 0000 0000 (00h)</i> | | | | | | | |

| Bit | Bit Description |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Middle hall element control register. The M_ctrl register must be set to 00h (default value) after power up for N40P112 module. |

11.9 J_ctrl Register (2Ch)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| J_ctrl[7] | J_ctrl[6] | J_ctrl[5] | J_ctrl[4] | J_ctrl[3] | J_ctrl[2] | J_ctrl[1] | J_ctrl[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| <i>Reset value: 0000 0110 (06h)</i> | | | | | | | |

| Bit | Bit Description |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Sector dependent attenuation of the outer Hall elements. The J_ctrl register must be set to 06h (default value) after power up for N40P112 module. |

11.10 T_ctrl Register (2Dh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| T_ctrl[7] | T_ctrl[6] | T_ctrl[5] | T_ctrl[4] | T_ctrl[3] | T_ctrl[2] | T_ctrl[1] | T_ctrl[0] |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| <i>Reset value: 0000 1001 (09h)</i> | | | | | | | |

| Bit | Bit Description |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Scaling control register. This register controls the scaling factor of the XY coordinates to fit to the 8-bit X and Y register (full dynamic range). The T_ctrl register must be set to 0Dh after power up for N40P112 module. |

11.11 Control Register 2 (2Eh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------------|-------|-------|-------|-------|-------|--------------|-------|
| Test | Test | Test | Test | Test | Test | inv_spinning | Test |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| <i>Reset value: 1000 0100</i> | | | | | | | |

| Bit | Bit Description |
|-----|-------------------------------------------------------------|
| 7 | Test bit. Must configured '1'. |
| 6:3 | Test bit. Must configured '0'. |
| 2 | Test bit. Must configured '1'. |
| 1 | Magnet Polarity. Must be set to '0' with EasyPoint modules. |
| 0 | Test bit. Must be '0'. |

11.12 Registers Table

The following registers / functions are accessible over the serial I²C interface.

Table 8. Registers

| Register | Number of bits | Access | Address | Format | Reset Value | Bit | Description |
|---------------------------------|----------------|--------|---------|-------------|-----------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IC Identification | | | | | | | |
| ID Code | 8 | R | 0C | | 0Ch | <7:0> | 8 bit Manufacture ID Code |
| ID Version | 8 | R | 0D | | 0Dh | <7:4> | 8 bit Component ID Version |
| Silicon Revision | 8 | R | 0E | | 00h | <7:0> | 8 bit Silicon Revision |
| Control_register_1 | | | | | | | |
| Idle | 1 | R/W | 0Fh | | 1b | <7> | 1 : Idle mode 0 : Low Power mode |
| Low_power_timebase | 3 | R/W | 0Fh | | 111b | <6:4> | Low Power readout time base register |
| INT_disable | 1 | R/W | 0Fh | | 0b | <3> | Disables the interrupt functionality. 1 : Interrupt disabled 0 : Interrupt enabled |
| INT_function | 1 | R/W | 0Fh | | 0b | <2> | Interrupt control register 0 : Interrupt goes low with every new calculated x/y coordinates 1 : Interrupt pin goes low in when new x/y coordinates are calculated and the magnet has exited the xp, xn, yp, yn threshold values |
| soft_rst | 1 | R/W | 0Fh | | 0b | <1> | Soft Reset 0 : Normal mode 1 : All registers return to their respective reset value |
| data_valid | 1 | R | 0Fh | | 0b | <0> | Data valid indicator 0 : X/Y calculation ongoing 1 : X/Y calculation finished, coordinates ready |
| X/Y Coordinate Registers | | | | | | | |
| x | 8 | R | 10h | two's comp. | 00h | <7:0> | Result X coordinate |
| y_res_int | 8 | R | 11h | two's comp. | 00h | <7:0> | Result Y coordinate, resets the interrupt flag |
| Range Settings | | | | | | | |
| xp | 8 | R/W | 12h | two's comp. | 5h (5 dec) | <7:0> | Wake up threshold @ positive X -direction |
| xn | 8 | R/W | 13h | two's comp. | FBh (-5 dec) | <7:0> | Wake up threshold @ negative X -direction |
| yp | 8 | R/W | 14h | two's comp. | 5h (5 dec) | <7:0> | Wake up threshold @ positive Y -direction |
| yn | 8 | R/W | 15h | two's comp. | FBh (-5 dec) | <7:0> | Wake up threshold @ negative Y -direction |
| Channel voltages (3) | | | | | | | |
| c4_neg <11:8> | 4 | R | 16h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 4, negative current spinning Sign extended to 8 bit |
| c4_neg <7:0> | 8 | R | 17h | two's comp. | 00h | <7:0> | Voltage @ channel 4, negative current spinning |
| c4_pos <11:8> | 4 | R | 18h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 4, positive current spinning Sign extended to 8 bit |
| c4_pos <7:0> | 8 | R | 19h | two's comp. | 00h | <7:0> | Voltage @ channel 4, positive current spinning |

Table 8. Registers

| Register | Number of bits | Access | Address | Format | Reset Value | Bit | Description |
|-------------------------------------------|----------------|--------|---------|-------------|-------------|----------------|-----------------------------------------------------------------------------------|
| c3_neg <11:8> | 4 | R | 1Ah | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 3, negative current spinning Sign extended to 8 bit |
| c3_neg <7:0> | 8 | R | 1Bh | two's comp. | 00h | <7:0> | Voltage @ channel 3, negative current spinning |
| c3_pos <11:8> | 4 | R | 1Ch | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 3, positive current spinning Sign extended to 8 bit |
| c3_pos <7:0> | 8 | R | 1Dh | two's comp. | 00h | <7:0> | Voltage @ channel 3, positive current spinning |
| | | | | | | | |
| c2_neg <11:8> | 4 | R | 1Eh | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 2, negative current spinning Sign extended to 8 bit |
| c2_neg <7:0> | 8 | R | 1Fh | two's comp. | 00h | <7:0> | Voltage @ channel 2, negative current spinning |
| c2_pos <11:8> | 4 | R | 20h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 2, positive current spinning Sign extended to 8 bit |
| c2_pos <7:0> | 8 | R | 21h | two's comp. | 00h | <7:0> | Voltage @ channel 2, positive current spinning |
| | | | | | | | |
| c1_neg <11:8> | 4 | R | 22h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 1, negative current spinning Sign extended to 8 bit |
| c1_neg <7:0> | 8 | R | 23h | two's comp. | 00h | <7:0> | Voltage @ channel 1, negative current spinning |
| c1_pos <11:8> | 4 | R | 24h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 1, positive current spinning Sign extended to 8 bit |
| c1_pos <7:0> | 8 | R | 25h | two's comp. | 00h | <7:0> | Voltage @ channel 1, positive current spinning |
| | | | | | | | |
| c5_neg <11:8> | 4 | R | 26h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 5, negative current spinning Sign extended to 8 bit |
| c5_neg <7:0> | 8 | R | 27h | two's comp. | 00h | <7:0> | Voltage @ channel 5, negative current spinning |
| c5_pos <11:8> | 4 | R | 28h | two's comp. | 00h | <3:0> <7:4> | Voltage @ channel 5, positive current spinning Sign extended to 8 bit |
| c5_pos <7:0> | 8 | R | 29h | two's comp. | 00h | <7:0> | Voltage @ channel 5, positive current spinning |
| Control Register for the Algorithm | | | | | | | |
| M_ctrl | 8 | R/W | 2Bh | | 00h | <7:0> | Middle Hall element control For N40P112, configure to 00h (default) |
| J_ctrl | 8 | R/W | 2Ch | | 06h | <7:0> | Attenuation of the outer Hall elements For N40P112, configure to 06h (default) |
| T_ctrl | 8 | R/W | 2Dh | | 09h | <7:0> | Scaling factor of XY coordinates For N40P112, configure to 0Dh |
| Control_register_2 | | | | | | | |
| Test | 1 | R/W | 2Eh | | 1b | <7> | Test only, must be '1' |
| Test | 1 | R/W | 2Eh | | 0b | <6> | Test only, must be '0' |
| Test | 1 | R/W | 2Eh | | 0b | <5> | Test only, must be '0' |
| Test | 1 | R/W | 2Eh | | 0b | <4> | Test only, must be '0' |
| Test | 1 | R/W | 2Eh | | 0b | <3> | Test only, must be '0' |
| Test | 1 | R/W | 2Eh | | 1b | <2> | Test only, must be '1' |
| inv_spinning | 1 | R/W | 2Eh | | 0b | <1> | Invert the channel voltage. For N40P112, set to '0' |
| Test | 1 | R/W | 2Eh | | 0b | <0> | Test only, must be '0' |

12 Package Drawings and Markings

Figure 18. N40P112 Dimensions (mm ±0.15)

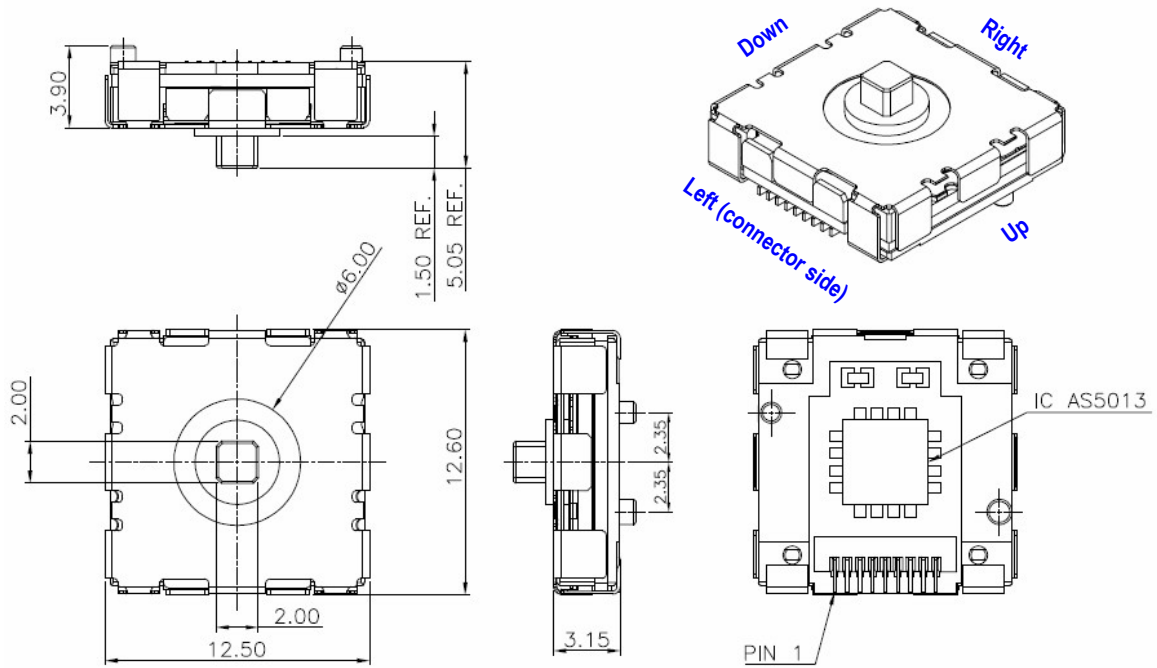


Figure 19. Recommended PCB Layout (mm ±0.05)

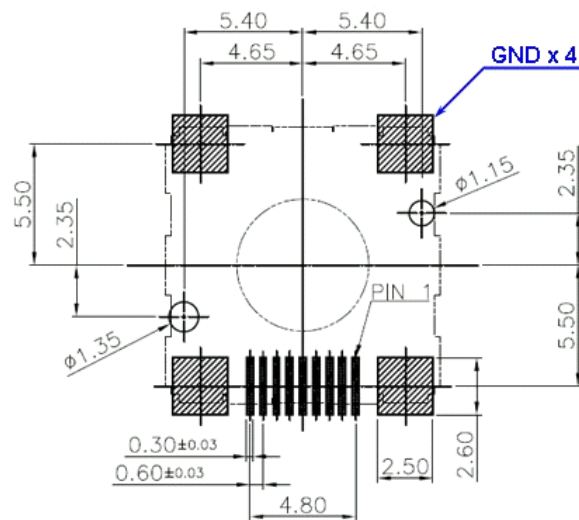
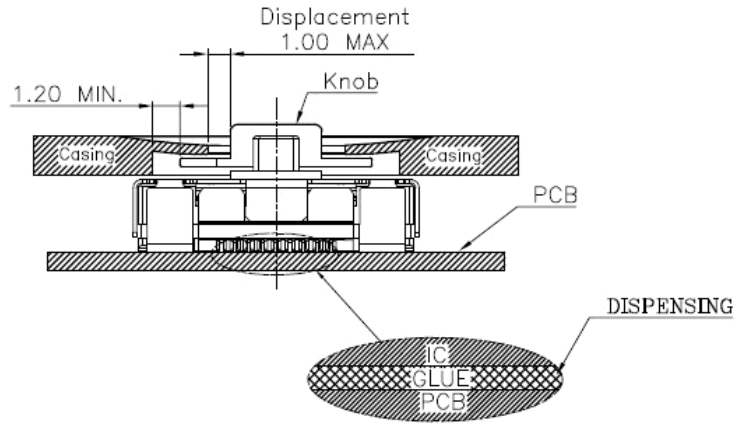


Figure 20. Recommended on Casing Design & Mounting Note



Revision History

| Revision | Date | Owner | Description |
|----------|--------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0.8 | 16 Jul, 2010 | jlu | Initial release |
| 1.0 | 01 Dec, 2010 | | Updated Applications on page 1 and url in the footer |
| 1.1 | 16 Feb, 2011 | | Updated sections 8.3.1 , 10 , 10.2 , 10.3 , 11.1 , 11.3 , 11.10 , 11.11 , 11.12 |

Note: Typos may not be explicitly mentioned under revision history.

13 Ordering Information

The devices are available as the standard products shown in [Table 9](#).

Table 9. Ordering Information

| Ordering Code | Description | Delivery Form |
|-----------------|-----------------------------|---------------|
| N40P112-00001-H | 0.35N (± 0.10 N) force | Tubes |
| N40P112-00011-H | 0.35N (± 0.10 N) force | Tape & Reel |
| N40P112-00002-H | 0.55N (± 0.15 N) force | Tubes |
| N40P112-00012-H | 0.55N (± 0.15 N) force | Tape & Reel |

Note: All products are RoHS compliant.

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Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpemstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

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