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Datasheet: AS8515 Data Acquisition System with Power Management and LIN Transceiver for 12V Battery Sensor Applications

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AS8515

Data Acquisition System with Power Management and LIN Transceiver for 12V Battery Sensor Applications

1 General Description

The AS8515 is designed for simultaneous measurement of shunt current sensor signal and battery voltage by two independent ADC channels. Both channels can measure small signals up to ±160 mV versus ground through programmable gain amplifier or larger signals in the 1V range without amplifier. After analog to digital conversion and digital filtering, the resulting digital values are accessible through 4-wire serial interface. The device is powered directly from the battery through LDO and provides a 3.3V supply for an external microcontroller. For communication with the next level ECU, the device offers a LIN 2.1 transceiver. Measurement of battery voltage is supported through resistive attenuator with disable for power saving in standby.

The device is a stacked die system providing a high voltage CMOS IC for power management and transceiver functions as a *Top die* and low voltage sensor interface functions as a *Bottom die* inside a 32-pin MLF (5x5 mm) package.

2 Key Features

- A precision voltage attenuator with power down facility
- LIN 2.1 transceiver
- Power-On Reset with OTP adjustable reset timeout and brown-out detection
- A window Watchdog function in the normal mode and a timeout Watchdog in the device standby mode as a factory option
- Load dump protection (42V) for all battery supplied pins, LIN bus pin, and Enable pin
- Internal reverse polarity protection (up to -27V) for all battery-sensing pins, and LIN bus pin
- Over temperature warning & shutdown functions
- Two independent high resolution A/D converters with programmable over sampling ratio
- Programmable sampling rate up to 4kHz throughput
- Programmable gain, low noise amplifier for current channel with gain stages 5, 25, 40, 100
- Internal temperature sensor
- Synchronous acquisition for both ADC channels
- Reference-voltage source (high precision and high stability)
- Offset auto zero architecture on both channels
- Current monitoring comparator with interrupt signal generation and µC clock enable. Timer with 2 related outputs for single shot sampling of current and voltage channel in low power mode.
- Precision on chip RC oscillator or external clock. Low slew, low EMC clock output which can be used by external microcontroller which is enabled respectively disabled by mode control through SPI and interrupt from current monitor in low power mode.

The integrated circuit can execute measurements with internal and external sensors and sources for the voltage channel and with external sensor for the current channel.

External Sensors:

- Current measurement via Shunt resistor (4 ranges)
- Battery voltage (internal voltage divider to battery)
- ETR and ETS for external temperature sensor (with switchable current source)

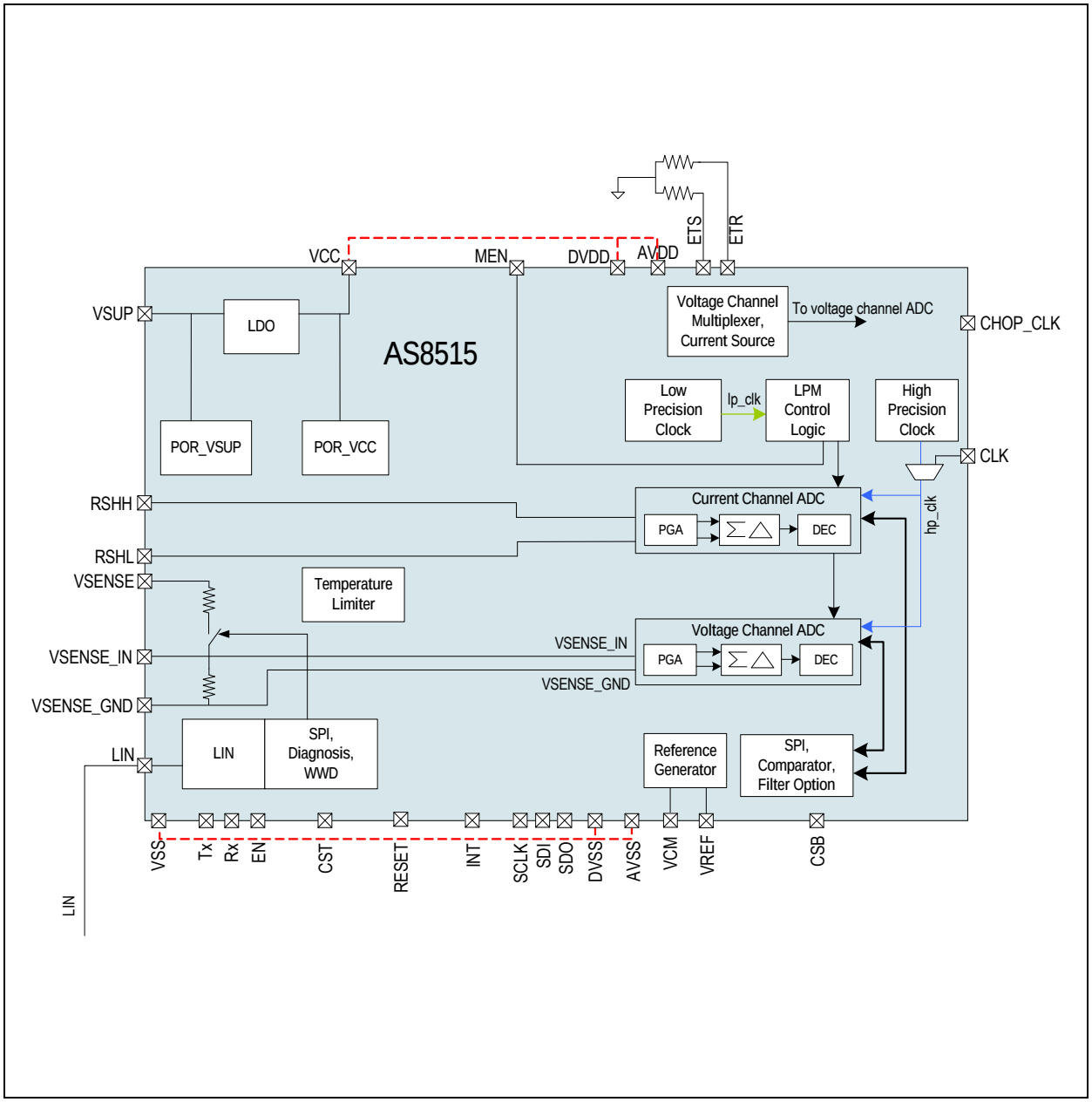
Internal Sensors:

- On chip temperature sensor
- Internal current sources for functional test of measurement path and the connection of shunt resistor

3 Applications

The AS8515 is suitable for battery sensors, having shunt current sensor at minus pole. For lead acid, AGM, Li-Ion batteries up to 18V nominal, 42V over voltage capability.
The device is also ideal as a general purpose sensor interface for automotive LIN slaves.

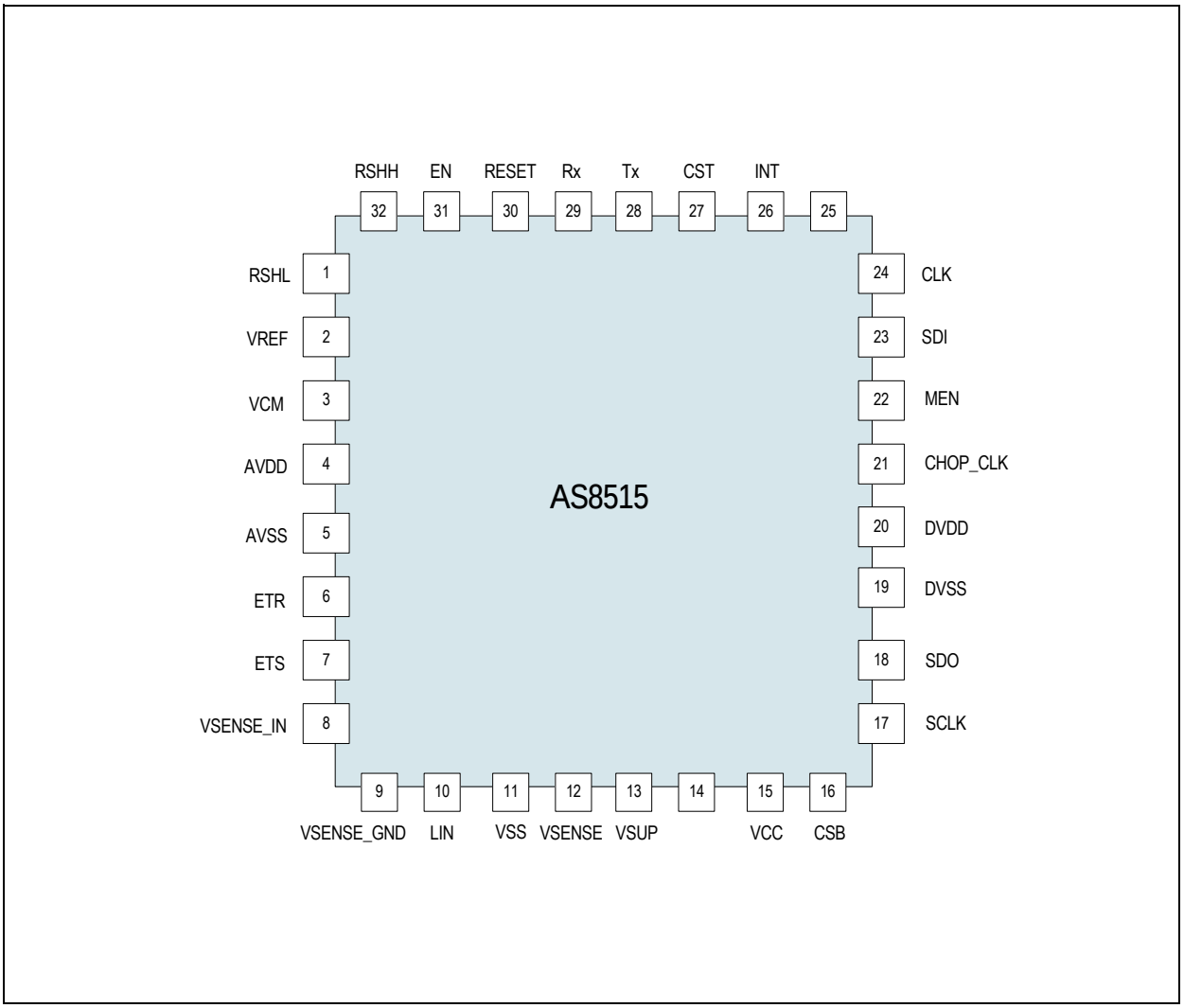
Figure 1. AS8515 Block Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
RSHL	1	Analog input	Negative differential input for current channel
VREF	2	Analog output	Internal reference voltage to Sigma Delta ADC; Connect 100nF to AVSS from this pin.
VCM	3	Analog output	Common mode voltage to the internal measurement path; Connect 100nF to AVSS from this pin.
AVDD [1]	4	Analog input	+3.3V Power-supply; Supplied by LDO output (VCC) in *Top die*; Should be shorted to pin 21 (VCC) externally.
AVSS [2]	5	Power supply	0V Power-supply Ground analog

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
ETR	6	Analog input	Voltage channel single ended input
ETS	7		
VSENSE_IN	8	Analog I/O	Battery voltage attenuator output and voltage channel input
VSENSE_GND	9	Analog input	Input signal for voltage channel (low)
LIN	10	Analog I/O	LIN BUS
VSS [2]	11	Power supply	0V Power-supply Ground analog
VSENSE	12	Analog input	Battery voltage input Connect 100nF to VSS from this pin.
VSUP	13	Power supply	Supply input from battery (through external reverse polarity protection device)
-	14	-	-
VCC [1]	15	Analog output	Regulated 3.3V output supply for loads up to 50mA
CSB	16	Digital input	Chip select for *Bottom die*
SCLK	17	Digital input	Clock signal SPI
SDO	18	Digital output	Data signal SDO
DVSS[2]	19	Power supply	0V Power-supply digital
DVDD [1]	20	Analog input	+3.3V Power-supply; Supplied by LDO output (VCC) in *Top die*; Should be shorted to pin 21(VCC) externally.
CHOP_CLK	21	Digital output	Chopper clock
MEN	22	Digital I/O	Digital output for *Bottom die* in SBM mode[3] and input for *Top die*
SDI	23	Digital I/O	Data signal SDI
CLK	24	Digital I/O	Internal/External digital clock signal
-	25	-	-
INT	26	Digital I/O	Interrupt not: Wake-up, digital interrupt, ready flag 2
CST	27	Digital input	Chip select for *Top die*
Tx	28	Digital I/O	LIN transceiver transmit pin
Rx	29	Digital I/O	LIN transceiver receive pin
RESET	30	Digital output	Reset output (open drain)
EN	31	Digital input	Enable input
RSHH	32	Analog input	Positive differential input for current channel

1. Pin #4, pin #20 and pin #21 needs to be shorted externally on the board. Pin #21 is the LDO output that supplies pin #4 and pin #20.
2. Pin #5, pin #11 and pin #19 needs to be shorted externally on the board as they are the grounds.
3. Use as output port only.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrical Parameters						
VSUP	Supply voltages	-0.3		42	V	
VSENSE	Battery voltage inputs	-27		42	V	
AVDD, DVDD	DC supply voltage	-0.3		5	V	
EN	Enable input	-0.3		42	V	
VCC	Regulated output supplies	-0.3		5	V	VCC generated by *Top die* must not be larger than 5V on board level as it has to be connected with *Bottom die* AVDD and AVCC
LIN	LIN bus	-27		40	V	
	Analog & digital inputs and outputs	-0.3		5	V	
	Input current (latch-up immunity)	-100		100	mA	Norm: AEC-Q100 – or Jedec 78
Electrostatic Discharge						
ESD	Electrostatic discharge Norm: AEC-Q100	±6			kV	LIN, VSS
		±4			kV	VSUP, VSENSE
		±2			kV	All other pins
Continuous Power Dissipation						
P_{tot} [1]	Total operating power dissipation (all supplies and outputs)			0.375	W	MLF-32 in still air, soldered on JEDEC standard board @125º ambient, static operation = no time limit
Temperature Ranges and Storage Conditions						
R_{Θ}	Package thermal resistance		34	40	ºC/W	
T_{stg}	Storage temperature	-55		150	ºC	
T_J	Junction temperature			130	ºC	
T_{BODY}	Package body temperature			260	ºC	*The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).*
	Soldering conditions			250	ºC	
	Humidity non-condensing	5		85	%	

1. Total power dissipation cannot exceed 0.375W to avoid increase in junction temperature, i.e. greater than 130ºC. VCC LDO can supply current externally, which is not greater than 17mA at 18V VSUP and 20mA at 16V VSUP.

6 Electrical Characteristics

Unless otherwise noted in this specification, all defined tolerances of parameters are assured over the whole operation conditions range and also over lifetime.

6.1 Operating Conditions

Table 3. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUP}	Supply voltages	4.3		18	V	
V_{SENSE}	Battery voltage input	4.5		18	V	
AVDD	Positive supply voltage	3.15		3.45	V	
AVSS	Negative supply voltage	0		V		
DVDD	Positive digital supply voltage	3.15		3.45	V	Referring to DVSS, Typical ±10%
DVSS	Negative digital supply voltage	0			V	
LIN	LIN bus	0		18	V	
EN	Enable input	0		18	V	
VCC	Regulated output supply	3.15		3.45	V	
T_{AMB}	Ambient temperature	-40		115	ºC	Maximum junction temperature (T_J) is 130ºC
I_{SUP} [1]	Supply current			27	mA	
f_{CLK}	System clock frequency		8.192		MHz	When external clock is selected, internal clock will be 4.096 MHz

1. Total power dissipation cannot exceed 0.375W to avoid increase in junction temperature, i.e. greater than 130ºC. VCC LDO can supply current externally, which is not greater than 17mA at 18V VSUP and 20mA at 16V VSUP.

6.2 DC/AC Characteristics for Digital Inputs and Outputs

All pull-up, pull-downs have been implemented with active devices. SDO have been measured with 10pF load.

INT Output.

Table 4. INT

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				4	mA

CST, CSB, TxD.

Table 5. CST, CSB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current		-1		+1	µA
I_{PU}	Pull-up current	Pulled to GND	-150		-10	µA

SDI, SCLK.

Table 6. SDI, SCLK

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{LEAK}	Input leakage current		-1		+1	µA

SDO Output.

Table 7. SDO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				4	mA

CHOP_CLK Output.

Table 8. CHOP_CLK

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				4	mA

EN Input.

Table 9. EN

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		0.8*VCC			V
V_{IL}	Low level input voltage				0.2*VCC	V
I_{LEAK}	Input leakage current	EN = VSS	-1		+1	µA
I_{pd_en}	Pull-down current	Pulled up to VCC	30		100	µA

CLK I/O.

Table 10. CLK I/O

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		2.4			V
V_{IL}	Low level input voltage				1	V
I_{LEAK}	Input leakage current		-1		+1	µA
I_{PD_EN}	Pull-down current		10		100	µA
I_O	Output current				4	mA
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V

MEN Output.

Table 11. MEN

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				2	mA

Rx Output.

Table 12. Rx

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		VCC-0.5			V
V_{OL}	Low level output voltage				VSS+0.4	V
I_O	Output Current				1	mA
I_{pu_reset}	Pull-up current	Pulled down to VSS	-30		-100	µA

RESET Output.

Table 13. RESET

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current	Open Drain Pull-down			8	mA

6.3 System Specifications

Table 14. System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Ivsupnom	Current consumption in normal mode	No load on VCC, LIN bus in dominant state			7	mA
Ivsupstdby	Current consumption standby	No load on VCC, LIN bus in recessive state		80		µA

Note: Stand by mode power consumption is sum of stop mode power consumption and average of normal mode power consumption over a period of 2s (NOM1 time of device is low in Standby mode).

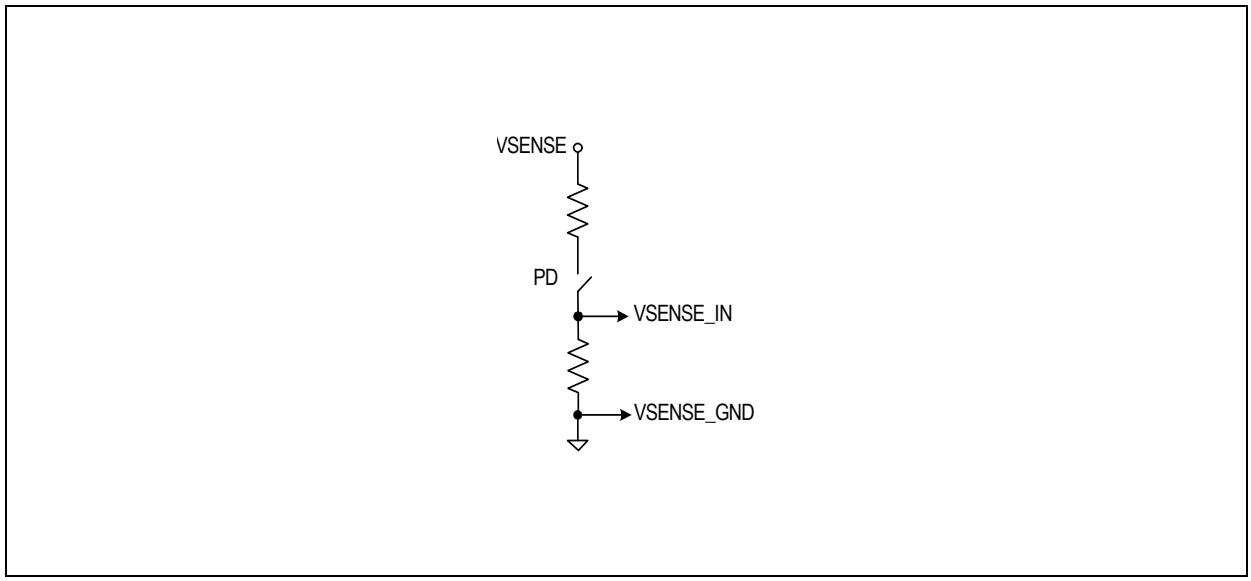
7 AS8515 Top Die Overview

The AS8515 *Top die* consists of a resistive divider, a low dropout regulator, and a LIN bus transceiver. Additionally integrated are a RESET unit with a power-on-reset delay, programmable window watchdog and timeout watchdog timers. It also includes a watchdog timeout on LIN Tx node to indicate if the Microcontroller is stuck in a loop and the LIN bus remains in dominant time for more than the necessary time.

7.1 Voltage Attenuator

A resistive divider is used as a battery voltage attenuator. Like the amplifier, the attenuator can be enabled or disabled through SPI, and in the device standby mode, we additionally need logic high on MEN pin for enabling. Internal reverse polarity protection is provided for VSENSE pin.

Figure 3. Attenuator Implementation



7.2 Voltage Regulators (LDO)

The device has a low-dropout voltage regulator named LDO, 3.3V voltage outputs. The output of the LDO is VCC. The regulator is always ON except when the device enters the over-temperature shutdown.

The regulator has in-built short-circuit current limitation feature. The regulator can be temporarily shut down for hard reset of the external circuitry by configuring the device to temporary shutdown mode through SPI.

The LDO power-up happens when the POR-VSUP event occurs (RESET_VSUP_N switching from low to high). The LDO will be switched off if there is an under voltage on VCC, that is, when RESET_VCC_N switches back to low.

7.3 LIN Transceiver

The device has a LIN transceiver with slew-controlled bus driver for controlling the electromagnetic emissions from the LIN bus. Further, the slew rate is independent of the bus load. The transmitter relays the data from the LIN controller (Tx pin) to the bus (LIN pin), and the receiver provides the data on the bus to the controller (Rx pin). The transceiver conforms to the LIN 2.1 standard.

The LIN transceiver has a timeout watchdog for Tx. After the timeout, the LIN bus will be released to the recessive state from the dominant state.

The bus driver has an in-built short-circuit current limitation facility to protect the device from damage when there is a short between the bus and the supply. In addition to the data receiver, there is a low-power receiver active in the device standby mode which received a wake-up event from the LIN bus to bring the device to normal mode.

7.4 Temperature Monitor/Limiter

The temperature limiter circuit powers down the device when the junction temperature exceeds 170°C (nominal). It also issues an over-temperature warning at 160°C (nominal). The device is powered up again when the junction temperature falls below 140°C (nominal). The over-temperature warning flag is also cleared at this temperature.

The temperature limiter circuit can be optionally disabled through SPI.

7.5 VSUP Under-voltage Reset

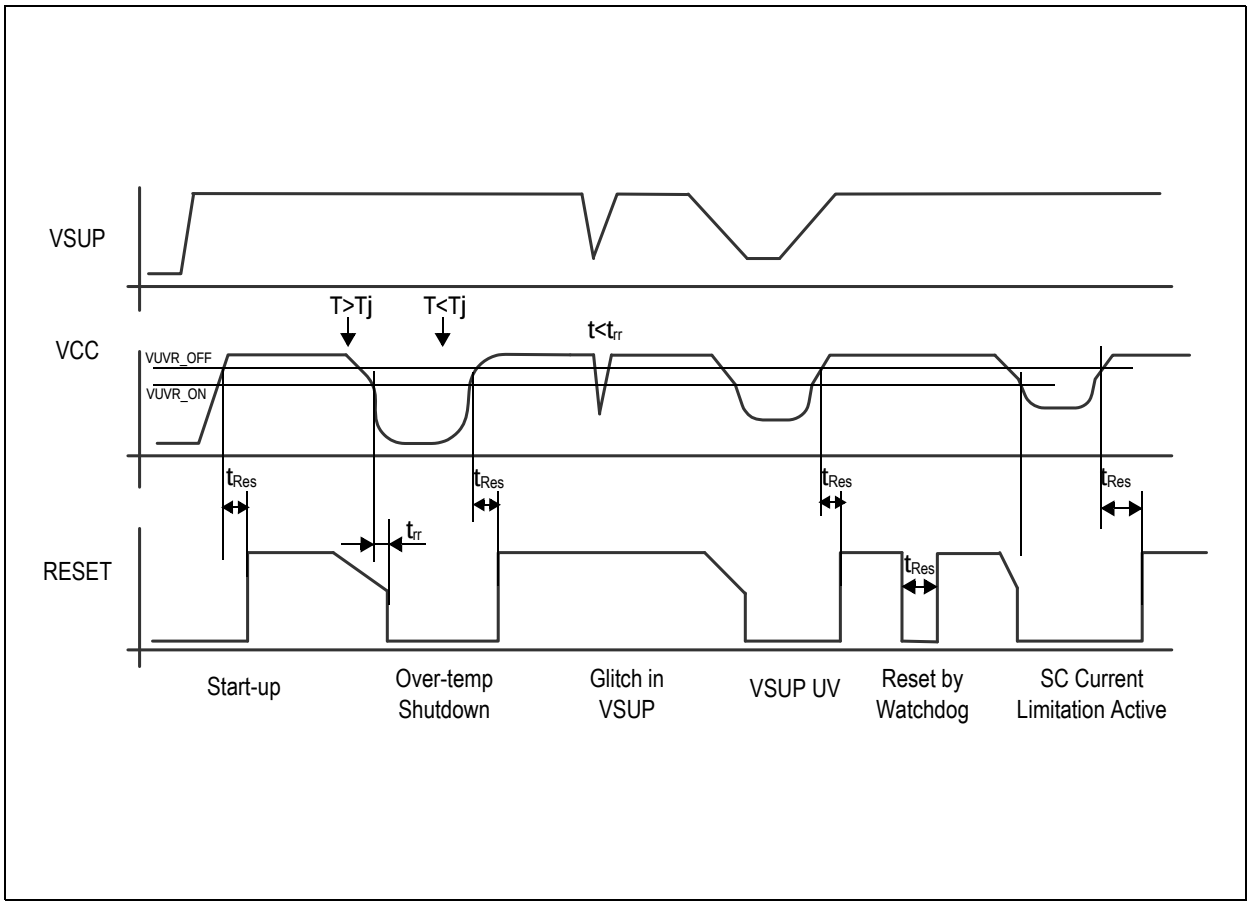
When VSUP drops below VSUVR_ON, the RESET_VSUP_N switches back to low level. This is treated as a master reset and will have the highest priority over all other signals. In this case, the regulators, LIN transceiver, and all other blocks are shut off, and the device comes to a complete stop. The device returns to the normal mode when VSUP rises over VSUVR_OFF again irrespective of the mode it was in prior to this under-voltage condition.

7.6 Reset

RESET module generates an active-low reset signal for the external circuitry supplied by VCC. The behavior of the reset output is depicted in Figure 4 in different cases. As shown, RESET signal is affected by an under-voltage condition on VCC and Watchdogs which are described in detail in the subsequent sections.

The reset period can be one-time programmed to 4, 16 and 32 ms with a default value of 8 ms.

Figure 4. Reset Functionality



7.7 VCC Under-voltage Reset

When VCC drops below VUVR_ON, the RESET_VCC_N switches back to low level. This event generates a reset output. The reset output is released again only a reset period (t_{Res}) later after VCC rises above VUVR_OFF. If the time difference between the VCC falling below VUVR_ON and rising above VUVR_OFF is less than t_{rr}, there will be no reset output. The reset output is affected in the conditions like over-temperature shutdown and temporary shutdown only through VCC under voltage.

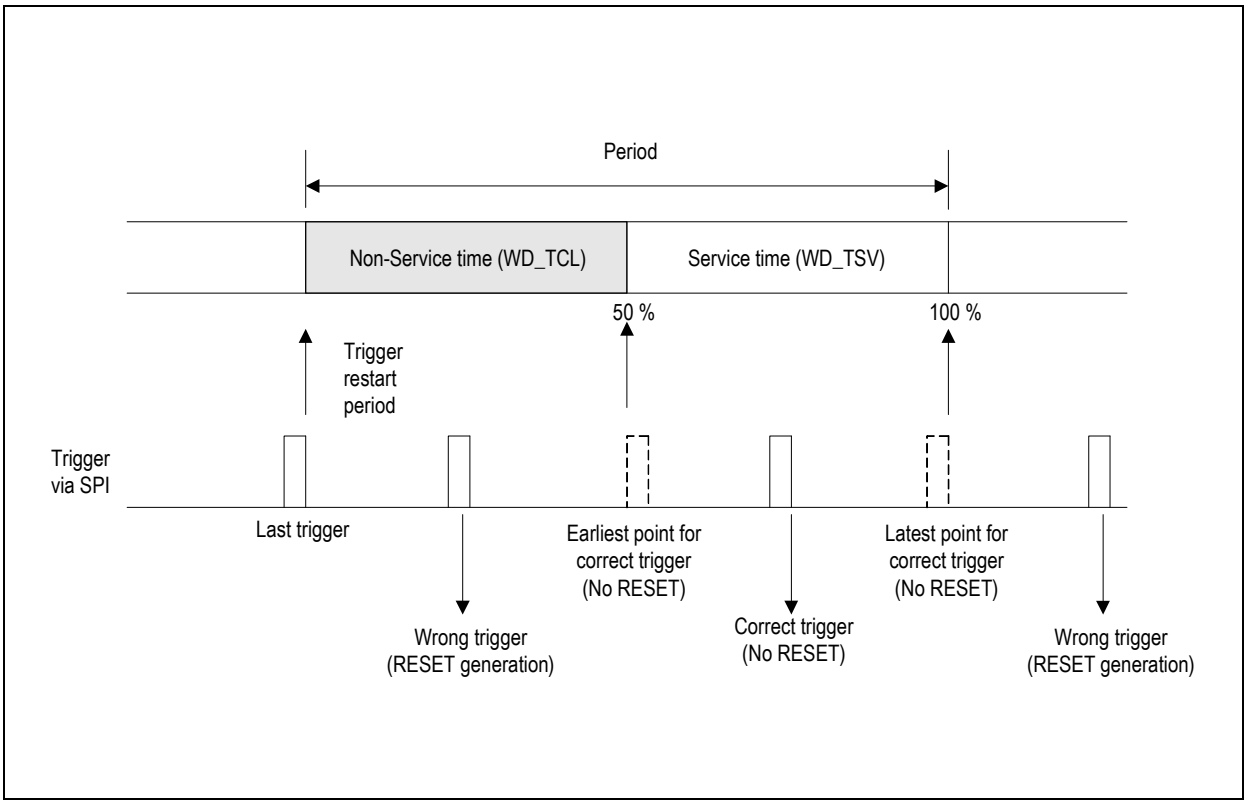
VCC under-voltage reset thresholds (VUVR_ON and VUVR_OFF) can be chosen by OTP.

7.8 Window Watchdog (WWD)

The Window Watchdog ensures that the Microcontroller is properly functioning in the normal mode of the device. The Watchdog is started after a reset and the Microcontroller needs to send a trigger in the window of WD_TSV (service time). If the trigger occurs early, in the period WD_TCL, or after WD_TSV, a reset output is generated.

The Microcontroller can access the trigger bit for the watchdog through SPI. The WWD can be enabled and the window times can be programmed through OTP bits and enabled as a factory option.

Figure 5. Window Watchdog Functionality



7.9 Timeout Watchdog (TWD)

The Timeout Watchdog ensures that the Microcontroller is in proper functional state in the device standby mode. The Watchdog timer will be started upon a rising edge on INT and will generate a reset output if the Microcontroller doesn't send a trigger before the timeout.

The Microcontroller can access the trigger bit for the watchdog through SPI. The TWD can be enabled by OTP and the timeout interval can be programmed through SPI.

7.10 Modes of Operation

The AS8515 *Top die* provides the following four main operating modes:

- Normal Mode
- Standby Mode
- Temporary Shutdown Mode
- Thermal Shutdown Mode

The LIN transceiver can be programmed to operate with lower slew in the normal mode. See Figure 6 for a detailed state transition diagram. Soft states like “TxWD Wait”, “Standby Wait”, and other wait states have also been included in the state diagram for completeness.

Figure 6. Finite State Machine Model of AS8515 Top Die

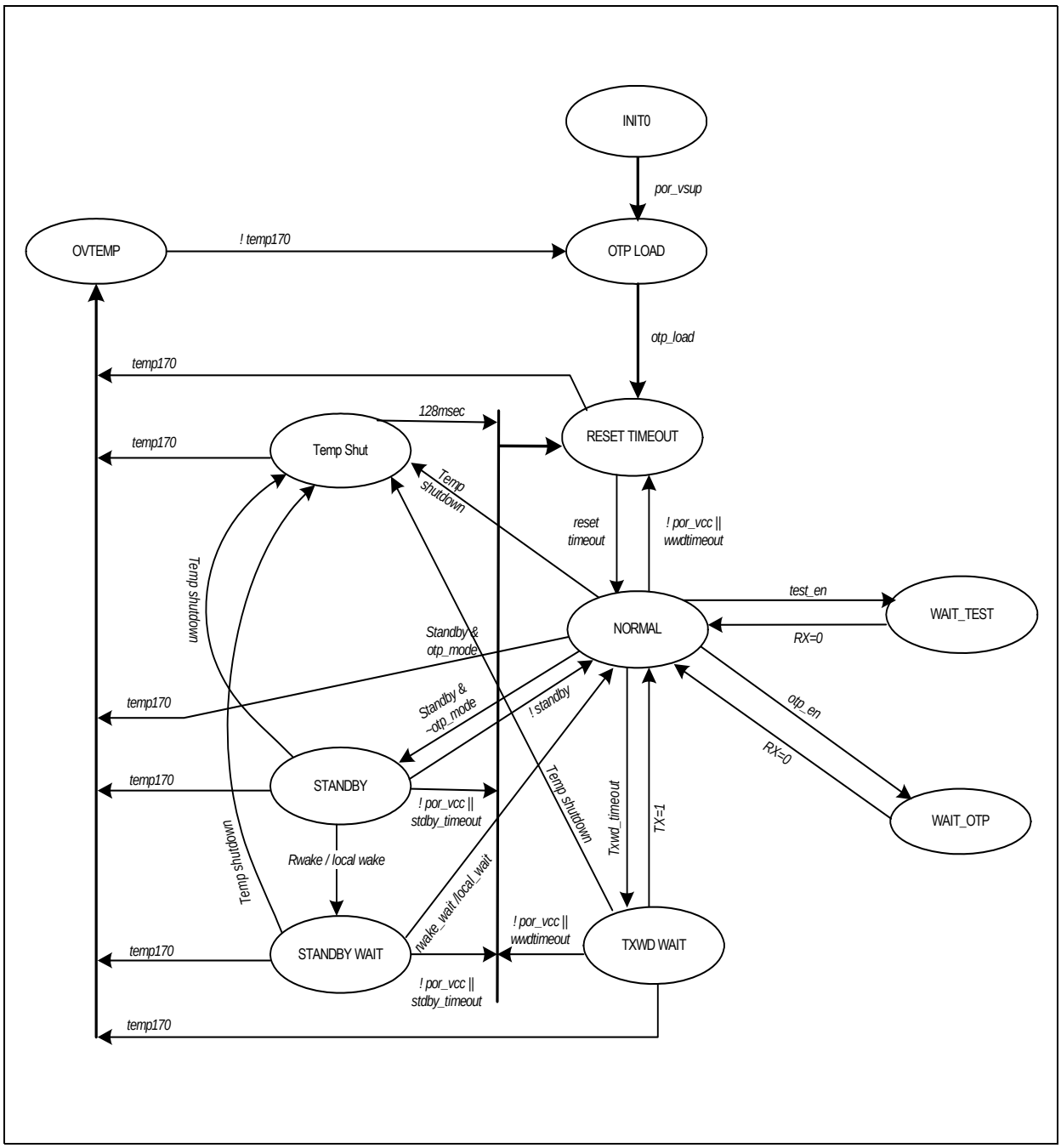


Table 15. Transition Table

Transition		Interface				Reg. 0x05 D0	Flags				Comments
From Mode	To Mode	LIN	Rx	Tx	EN		Rwake	U_{VSENSE}	OT	U_{VCC}	
Normal Mode	Stand-By	X-RS	X-H[1]	H[2]	H-L[2]	L	X	X	inactive	inactive	Tx is high for $T_{STNDY\_trigger}$
	Temporary Shutdown	X-RS	X-H[1]	X	H	H[2]	X	X	inactive	set	The Control Bit is set through the 4-Wire SPI interface
	Over-Temperature	X-RS	X-H[1]	X	X	L	X	X	set	set	Temperature monitor output asserted (covered by scan)
Standby Mode	Normal (LW)	X	H-X[1]	X	L-H[2]	L	X	X	inactive	inactive	
	Normal (RW)	X	H-X[1]	H	X	L	set	X	inactive	inactive	Remote Wake up Event occurred on LIN
	Temporary Shutdown	RS	H[1]	H	L	H[2]	X	X	inactive	set	The Control bit is set through the 4-Wire SPI interface
	Over-Temperature	RS	H[1]	H	L	L	X	X	set	set	Temperature monitor output asserted (covered by scan)
Temporary Shutdown Mode	Normal	RS-X	H-X[1]	X	X	L	X	X	inactive	clear	Internal 128ms timer expired
Over-temperature Mode	Normal	RS-X	H-X[1]	X	X	L	X	X	clear	clear	Temperature monitor output de-asserted (covered by scan)
All States	Power Off	X	X	X	X	X	X	L-H[2]	X	X	

1. Effect of transition
2. Cause for transition

Note: L = Low state, H = High state, OT = Over temperature Reset, U_{VCC} = Under-voltage VCC, U_{VSENSE} = Under-voltage VSENSE, Rwake = Remote wake, X = don't care.

7.10.1 Normal Mode

This is the mode after the power-up. In this mode, voltage regulator, LIN transceiver, window Watchdog is all active. The resistive divider can be enabled through SPI. LIN transceiver is capable of sending the Tx data from microcontroller to the LIN bus at a maximum rate of 20Kbps.

7.10.2 Standby Mode

Standby Mode is a functional low power mode and is entered by pulling EN to ground. The LIN transceiver, resistive divider, window watchdog, and Tx timeout watchdog circuits are disabled. But, it is possible to selectively enable the voltage and current measurement paths in this mode using an externally generated measurement enable (MEN) signal on the MEN pin. The timeout Watchdog can be enabled in this mode to make sure that the Microcontroller is active.

7.10.3 Temporary Shutdown Mode

In this mode, the regulator is powered down and the VCC is pulled down. This provides an alternative way to reset those components powered by AS8515. The feature has to be enabled by an OTP bit (factory programming option) and can be invoked through SPI. The LIN transceiver along with the LIN wake-up circuits are powered down. No remote wake functionality possible. LIN bus enters into recessive state. The system goes out of this mode to normal mode after the timeout of an internal timer.

7.10.4 Thermal Shutdown Mode

If the junction temperature T_J is higher than T_{sd}, the device will be switched into the thermal shutdown mode. The regulator and the transceiver are completely disabled. Only the over-temperature monitor is active. As soon as the temperature returns back to T_{RET}, the system enters normal mode.

7.11 Initialization

When the power supply is switched on, when VSUP > VSUVR_OFF, RESET_VSUP_N becomes high. This starts the regulator LDO with 3.3V and Vuvr_off option of 2.75V. When VCC > Vuvr_off (2.75V), active-low PORN_2_OTP is generated. The rising edge of PORN_2_OTP loads contents of fuse onto the OTP latch after load access time T_{Load}. LOAD_OTP_IN_PREREG signal loads contents of OTP latch onto a register. This register provides the actual settings of LDO, Vuvr_off and Reset Timeout period T_{Res}. This is done as the OTP block is powered by the VCC. If VCC > Vuvr_off (phase 2), Reset timeout is restarted. RESET signal is de-asserted after Reset Timeout period T_{Res} (phase 2) and then device enters into normal mode. The circuit also needs to initialize correctly for very slow ramp rates on VSUP (of the order of 0.5V/min).

Figure 7. Initialization Sequence

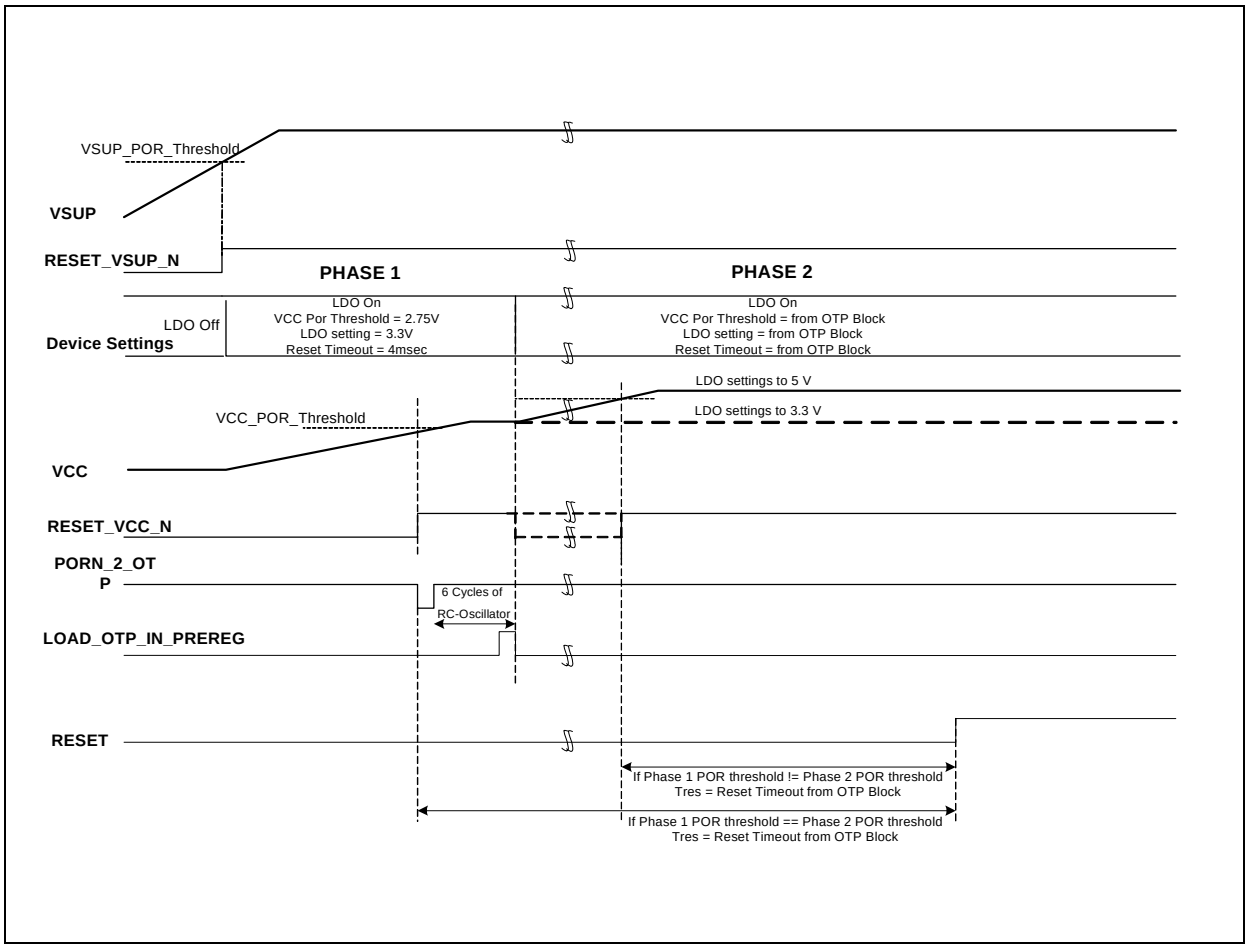


Table 16. VSUP>Vsuvr_on and VCC<Vuvr_on

Block	Output Signal
TRANSCEIVER=Enabled (disabled only during initial VSUP ramp-up)	LIN=high-z, Rx=follows VCC…
LDO=Enabled (disabled only during initial ramp-up)	VCC=low…
RESET BLOCK=Enabled	RESET=high-z…
RESISTIVE DIVIDER=Enabled	VSENSE=high…, VSENSE_DIV=enabled

Table 17. VSUP<Vsuvr_on

Block	Output Signal
TRANSCEIVER=Disabled	LIN=high-z, Rx=high-z…
LDO=Disabled	VCC=low
RESET BLOCK=Disabled	RESET=high-z
RESISTIVE DIVIDER=Disabled	VSENSE=high, VSENSE_DIV=low

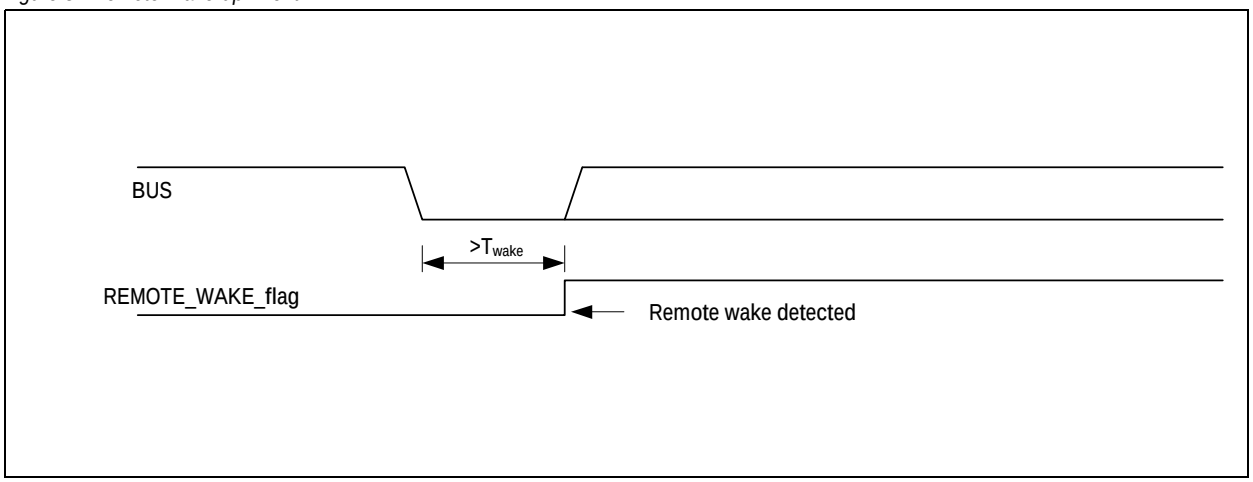
7.12 Wake-up

When the device enters standby mode, it can be brought back to the normal mode. A dominant state on the BUS for duration of t_{WAKE} (see Table 22) will result in the device wake-up which is termed as remote wake.

7.12.1 Remote Wake-up Event

In all low power modes of *Top die*, low power BUS receiver is ON. If BUS is in dominant state for longer than t_{WAKE} then, remote wake is sensed on the BUS and REMOTE_WAKE_flag is set. Indication of wake-up is given to µC by setting a bit in interrupt register and giving interrupt on INTN pin.

Figure 8. Remote Wake-up Event



7.13 LIN BUS Transceiver

The AS8515 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller. The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a de-bouncing unit.

7.13.1 Transmit Mode

During transmission the data at the pin Tx will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:

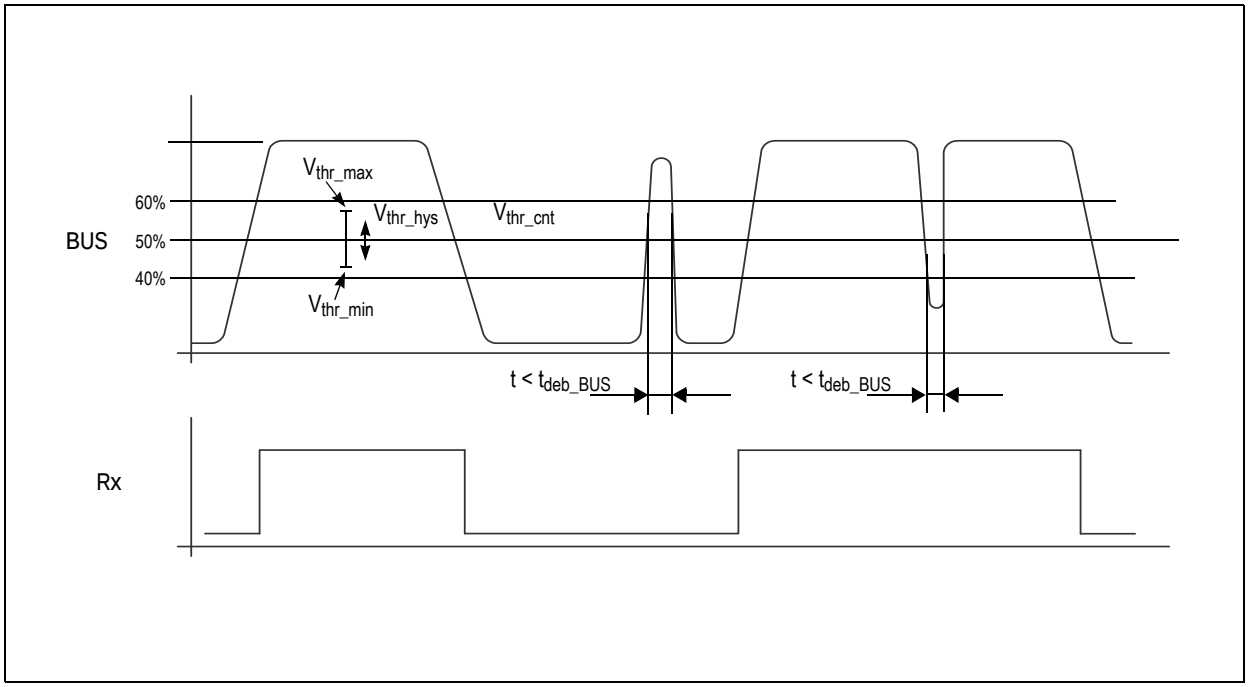
- Thermal Shutdown active
- Master Reset (VSUP < Vsuvr_on)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS (VBUS>VSUP). No additional termination resistor is necessary to use the AS8515 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VSENSE.

7.13.2 Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin Rx. Short spikes on the bus signal are suppressed by the implemented debouncing circuit. Including all tolerances the LIN specific receive threshold values of 0.4*VSUP and 0.6*VSUP will be securely observed.

Figure 9. Receive Mode Impulse Diagram

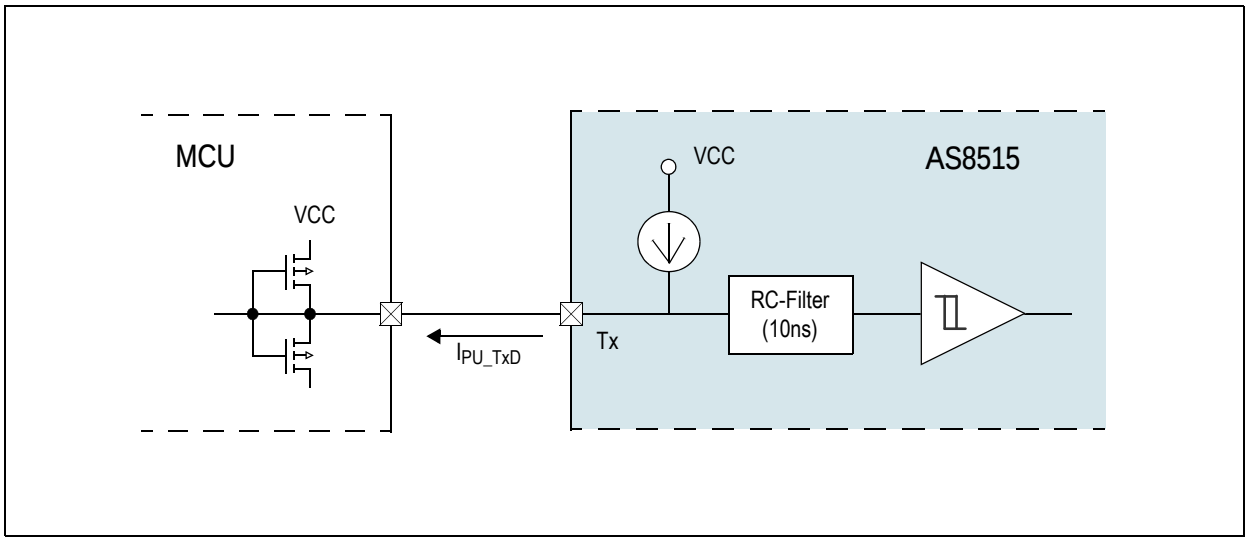


7.14 Rx and Tx Interface

7.14.1 Input Tx

The 3.3V input Tx controls directly the BUS level. LIN Transmitter acts like a slew-controlled level shifter. A dominant state (low) on Tx leads to the LIN bus being pulled low (dominant state) too. The Tx pin has an internal active pull up connected to VCC. This guarantees that an open Tx pin generates a recessive BUS level.

Figure 10. Tx Interface



7.14.2 Output Rx

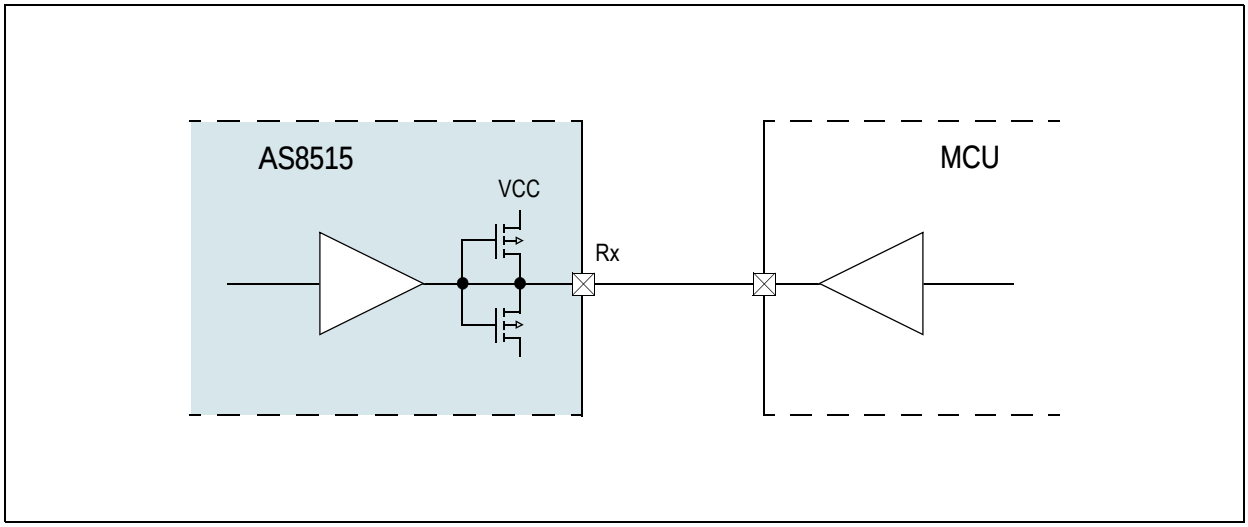
The received BUS signal will be output to the Rx pin:

BUS < Vthr_cnt – 0.5 * Vthr_hys → Rx = low

BUS > Vthr_cnt + 0.5 * Vthr_hys → Rx = high

This output is a push-pull driver between VCC and GND with an output current of 1mA

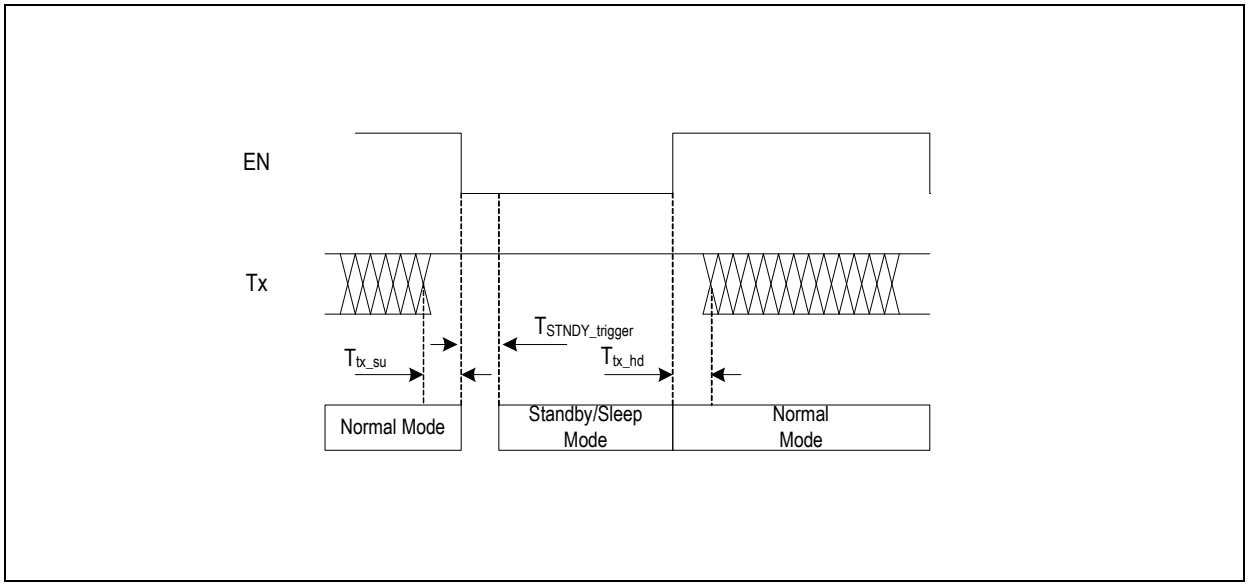
Figure 11. Rx Interface



7.15 MODE Input EN

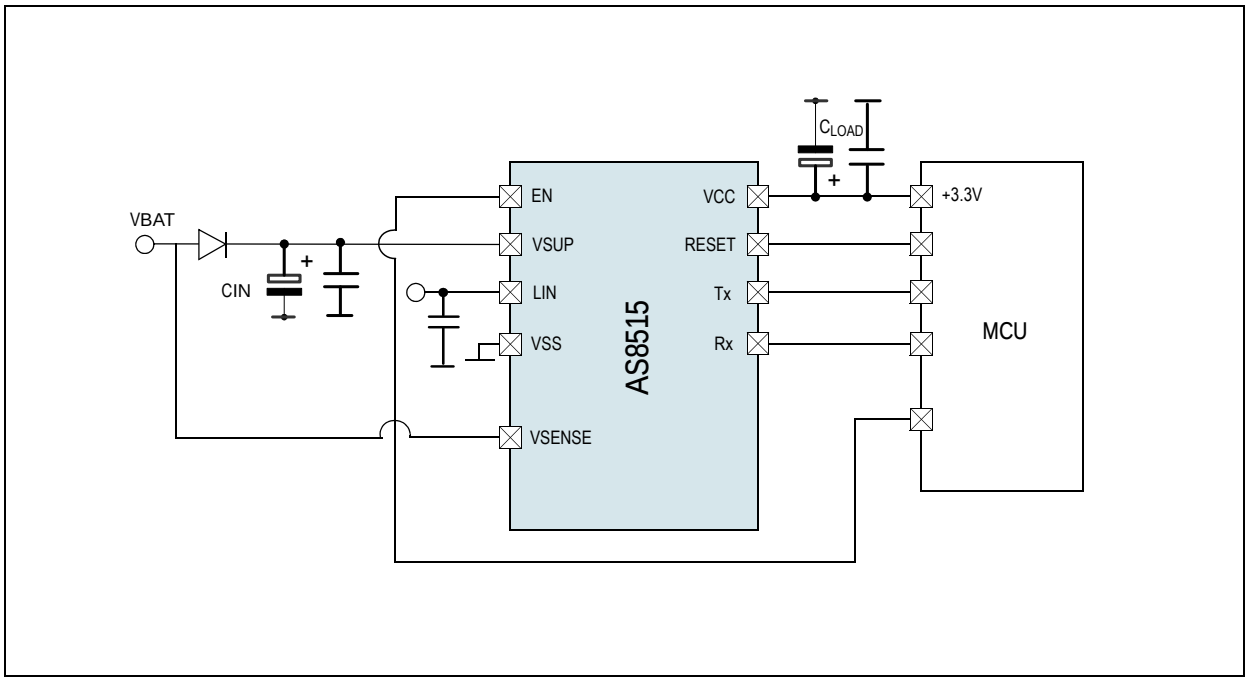
The AS8515 *Top die* is switched from normal mode to the standby mode with a falling edge on EN and keeping Tx high for $T_{STNDY\_trigger}$ time. Device is switched from standby mode to normal mode with a rising edge at the EN pin. The mode change for *Top die* with a falling edge on EN can be done independently from the state of the transceiver bus. This ensures the direct control of device to enter into standby mode by microcontroller using EN pin.

Figure 12. EN Pin Functionality



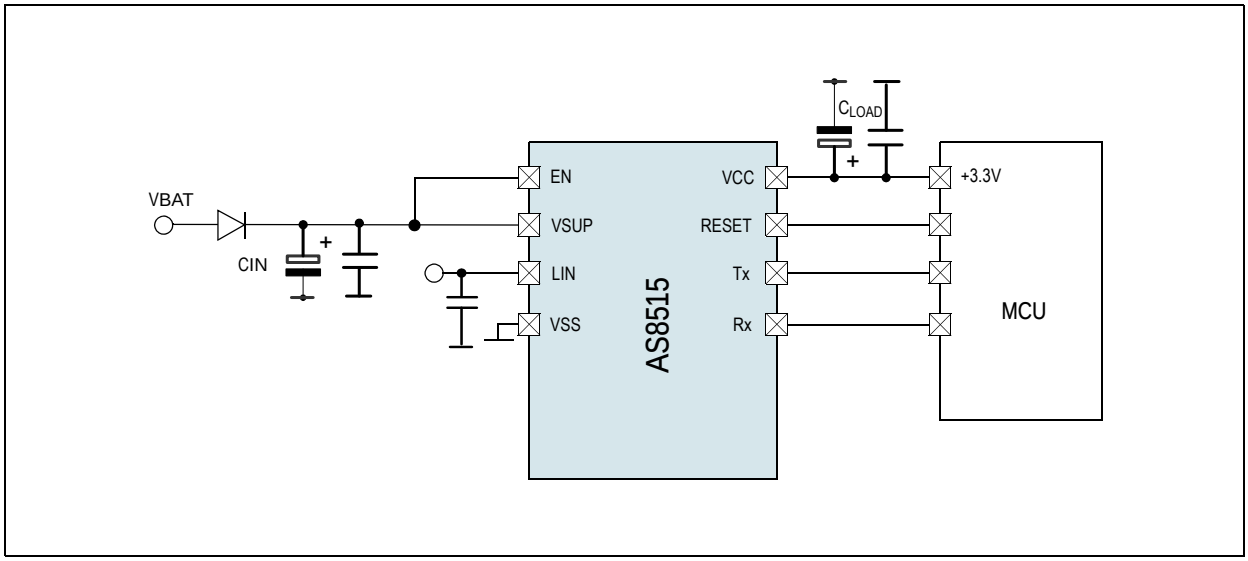
The EN input has an internal active pull down to secure that if this pin is not connected, a low level will be generated.

Figure 13. Enable Interface



If the application doesn't need the low-power modes of the device, a direct connection of EN to VCC is possible. In this case the *Top die* operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via VSUP signal as shown below.

Figure 14. EN Connection for Permanent Normal Mode



7.16 Top Die Block Specifications

This section provides specification of design related key parameters.

7.16.1 Voltage Attenuator

Table 18. Voltage Attenuator

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RDIV	Division ratio			21		V/V
VSENSE	Input voltage range/ Battery voltage range		4.5	12	18	V
$\varepsilon_{p,RDIV}$	Ratio error	At room temperature, VSENSE=12V			±1	%
$\varepsilon_{dt1,RDIV}$	Ratio drift (with reference to Temperature)	Temperature: -25 to +65° @VSENSE=12V Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.05		%
$\varepsilon_{dt2,RDIV}$		Temperature: -40 to +125° @VSENSE=12V Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.2		
$\varepsilon_{dv1,RDIV}$	Ratio drift (with reference to VSENSE)	VSENSE: 11V to 13V @Temperature=27° Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.05		%
$\varepsilon_{dv2,RDIV}$		VSENSE: 6V to 18V @Temperature=27° Maximum values will be added after device evaluation (to be guaranteed by evaluation)		±0.2		

7.16.2 Voltage Regulator (LDO)

Table 19. Voltage Regulator

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SUP}	Input Supply Voltage		4.3	12	18	V
VCC	Output Voltage Range		3.15	3.3	3.45	V
I_{LOAD}	LDO Load Current				45	mA
ICC_SH	Output Short Circuit Current	Normal mode			250	mA
dVCC1	Line Regulation	ΔVCC / ΔVSUP for VSUP range			8	mV/V
LOREG	Load Regulation	ΔVCC / ΔICCn (0.5mA < I_{LOAD} < 50mA)			1	mV/mA
CL1	Output Capacitor 1 LDO	Electrolytic	2.2		10	µF
ESR1			1		10	Ω
CL2	Output Capacitor 2 LDO	Ceramic	100		220	nF
ESR2			0.02		1	W
CSUP1E	Input capacitor (Electrolytic)	For EMC suppression	22		100	µF
ESR1_CSUP			1		10	Ω
CSUP2C	Input capacitor (Ceramic)		100		220	nF
ESR2_CSUP			0.02		1	Ω

7.16.3 LIN Transceiver

DC Electrical Characteristics.

Table 20. Driver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{bus_lim}		Current limitation in dominant state LIN = VSUP_max	40	120	200	mA
LIN_V_{OL}		Output Voltage BUS (dominant state), I_{LIN} = 40mA (short-circuit condition tested at V_{OL}=2.5V)			2	V
Pull-up resistor		Normal mode (recessive BUS level on Tx pin)	20	40	60	KΩ
$I_{bus\_leak\_rec}$		Driver OFF; 7.3V < VSUP < 18; 8V < V_{BAT} < 18, VSUP < VBUS < 1.08 * VSUP (to be tested at VBUS = 18V)			20	µA

Table 21. Receiver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{bus\_leak\_dom}$		Input Leakage current at receiver Driver OFF; VBUS = 0V; VSUP = 12V; VCC = 3.3V	-1			mA
$I_{bus\_no\_GND}$		VSS = VSUP; VSUP = 12V; 0V < VBUS < 18V, VCC = 3.3V (to be tested at VBUS = 18V)	-1		1	mA
$I_{bus\_no\_bat}$		VSUP = VSS; 0V < VBUS < 18V, VCC = VSS (to be tested at VBUS = 18V)			100	µA
V_{bus_dom}					0.4	VSUP
V_{bus_rec}			0.6			VSUP

Table 21. Receiver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{bus_cnt}		$V_{bus\_cnt} = (V_{th\_dom} + V_{th\_rec})/2$ [1]	0.475		0.525	VSUP
V_{hys}		$V_{hys} = (V_{th\_dom} - V_{th\_rec})$ [1]	0.05		0.175	VSUP

1. V_{th_dom} : Receiver threshold of the recessive to dominant LIN bus edge
   V_{th_rec} : Receiver threshold of the dominant to recessive LIN bus edge

AC Electrical Characteristics.

LIN Driver, Bus load conditions (C_{BUS} ; R_{BUS}): 1nF; 1kΩ / 6, 8nF; 660Ω / 10nF; 500Ω

Table 22. LIN Driver

Symbol	Parameter	Condition	Min	Typ	Max	Unit
D1	(worst case 20Kbps transmission)	V_{th_rec}(max) = 0.744 x VSUP; V_{th_dom}(max) = 0.581 x VSUP; VSUP = 6.0V...18V; tbit = 50µs; D1 = tbus_rec(min) / (2 x tbit)	0.396			
D2	(worst case 20kbps transmission)	V_{th_rec} (min) = 0.422 x VSUP; V_{th_dom} (min) = 0.284 x VSUP; VSUP = 6V...18V; tbit = 50µs; D2 = tbus_rec(max) / (2 x tbit)			0.581	
D3	(worst case 10.4kbps transmission)	V_{th_rec} (max) = 0.778 x VSUP; V_{th_dom} (max) = 0.616 x VSUP; VSUP = 6.0V...18V; tbit = 96µs; D3 = tbus_rec(min) / (2 x tbit)	0.417			
D4	(worst case 10.4kbps transmission)	V_{th_rec} (min) = 0.389 x VSUP; V_{th_dom} (min) = 0.251 x VSUP; VSUP = 6V...18V; tbit = 96µs; D4 = tbus_rec(max) / (2 x tbit)			0.59	
t_{dLR}		VCC = 3.3V; Propagation delay bus dominant to Rx LOW			6	µs
t_{dHR}		VCC = 3.3V; Propagation delay bus dominant to Rx HIGH			6	µs
t_{RS}		Receiver delay symmetry	-2		2	µs
t_{WAKE}		Dominant time for wake-up via LIN bus	30		150	µs
t_{sln}		Transition from standby mode to normal mode (clock frequency is 128KHz ±25%)		4		Clock cycles
t_{nsl}		Transition from normal mode to standby mode (clock frequency is 128KHz ±25%)		6		Clock cycles
t_{rec_deb}		Receiver de-bounce time	0.6		3	µs
C_{int}		Internal capacitance of the LIN node configured as a slave with a 180pF cap on the LIN bus		220	250	pF

7.17 Timing Diagrams

Figure 15. Timing Diagram for Propagation Delays

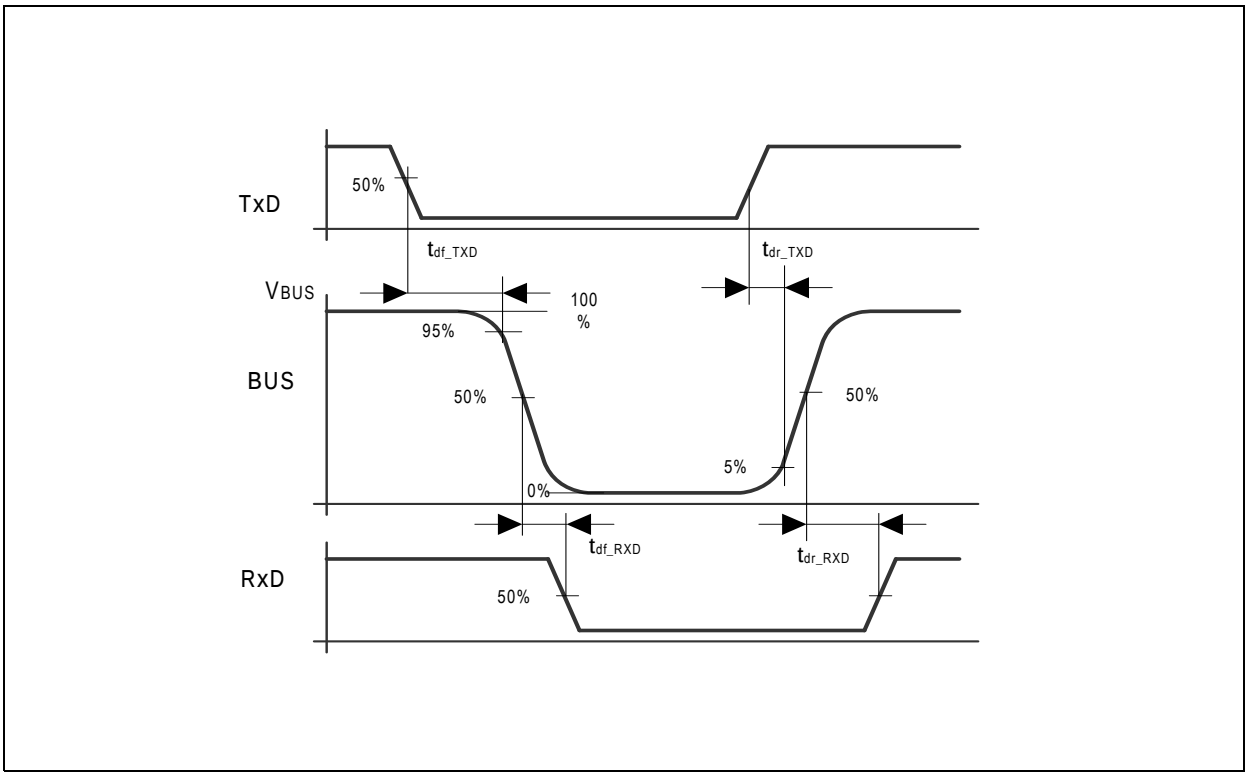
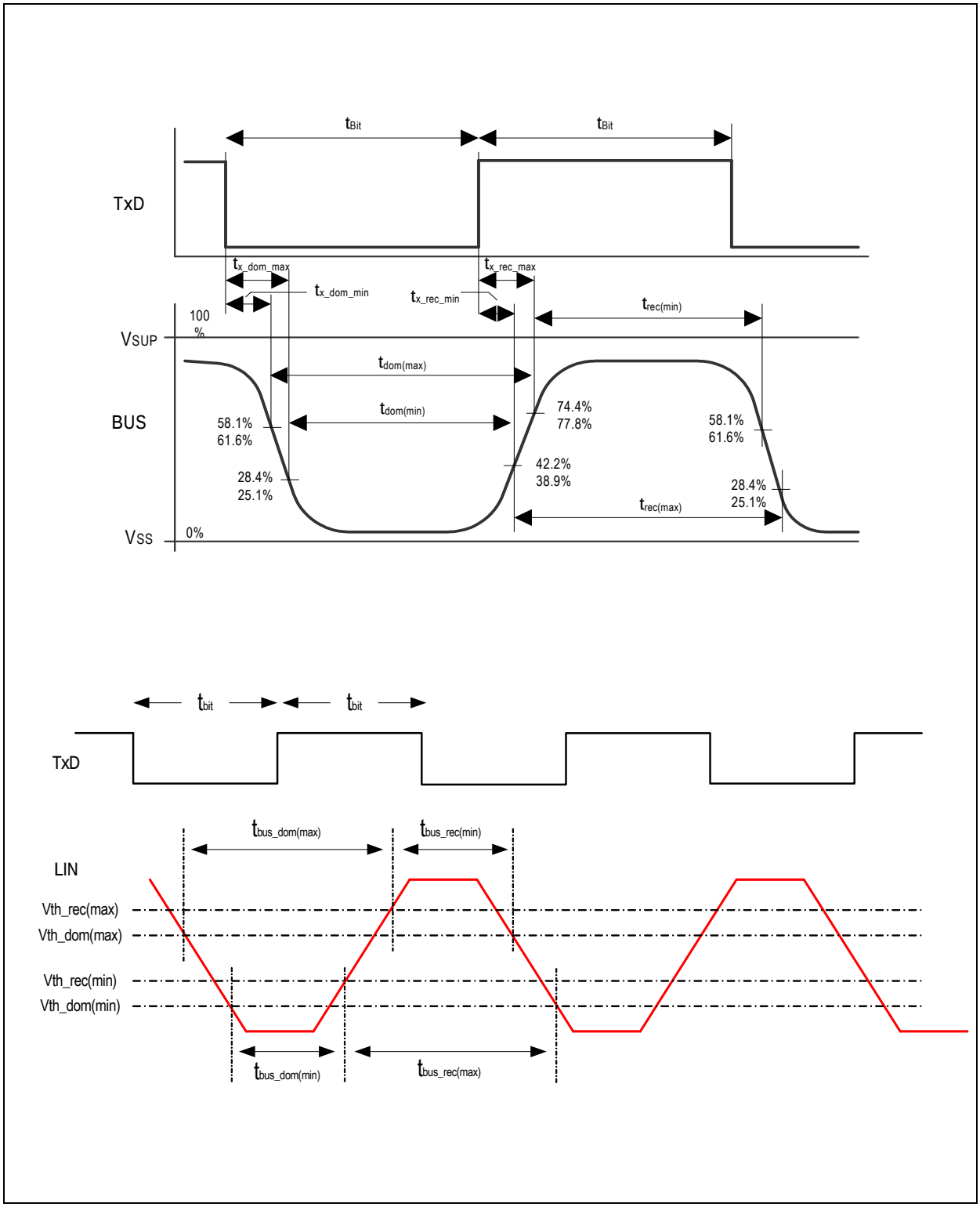


Figure 16. Timing Diagram for Duty Cycle According to LIN 2.1 and J2602



7.17.1 Tx Timeout Watchdog

Table 23. Tx Timeout Watchdog

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{lin_wdog}	Timeout period for the dominant state		0.5	1	2	s

7.17.2 Temperature Limiter

Table 24. Temperature Limiter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sd}	Shut down temperature	Junction temperature	155	170	185	°C
T_{otset}	Over-temperature warning		142	157	172	°C
T_{ret}	Return temperature		125	140	155	°C

7.18 Top Die Registers

The serial interface can be used for communication between AS8515 and an external microcontroller. The device is only a slave and the microcontroller has to initiate the communication. The device can be configured by writing into the control registers and the diagnostic information can be read out from the diagnostic registers. Pin CST is used as chip select for SPI communication.

A total of 32 registers, each of 8-bits which include configuration, diagnostic, and backup are available. The registers can be accessed using the 4-wire serial interface. Table 25 provides a description of all AS8515 *Top die* registers.

Table 25. AS8515 Top Die Registers

Address	Register Name	Default Value	R/W	Description
Configuration and Control Registers				
0x00	Reserved			
0x01	Reserved			
0x02	Reserved			
0x03	Device Configuration Register	On POR_VCC 0000_1100	R/W	D0 Reserved D1 Voltage Attenuator Enable Bit. 0 Disabled, 1 Enabled D2 Enable/Disable Over Temperature Monitor 0 Disabled, 1 Enabled D3 Enable/Disable LIN Transceiver 0 Disabled, 1 Enabled D4 Reserved D5-D7 Reserved
0x04	Device Control Register	On POR_VSUP 0000_0001	R/W	D0 High-slew / Low-slew control 1 High-slew, 0 Low-slew D1-D7 Reserved
0x05	Temporary Shutdown Register	On POR_VCC 0000_0000	R/W	D0 Temporary shutdown control bit 1 Enter temporary shutdown D1-D7 Reserved
0x06	Window Watch Dog Trigger Register	On POR_VCC 0000_0000	W	D0 Window Watchdog trigger bit D1 Timeout Watchdog trigger bit Upon a trigger, the bit will be cleared within 2 internal clock cycles. D2-D7 Reserved
0x07	Reserved			
0x0A	Reserved			
0x0B	Reserved			

Table 25. AS8515 Top Die Registers

Address	Register Name	Default Value	R/W	Description
0x0C	Reserved			
0x0D	Reserved			
0x0E	Watchdog Timer Control Register	On POR_VCC 0000_0000	R/W	D0 Timer resolution 0 1 second, 1 32 seconds D1-D7 Timeout period. If D0=1, then timeout period = D[7:1]*64*0.512 seconds, else timeout period = D[7:1]*0.512 seconds
0x0F	Reserved			
OTP Registers				
0x10 …… 0x17	OTP_BITS_REG[0:7] …….. OTP_BITS_REG_[55:63]	On POR_VSUP 0000_0000	R	8 OTP data registers These registers contain all the 64 OTP bits. It can be read by the MCU when needed. OTP_bits 0 – 63 OTP_BITS_REG[00:07] = OTP_BITS[00:07] OTP_BITS_REG[08:15] = OTP_BITS[08:15] OTP_BITS_REG[16:23] = OTP_BITS[16:23] OTP_BITS_REG[24:31] = OTP_BITS[24:31] OTP_BITS_REG[32:39] = OTP_BITS[32:39] OTP_BITS_REG[40:47] = OTP_BITS[40:47] OTP_BITS_REG[48:55] = OTP_BITS[48:55] OTP_BITS_REG[56:63] = OTP_BITS[56:63]
Diagnostic Registers				
0x08	Diagnostic Register-1	On POR_VSUP 0000_0011	R	D7-D0 = DR[7:0], 8-LSB bits of the 24-bit Diagnostic Register. D0 POR-VSUP Set when VSUP < Vsuvr_on, cleared after µC read D1 Under voltage VCC (UVVCC) Set when VCC < Vuvr_on, cleared after µC read D2 Over-temperature Reset (OTEMP170) Set when temp > T_{sd}, cleared after µC read D3 Over-temperature warning (OTEMP160) Set when temp > T_{otset}, cleared after µC read D4 Overvoltage VSENSE (OVVSENSE) Set when VSUP > Vovthh, cleared after µC read D5 Reserved D6 Remote wakeup (RWAKE) Set on remote wakeup event on LIN Bus, cleared after µC read D7 Set on failure of window Watchdog trigger, cleared after µC read
0x09	Diagnostic Register-2	On POR_VSUP 0000_0000	R	D7-D0 = DR[15:8], Next 8-LSB bits of the 24-bit Diagnostic Register. D0 Tx timeout of 1sec (TXTIMEOUT) Set on Tx low > 1sec, cleared after µC read D1 TEMPSHUT This bit is set on entering temporary shutdown state and cleared after µC read. D2 Set on failure of timeout Watchdog trigger, cleared after µC read D3 Load Dump Flag D7-D4 Reserved

8 AS8515 Bottom Die Overview

The AS8515 *Bottom die* consists of two independent high resolution 16-bit SD analog to digital conversion channels. The measurement path of these two channels integrates a programmable gain amplifier, chopper and de-chopper, sigma-delta modulator, decimator and a digital filter for simultaneous measurement of Current and Voltage/Temperature.

The two measurement channels, namely the Current and Voltage/Temperature measurement channels have identical data path.

The input signal is amplified in the Programmable Gain Amplifier (PGA) with any of the selected gains of 1, 5, 25, 40 and 100 facilitating measurement of a wide range of Current, voltage and temperature levels. Gain Settings for different input ranges and any associated restrictions are explained in the Table 27.

Offset in the measurement path is minimized with the use of a chopper and a de-chopper at appropriate stages in the data path. By default the chopper/de-chopper is ON in the measurement path. It may be disabled by programming the appropriate register.

The amplified input signal is converted into a single-bit pulse-density modulated stream by the Σ-Δ Modulator. A decimator acting as a low-pass filter filters out the quantization noise and generates 16-bit data corresponding to the input signal. The decimation ratios of 64, 128 may be selected in the first filter stage. For reducing data rate further, the second stage decimation can be used.

An optional FIR Filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems.

8.1 Current Measurement Channel

The voltage across a Shunt Resistor, connected in series with the Battery negative terminal, forms the input signal to the Current Measurement channel. RSHH and RSHL are the Current measurement input pins. Offset in the input signal is nullified with the use of a chopper and a de-chopper at appropriate stages in the data path. The programmable gain amplifier in the data path with programmable settings of 1, 5, 25, 40 and 100 enables measurement of current ranges from ±1A to ±1500A. The sampled input signal is converted into a single-bit pulse-density modulated stream by the Σ-Δ Modulator. A decimator acting as a low-pass filter filters out the quantization noise and generates 16-bit data equivalent to the input current signal. The programmable input sampling rate and the decimation ratio determine the output data rates. The data path can be programmed to provide 1Hz to 2 kHz rates in the various modes available. An optional FIR filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems.

After enabling the current measurement channel, the delay for the availability of the first sample is two conversion cycles.

8.2 Voltage/Temperature Measurement Channel

The other two parameters of the Battery for measurement are Voltage and its Temperature. The second channel accepts signals from four independent sources through a Multiplexer as listed below:

- An attenuator battery voltage obtained through internal resistor divider from *Top die*, (or)
- A signal from the external temperature sensor, (or)
- A signal from external reference, (or)
- A signal from the internal temperature sensor.

Apart from this difference in the multiplexing of four input signals, the rest of the data path is identical to the Current measurement channel. RSHH and RSHL are the Current measurement input pins.

The Battery Voltage which can go up to 18V is attenuated through a Resistor Divider externally and is applied to the Voltage Channel. For Automotive Battery measurement, the Gain of the PGA should be restricted to 5 and 25. The latency for the first result from the voltage measurement channel is two conversion cycles.

A second option on this measurement channel is to measure Temperature. Internally generated constant current is pumped through the Temperature Sensor with positive temperature coefficient, and, a high- precision resistor. The voltages across the sensor and the resistor form the inputs to the measurement channel one at a time. The difference between the two voltages which is independent of the magnitude of the current is used to determine the temperature accurately. The voltage across the sensor is applied between the ETS and VSS pins and, the voltage across the high-precision resistor is applied between ETR and VSS. External temperature measurement involves the acquisition of two signals one after the other using the same constant current source. The latency for the first result from the temperature measurement channel is two conversion cycles.

A third option on the measurement channel is to measure the internal temperature. Hence, one of the three options for measurement of Battery Voltage, External Temperature and, internal temperature may be carried out by selection of appropriate inputs through the internal multiplexer selection.

ETR and ETS inputs can optionally be used to measure other signal sources like external resistive attenuators for battery voltages different to 12V nominal.

ETR and ETS are single ended inputs and referenced to AVSS. Voltage drop on internal bond wire causes ~100 digits of offset with systematic temperature dependency of another 50 LSB's over temperature.

8.3 Digital Implementation of Measurement Path

Figure 17. Block Diagram of Digital Implementation

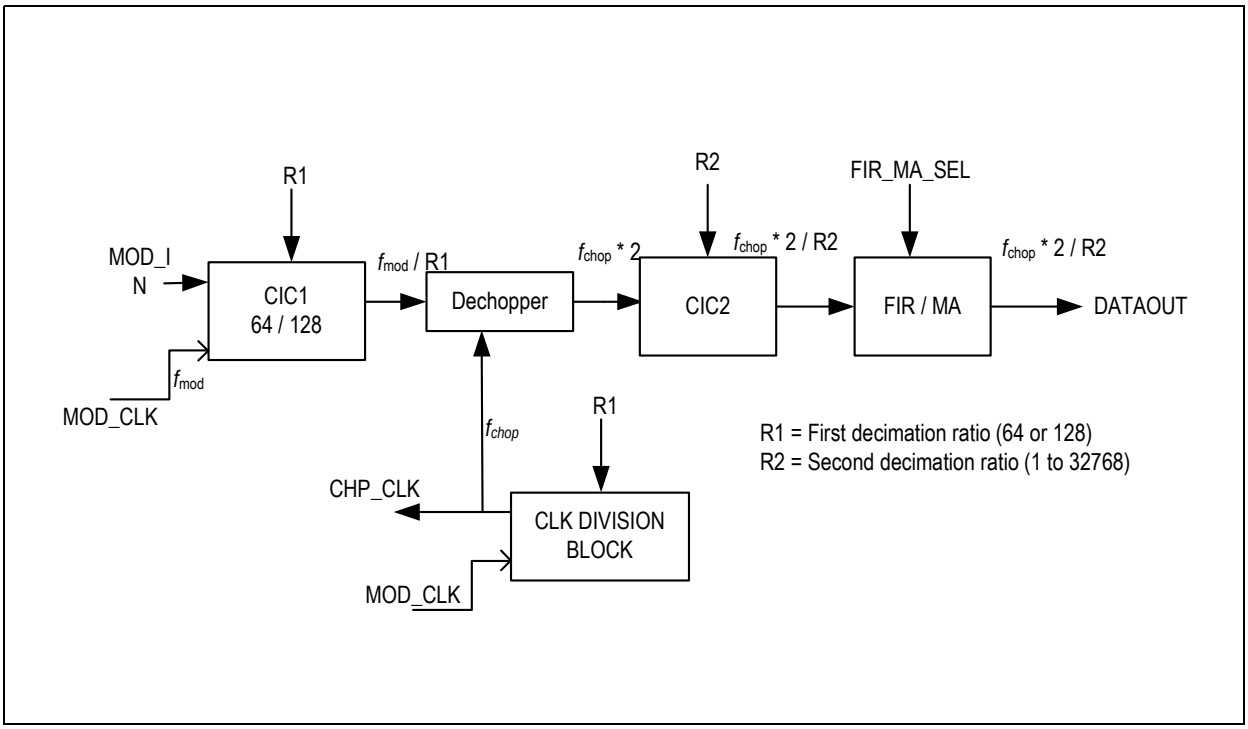


Figure 17 shows the digital implementation of the decimator and filter to process the 1-bit output of the Modulator. This block receives a 1-bit pulse density modulated output (MOD_IN) from the second order sigma delta modulator along with the oversampling frequency clock (MOD_CLK). The MOD_CLK directly goes to a clock division block, which generates chopper clock (CHOP_CLK). The CHOP_CLK can be one of 2kHz or 4kHz selected by Register CLK_REG in Table 46. The MOD_CLK can be either 1MHz or 2MHz. The Decimation is a two phase process. In the first phase, the R1 down sampling rate can be obtained by selecting either 64 or 128 in Registers DECREG_R1_I, DECREG_R1_V in Table 46. The 16-bit CIC1 output is dechopped with respect to CHOP_CLK. The output of Dechopper is passed through the CIC2 filter with a decimation ratio of 1to 32768 in steps of power of 2. This output is then processed through a FIR or Moving Average (MA) filter. FIR Filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems. MA filter is used to provide averaged output and the number of samples for averaging can be any integer value from 1 to 15.

8.4 Reference-Voltage

Band gap-reference voltage is used for the ADC as a reference and for the generation of the current for external temperature measurement.

8.5 Oscillators

A High-speed oscillator (HS) generates the oversampling clock. For internal state machine and Interrupt generation, a low-speed Oscillator (LS) is also available.

8.6 Power-On Reset

The AS8515 has PORs, APOR and DPOR on analog and digital power supplies respectively. On PORs of both supplies, initialization sequence happens and the system status is shown in state diagram (see Figure 18).

As shown in the state diagram, the system is in RESET state until DPOR output goes to logic HIGH and subsequently until APOR output goes to logic HIGH. Once analog power supply is available, the system goes into OTP_INT state and loads the default values into the control and data registers and goes into STOP state. If analog POR, APOR goes low at any time, the system goes into RESET state. In the STOP state, the AS8515 can be programmed and by giving start command it starts working following the state machine.

8.7 Modes of Operation

The device operates in four different modes, namely,

- Normal Mode 1 (NOM1)
- Normal Mode 2 (NOM2)
- Standby Mode 1 (SBM1)
- Standby Mode 2 (SBM2)

The Normal Modes are full-power modes with the exception that in Normal Mode 2, sampling is normally at a programmed lower frequency and is increased to a higher rate only when a measured input signal level crosses the programmed threshold in the current measurement channel.

The Standby Modes are lower power modes. Sampling is normally at a very low frequency interval. In Standby Mode 2, data sampling can be carried out only when the internal comparator detects the input current to be greater than the programmed threshold and it generates interrupt on the INT pin.

The device enters into the “Stop” state on Power On. This is a state where in the data path is inactive and can be entered into from any of the four Modes. The State transition Diagram involving the state of Stop and the four Modes is illustrated in the Figure 18.

Figure 18. Finite State Machine Model of AS8515 Bottom Die

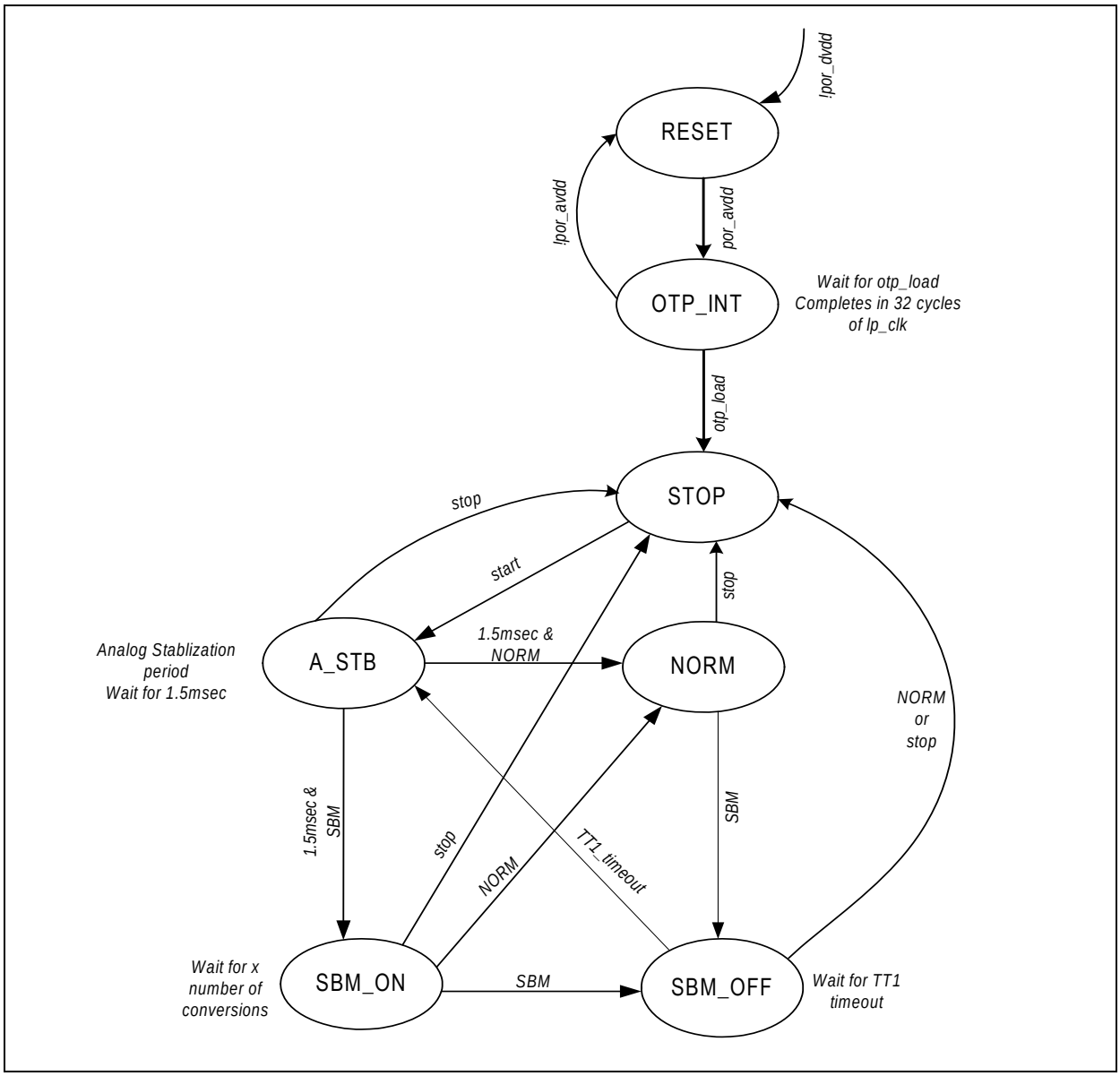


Figure Notes:

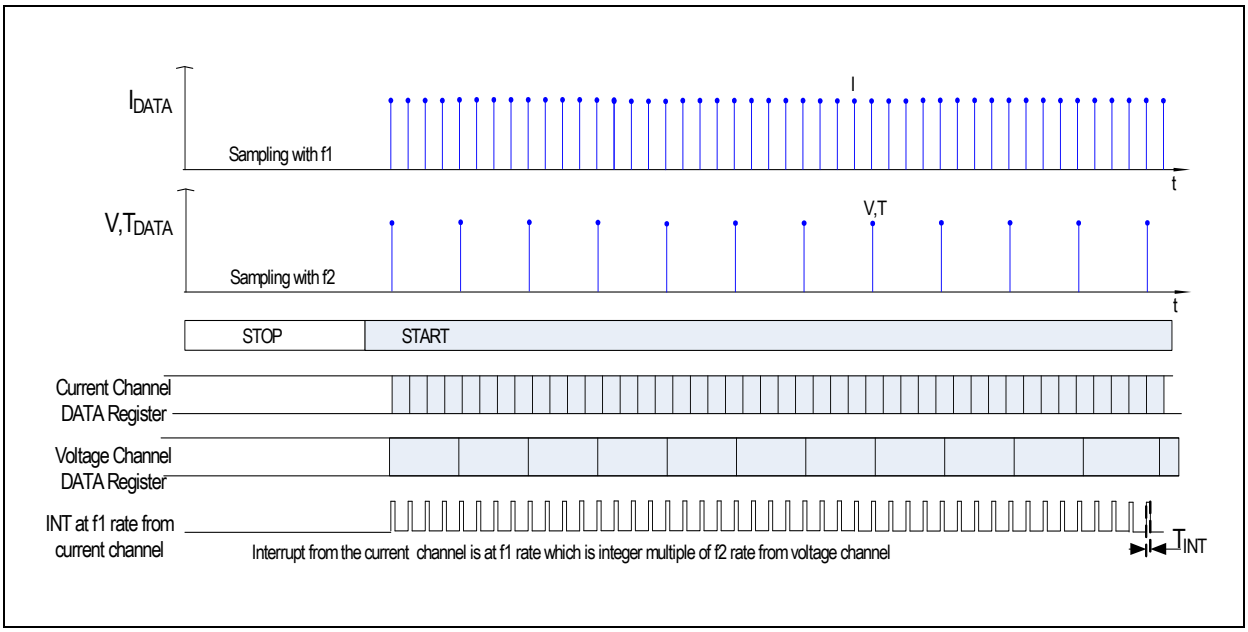
1. Device soft reset can be written in any of the following states STOP, A_STB, SBM_ON, SBM_OFF by writing “0” into D[7] of the RESET _REG (Address 0X09).
2. Measurement path of soft reset should be written in any the states, STOP, SBM_OFF by writing “0” into D[6] of the RESET _REG (Address 0X09).
3. When soft reset is used for the measurement path or for the device, external clock needs to be disabled if the system clock is external clock in the application.

8.7.1 Normal Mode 1 (NOM1)

On Power-on-reset of the device, AS8515 goes into STOP State.

Transition to Normal mode1 (NOM1) occurs when the “START BIT” D0 of Mode Control Register MOD_CTL_REG in Table 46 is set to “1” through the serial port SPI. Data Rate of voltage and current channels can be independently programmed and both the channels generate interrupts for every output available from ADC. The interrupt signal is generated on the INT pin. The width of the interrupt pulse is eight cycles of I_{p_clk}. The data is stable up to the next interrupt. If the data rate is different for the two channels, the interrupt rate would follow the higher rate among the two channels. Data update can be known by reading the status register. The functionality is explained in the waveform shown in Figure 19. When the device is configured to NORMAL Mode1 from any mode the configuration should be through the STOP state only.

Figure 19. Normal Mode 1

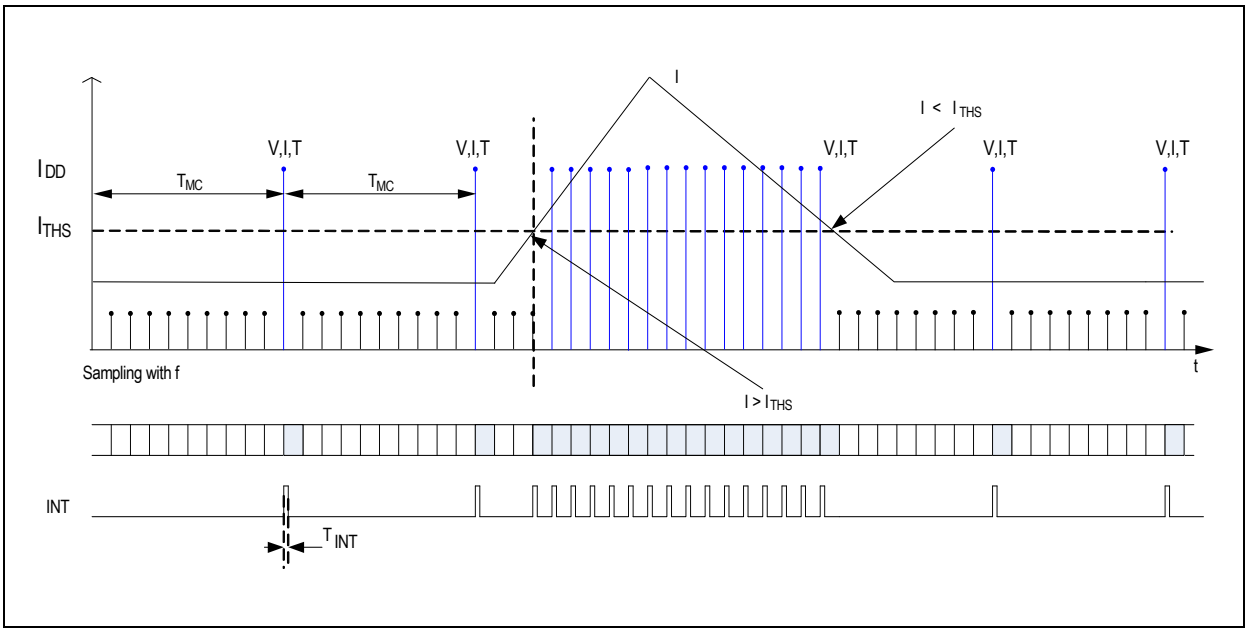


8.7.2 Normal Mode 2 (NOM2)

NOM2 differs from NOM1 in such a way that it allows for a relaxed data rate at a period of T_{MC} by programming the corresponding register as long as the amplitude of current is less than a programmed threshold I_{THC}. However, when, the measured input signal exceeds the programmed threshold, the data rate is changed to the rate of NOM1 mode.

Transition to NOM2 occurs when the “START BIT” D0 of Mode Control register MOD_CTL_REG in Table 46 is set to 1 and mode control bits to 01 through SPI. In this mode the data rate should be programmed with the time of T_{MC}. An interrupt signal is generated on INT at the rate of T_{MC} secs with a pulse width of eight cycles of I_{p_clk}. The data is stable up to the next interrupt. The data sample is compared against the programmed threshold and when it is exceeded, the data sampling rate is changed to provide data at the data rate of NOM1 mode. However, as soon as the data sample amplitude falls below the programmed threshold, the sampling rate is restored to provide data at the rate of T_{MC}. The functionality is illustrated in the waveform Figure 20.

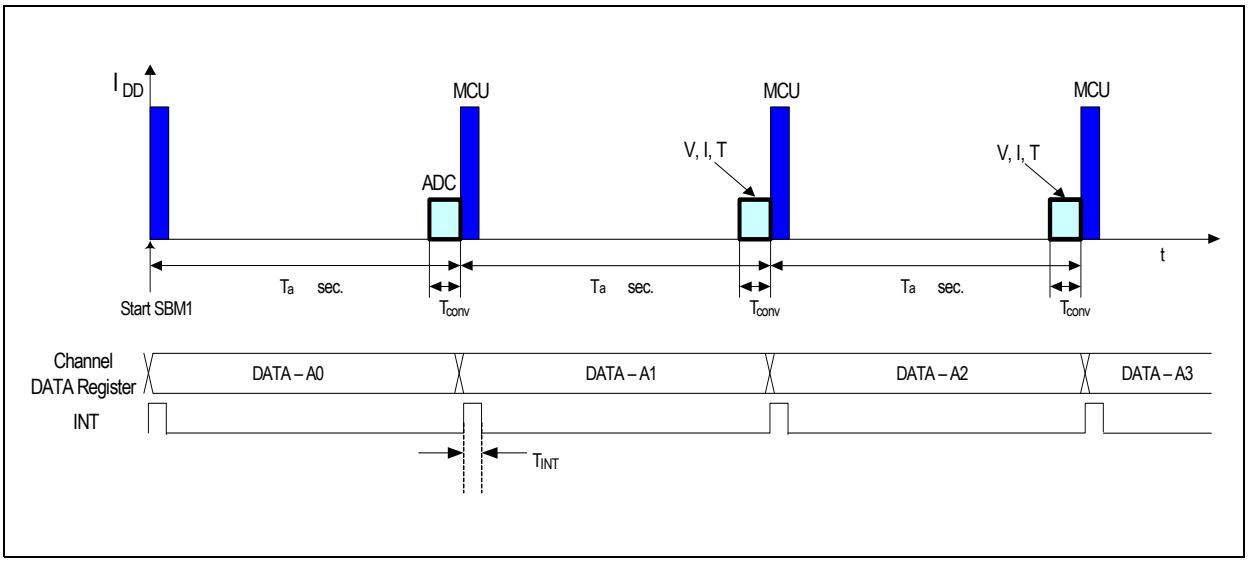
Figure 20. Normal Mode 2



8.7.3 Standby Mode1 (SBM1)

The low-power Standby Mode can be entered only through the STOP state. Transition to SBM1 mode occurs when the “START BIT” D0 of Mode Control register MOD_CTL_REG in Table 46 is set to “1” and Mode Control Bits to “10” through SPI. In this mode the date rate is programmable with the time of Ta. An interrupt signal is generated on INT at the rate of Ta seconds, and with a pulse width of eight cycles of I_{p_clk}. The data is stable up to the next interrupt. The functionality is illustrated in Figure. During the period of Ta, only one data sample is made available and, during the rest of the period, the device is maintained in STOP state to reduce power consumption. The microcontroller which receives the data on the Interrupt, is also expected to be processing the data for a short time as shown clearly in the Figure 21 to ensure the overall low-power consumption of the data acquisition and processing system.

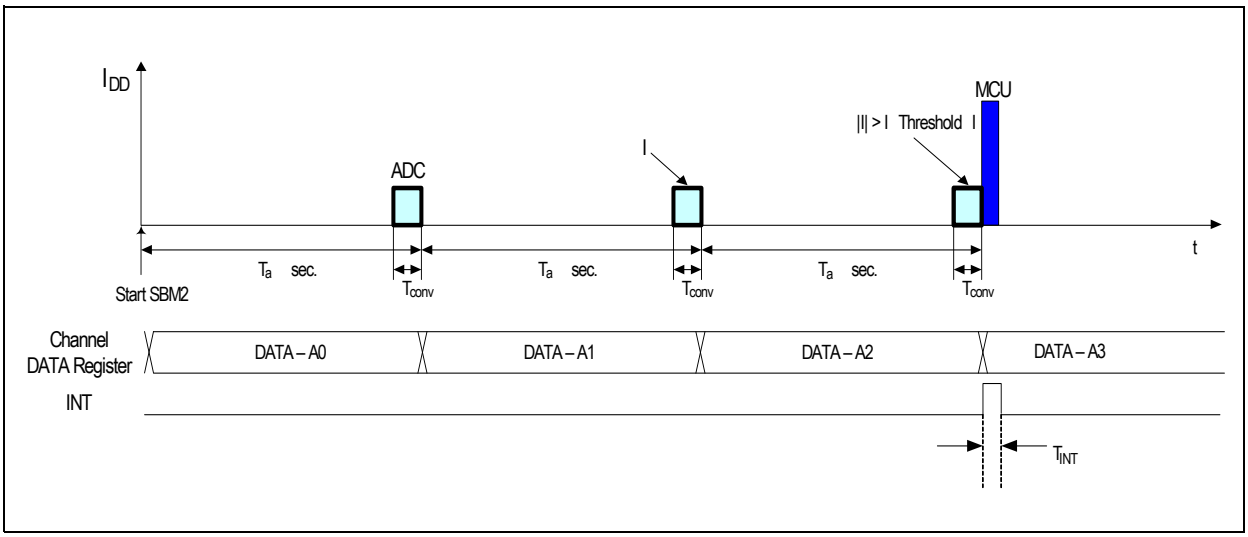
Figure 21. Standby Mode 1



8.7.4 Standby Mode2 (SBM2)

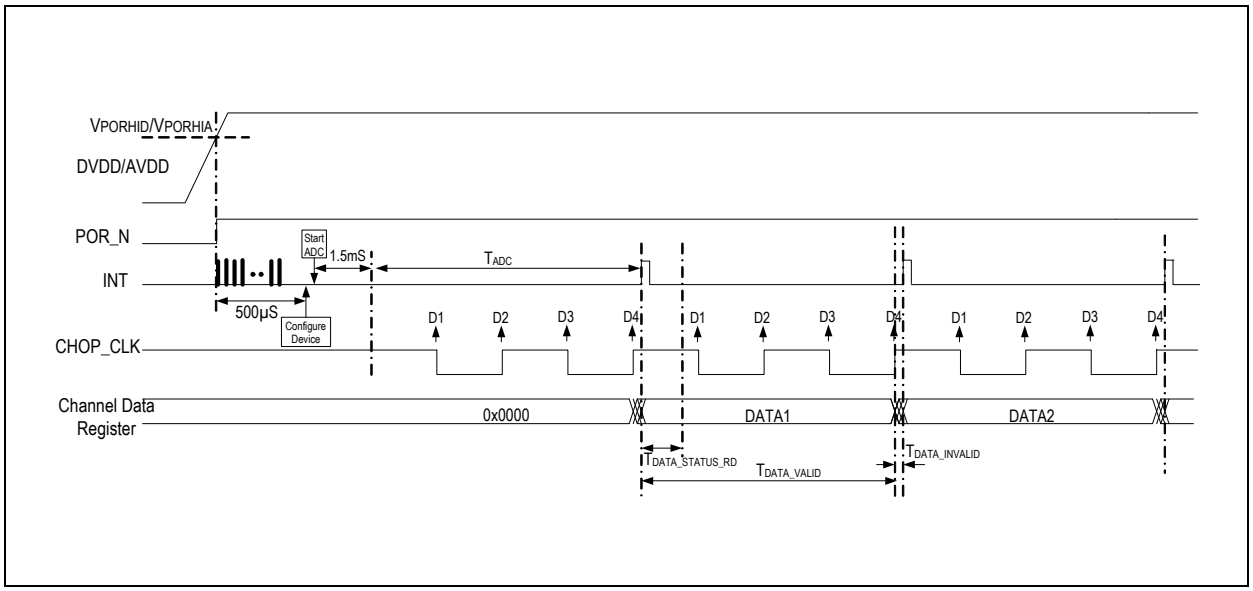
Standby Mode 2 is an extension of the Standby Mode1 to achieve even a lower power in the data acquisition system by providing interrupt to the microcontroller only when the data sample exceeds the set current threshold. The Standby Mode can be entered only through the STOP state. Transition to SBM2 mode occurs when the “START BIT” D0 of Mode Control register MOD_CTL_REG in Table 46 is set to “1” and Mode Control Bits D7,D6 to “1,1” through SPI. In this mode the date rate is programmable with the time of Ta in the Ta control registers B, C. The data sample is made available and an interrupt signal is generated on INT pin only when the input signal exceeds the threshold set in Current Threshold Registers D,E. It should be noted here that the data is stable for Ta seconds. The functionality is illustrated in Figure 22.

Figure 22. Standby Mode 2



8.8 Initialization Sequence at Power ON

Figure 23. AS8510 Device Initialization Sequence at Power ON



Device initialization starts if the DVDD and AVDD supplies are switched ON and DVDD > V_{PORHID}. The duration period of Initialization is 500µsec and during this period, INT pin toggles at the rate of internal low power oscillator. Toggling on INT during the period of initialization should be ignored in the system. Device configuration and activation should be carried out only after the initialization period.

On ADC start, device enters into analog stabilization state and takes 1.5msec for oscillator and Reference to settle. After this 1.5msec period, the first interrupt will occur after a time period of T_{ADC}.

$T_{DATA\_STATUS\_RD}$ is the time period during which the micro-controller should complete reading of data and status from the device. If reading is carried out beyond this time period, then, ADC performance will degrade for next sample generation. Status register gets cleared automatically only when micro-controller reads this register. Data in the channel registers is changed after T_{DATA_VALID} duration. Ensure that data channel registers and status registers are not read during the $T_{DATA\_INVALID}$ duration.

Example:

Configuration registers are set as follows:

CLK_REG = 8'b0010_0000

DEC_REG_R1_I = 0100_0101

DEC_REG_R2_I = 1100_0101

FIR_CTL_REG_I = 0000_0100

ADC is configured to a data rate of 1KHz, CHOP_CLK to 2KHz, and Modulator clock to 1MHz, Decimation ratio of CIC1 = 64, and Decimation ratio of CIC2 = 4. With these settings the various time periods as shown in the Figure 23 are as follows:

$T_{DATA\_STATUS\_RD}$ = 100 µsec

($T_{DATA\_STATUS\_RD}$ = (1/mod_clk) * R1 * [((mod_clk/(2*chop_clk))*(1/R1)) - 2.5)

$T_{DATA\_INVALID}$ = 8 µsec

T_{ADC} = 1msec

$T_{DATA\_VALID} = T_{ADC} - T_{DATA\_INVALID}$ = 1msec - 8 µsec

CHOP_CLK and POR_N are internal signals of the device.

Table 26 provides valid combinations of Modulator clock, Chopper clock and Decimation R1 and the corresponding values of $T_{DATA\_STATUS\_RD}$ and T_{ADC}.

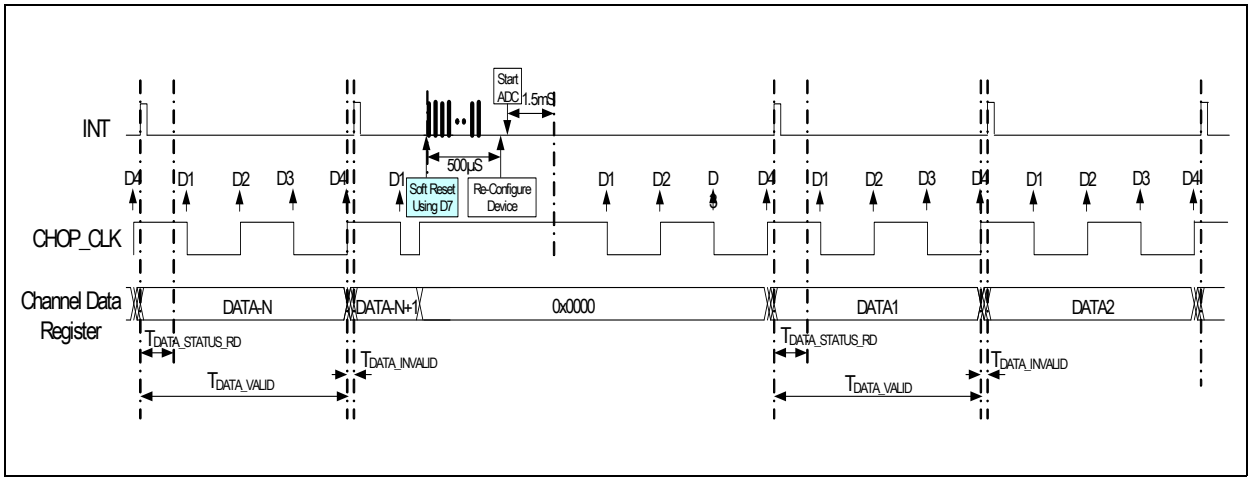
Table 26. Valid Combinations of Modulator Clock, Chopper Clock and Decimation Ratio R1

Modulator Clock	Chopper Frequency CHOP_CLK	Decimation Ratio R1	$T_{DATA\_STATUS\_RD}$	T_{ADC} R2/(2*CHOP_CLK) for R2=4
1.024MHz	2KHz	64	1usec * 64 * [4 - 2.5] = 96usec	1mSec
2.048MHz	2KHz	64	0.5usec * 64 * [8 - 2.5] = 176usec	1mSec
2.048MHz	2KHz	128	0.5usec * 128 * [4 - 2.5] = 96usec	1mSec
2.048MHz	4KHz	64	0.5usec * 64 * [4 - 2.5] = 48usec	0.5mSec

8.8.1 Soft-reset of Device Using Bit D[7] of Reset Register 0x09

It is possible to soft-reset the device by writing "0" into D[7] bit of Reset Register at 0x09. On applying soft-reset, the device enters into initialization state and D[6] bit changes back to "1". The duration period of Initialization is 500µsec, and, during this period, INT pin toggles at the rate of internal low power oscillator. Toggling on INT during the period of initialization should be ignored in the system. Device configuration and activation should be carried out only after the initialization period. See Figure 24 for the timing details of the sequence of device initialization on soft-reset.

Figure 24. AS8510 Device Initialization Sequence at Soft-reset



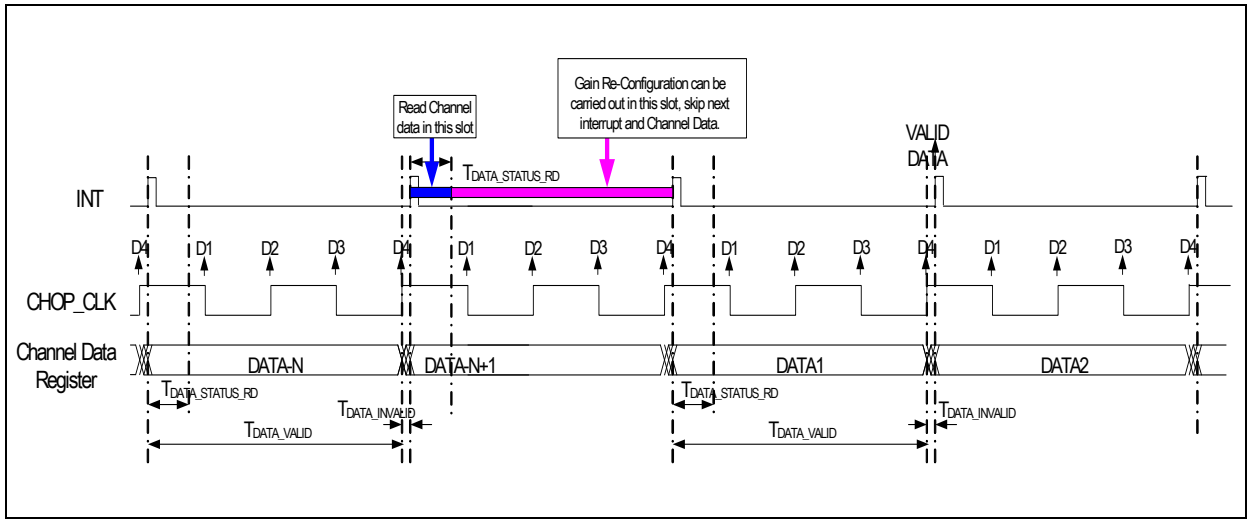
8.8.2 Soft-reset of the Measurement Path Using Bit D[7] of Reset Register 0x09

Measurement path also can be reset by using D[6] bit of Reset Register at 0x09. On applying soft-reset only signal measurement path registers will be reset. For applying this reset, device should be in STOP state. If the device is working with external clock, at the time of soft-reset the clock needs to be disabled.

8.8.3 Reconfiguring Gain Setting of PGA

Only PGA gain settings can be changed dynamically while ADC conversions are in progress. When PGA gain settings are changed, the first sample from the ADC is invalid. Ignore the first interrupt after the gain re-configuration. Valid data starts from the second interrupt onwards.

Figure 25. AS8510 - Re-configuration of Gain Setting of PGA



8.8.4 Configuring the Device During Normal Mode

Following registers can be programmed dynamically when the device is in operational mode (Normal mode).

- ACH_CTL_REG address is 0x17 for channel selection on the voltage measurement path
- PGA_CTL_REG address is 0x13 for gain setting
- PD_CTL_REG2 address is 0x15 for PGA Bypass
- ISC_CTL_REG address is 0x18 for current source programmability

During the operation (Normal mode) of the device, if any of the registers need to be programmed or changed other than the above mentioned registers, then it is required to STOP the device by writing into MOD_CTL_REG “STOP” bit and configure the device as per the requirements and start the device.

8.8.5 Standby Mode - Power Consumption

In Standby Mode 1 there is a timer based accurate measurement every Ta seconds. The device itself stays in idle-mode as long as it does not get a different command from the SPI interface. Internal oscillator frequency is typically foscint=262 kHz to reduce power consumption as long as the timer runs. After every time out of Ta seconds, it performs accurate measurement of current, voltage/ temperature. Data ready is signaled to microcontroller through an interrupt signal on INT and goes into STOP state.

In the SBM the following equations hold:

- T_{sbm1} = Ta= 10s (default value is 10secs); the power consumption is valid for this setting. This is the period of the repetition rate in SBM 1 and SBM2.
- $T_{sett} \approx$ 2ms (depending on external capacitors). This is the time required by the analog part to settle when the new measuring period is started. Any measurements performed during T_{sett} produce invalid results.
- T1 = 3ms (by default setting, every third measurement is sent to microcontroller in the SBM mode 1) is the time needed to perform the first measurement.
- $T_{meas} = T_{sett} + T1$ is the total active time needed to get a valid result.
- $DR_{SBM} = T_{meas}/T_{sbm} \approx$ 5ms/10s. This is the ratio of repetition time versus the active time (Device in NOM mode).

Power consumption = (DR_{SBM}*NOM mode power consumption) + ((10s-5ms)/10s)*Stop mode power consumption)

8.9 Bottom Die Block Specifications

This section provides specification of design related key parameters.

8.9.1 Current Measurement Ranges (across 100µΩ (±5%) shunt resistor)

Table 27. Current Measurement Ranges

Symbol	Parameter	I_{max} [A]	V_{sh} [mV]	PGA Gain Nominal	Data Rate (f_{OUT})	V_{INADC} [1] [mV]	PSR [2] [dB]
I10	Input current range of 10A in NOM	±8.5	±9	100	@ 1 kHz	±1209	60
I200	Input current range of 200A in NOM	±235	±25	40	@ 1 kHz	±1165	60
I400	Input current range of 400A in NOM	±400	±42	25	@ 1 kHz	±1132	60
I1500	Input current range of 1500A in NOM	±2000	±219	5	@ 1 kHz	±1000	60
I1	Input current range of 1A in SBM [3]	±1	±0.1	100	@ 1 Hz	±10	60
I10	Input current range of 10A in SBM [3]	±10	±1	100	@ 1 Hz	±100	60
I200	Input current range of 200A in SBM [3]	±200	±20	40	@ 1 Hz	±800	60

1. $V_{INADC} = V_{sh}$ * Gain, gain deviations to be considered according to Table 29 and Table 30.
2. AVDD, DVDD of 3.3V with ±5% variation.
3. For low power current monitoring, single shot measurement is performed with internal oscillator.

Note: The Data Rate at the output can be calculated according to the formula:

fsout=2*fchop /R2 (R2 is down sampling ratio taking values 1, 2, 4 up to 32768 as powers of 2)

Table 28. Valid Combinations of the Chopper Clock, Oversampling Clock and Decimation Ratios

Over Sampling Frequency	Chopper Frequency	Decimation Ratio
1.024MHz	2kHz	64
2.048MHz	2kHz	64
2.048MHz	2kHz	128
2.048MHz	4kHz	64

Differential Input Amplifier for Current Channel.

Table 29. Differential Input Amplifier for Current Channel

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN_AMP}	Input voltage range	RSHH and RSHL	-160		+160	mV
I_{IN_AMP}	Input current [1, 11]	RSHH and RSHL@ +160mV input voltage at 125ºC with PGA	-50	2	50	nA
ICM	Absolute input voltage range [2]			-160 +300		mV
G = G1	Gain1 [3, 4, 9]	I10		100		
G = G2	Gain2 [3, 4, 9]	I200		40		
G = G3	Gain3 [3, 4, 9]	I400		25		
G = G4	Gain4 [3, 4, 9]	I1500		5		
e	Gain deviation	i = 1, 2, 3, 4	0.9 * Gi		1.1 * Gi	
f_{P_AMP}	Pole frequency [4, 5]		15			kHz
εT1	Gain drift with temperature [6]	-20ºC to +65ºC Gain 5, 25, referenced to room temperature			±0.5	%
$V_{OSDRIFT}$	Offset drift with temperature [7, 10]			350		µV
V_{os}	Input referred offset [7, 10]	After trim, for temperature range -20 to 350µV at -20ºC			350	µV
V_{os_ch}		Chopping enabled		0		LSB
V_{Ndin}	Noise density [4, 8]			25		nV/√Hz
THD	Total harmonic distortion	For 150 Hz input signal		70		dB

Notes:

1. Leakage test accuracy is limited by tester resource accuracy and tester hardware.
2. For gain 100 PGA input common mode is 0V and the minimum supply is 3.15V.
3. The measurement ranges are referred only by the gain of input amplifier, while other parameters such as bandwidth etc. are programmed independently.
4. This parameter is not measured directly in production. It is measured indirectly via gain measurements of the whole path. It is guaranteed by design.
5. Pole frequency of input amplifier changes with GAIN. The number is valid for the gain at G1, while the bandwidth will be higher for other ranges. This parameter is not measured in production.
6. Based on device evaluation. Not tested.
7. These offsets are cancelled if chopping enabled (default).
8. Noise density calculated by taking system bandwidth as 150Hz.
9. Refer to Measurement Ranges shown in Table 27.
10. No impact on the measurement path. If the chopping is enabled, both the offset and offset drift will be eliminated.
11. For negative input voltages up to -160mV below ground, Input leakage is typically -20nA @ 65ºC due to forward conductance of protection diode.

Differential Input Amplifier for Voltage Channel.

Table 30. Differential Input Amplifier for Voltage Channel

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN_AMP}	Input voltage range [1, 10]		-160		+160	mV
I_{IN_RES}	Input resistance [2, 10]	VBAT_IN, ETR, ETS @ +160mV input voltage at 125ºC with PGA		12.5		kΩ
ICM	Absolute input voltage range [3]			-160 +300		mV
G = G1	Gain1 [4, 5]			100		
G = G2	Gain2 [4, 5]			40		
G = G3	Gain3 [4, 5]			25		
G = G4	Gain4 [4, 5]			5		
e	Gain deviation	i = 1, 2, 3, 4	0.9 * Gi		1.1 * Gi	
f_{P_AMP}	Pole frequency [5, 6]		15			kHz
V_{NDIN}	Noise density [5, 7]			25		nV/√Hz
THD	Total harmonic distortion	For 150Hz input signal		70		dB
εT1	Gain drift with temperature [8]	-20ºC to +65ºC Gain 5, 25, referenced to room temperature			±0.5	%
V_{OS}	Input referred offset [9]	After trim at -20ºC			350	µV
V_{os_ch}		Chopping enabled		0		LSB
$V_{OSDRIFT}$	Offset drift with temperature [9]			350		µV

Notes:

1. Input for the voltage channel can be as high as 1220mV, in this high input case PGA will be bypassed.
2. Leakage test accuracy is limited by tester resource accuracy and tester hardware, especially at low temperatures due to condensing moisture.
3. For gain 100 PGA input common mode is 0V and the minimum supply is 3.15V.
4. The measurement ranges are referred only by the gain of input amplifier, while other parameters such as bandwidth etc. are programmed independently.
5. This parameter is not measured directly in production. It is measured indirectly via gain measurements of the whole path. It is guaranteed by design.
6. Pole frequency of input amplifier changes with changing the GAIN. The number is valid for the gain at G1, while the bandwidth will be higher for other ranges. This parameter is not measured in production.
7. Noise density calculated by taking system bandwidth as 150Hz.
8. Based on device evaluation. Not tested.
9. No impact on the measurement path. If the chopping is enabled, both the offset and offset drift will be eliminated.
10. For negative input voltages up to -160mV below ground, Input leakage is typically -20nA @ 65ºC due to forward conductance of protection diode.

Sigma Delta Analog to Digital Converter.

Table 31. Sigma Delta Analog to Digital Converter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	Reference voltage [6]			1.225		V
V_{INADC}	Input range [1]	At V_{REF} = 1.22V	0		±1.22	V
R1	Oversampling ratio/Decimation Ratio [2]		64	128	128	
f_{OVS}	Oversampling frequency [3]			1024/ 2048		kHz
RES	Number of bits				16	bits
BW	Bandwidth [4]		1		500	Hz
S/N	Signal to noise ratio [5]			90		dB

Notes:

1. Production test at ±800mV. Maximum V_{IN} can be 1.22V with VREF=1.225V.
2. Programmable. It is defined with respect to the first decimator in the ΣΔ ADC.
3. Programmable: Internal clock is 1024/2048 kHz; external clock max is 8192 kHz.
4. Dependent on fovs, R1 and R2. The bandwidth is calculated according to the formula: BW=fovs/(2*R1*R2); the sampling frequency at the output of the A/D converter is 2*BW.
5. Defined at maximum input signal, BW=500 Hz (1Hz to 500 Hz), fovs=1024 kHz, R1=64, fchop=2 kHz and R2=2.
6. Reference voltage might be forced from external.

Bandgap Reference Voltage.

Table 32. Bandgap Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{REFTRIM}$	Reference Voltage after trim [1, 2]	Trim at 65ºC		1.225		V
V_{REFACC}	Reference Voltage Initial Accuracy [1, 2]	At 65ºC			±3.5	mV
$V_{REFDRIFT}$	Reference Voltage Temperature drift	Temperature range -20ºC to 65ºC			±0.4	%
		Temperature range -40ºC to 125ºC		+0.4/ -0.6		%
$PSRR_{REF}$	PSR @ dc			80		dB
SUT_{AVDD}	Start Up Time with supply ramp [3]			5		ms
SUT_{PD}	Start Up Time from power down [3]				1	ms
R_{NDVREF}	Output resistance of band gap			500	1000	Ω
V_{NDVREF}	Bandgap reference thermal noise density [3]				300	nV/√Hz
CL_{VREF}	Output Capacitor (Ceramic)			100		nF
ESR_{VREF}			0.02		1	Ω

Notes:

1. Accuracy at 65ºC.
2. No DC current is allowed from this pin.
3. This is a design parameter and not production tested.

Internal (Programmable) Current Source for External Temperature Measurement.

Table 33. External Temperature Measurement

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CURON}	5-bit current source enabled [1]	5-bit programmable current source	0	270	320	µA
I_{CUROFF}	5-bit current source disabled	Limited by leakage		10		nA
T_{K_CS}	Temperature coefficient of current source [2]			1000		ppm / °K
V_{MAXETR}	Voltage on pin ETR [3]				1000/G	mV
$V_{MAXETRMOD}$	Max voltage on pin ETR when PGA is bypassed [4]				1.22	V
V_{MAXETS}	Voltage on pin ETS for resistor sensor [3]				1000/G	V
$V_{MAXETSMOD}$	Max. Voltage on pin ETS when PGA is bypassed [5]				1.22	V

Notes:

1. Current value can be programmed through stop mode in steps of 8µA from 0 to 256µA with a process error of 30%.
2. Temperature coefficient is not important since external temperature measurement is a 2 step measurement. The value specified is guaranteed by design and will not be tested in production.
3. Maximum voltage on pin ETR (reference) can be calculated by given formula, where G is the gain of PGA (G=100).
4. Maximum voltage on pin ETR, if PGA is bypassed.
5. Maximum voltage on pin ETS, if PGA is bypassed.

CMREF Circuit (VCM).

Table 34. CMREF Circuit

Symbol	Parameter	Min	Typ	Max	Units
V_{VCM}	Output voltage	1.6	1.7	1.8	V
C_L	Load capacitance		100		nF

Internal AVDD Power-on Reset.

Table 35. Internal AVDD Power-on Reset

Symbol	Parameter	Min	Typ	Max	Units
V_{PORHIA}	Power On Reset Threshold	2.2	2.4	2.6	V
t_{PORA}	POR time - The duration from Power ON till the time, internal Power On Reset signal goes HIGH[1]	1			µs
I_{PORA}	Current consumption in POR block[2]		1.5		µA

1. POR pulse is always longer than t_{PORA} whatever the slope of the supply.
2. I_{PORA} can not be switched off.

Internal DVDD Power-on Reset.

Table 36. Internal DVDD Power-on Reset

Symbol	Parameter	Min	Typ	Max	Units
V_{PORHID}	Power On Reset Threshold	2.2	2.4	2.7	V
V_{HYST}	Hysteresis[1]	0.2	0.25	0.4	V
t_{PORD}	POR time - The duration from Power ON till the time, internal Power On Reset signal goes HIGH[2]	1			µs
I_{PORD}	Current[3]		1.5		µA

1. $V_{PORLO} = V_{PORHI} - V_{HYST}$ where V_{PORLO} is the lower threshold of POR.
2. $V_{PORLO} = V_{PORHI} - V_{HYST}$ where V_{PORLO} is the lower threshold of POR.
3. I_{PORD} can not be switched off.

Low Speed Oscillator.

Table 37. Low Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Units
f_{LS}	Frequency		262.144		kHz
f_{LS_ACC}	Accuracy		± 7		%
I_{LS}	Supply current		5		µA

High Speed Oscillator.

Table 38. High Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Units
f_{HS}	Frequency		4.096		MHz
f_{HSACC}	Accuracy [1]		±4		%
I_{HS}	Supply current		300		µA

Notes:

1. Accuracy after trimming.

External Clock.

Table 39. External Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CLKEXT}	Clock frequency			2048/ 4096/ 8192		kHz
DIV_{CLKEXT}	Clock division factor	to be programmed in Register 08 CLK_REG through the serial bus SPI.		2/4/8		
DC_{CLKEXT}	Duty Cycle of external clock		40		60	%

Internal Temperature Sensor.

Table 40. Internal Temperature Sensor

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{INTRNG}	Temperature sensor range		-40		125	ºC
ΔT_{IN}	Temperature measurement accuracy			3		ºC
T_{INTSLP}	Temperature sensor slope	Guaranteed by design; at PGA gain 5 which is the recommended Gain for internal temperature measurement.		27		Digits/C
TINT65G5	Temperature sensor output at gain 5		40660	41807	43012	Digits

8.9.2 System Specifications

Table 41. System Specifications

Symbol	Parameter	Min	Typ	Max	Units
I_S	Channel to channel isolation [1]			-90	dB
At	Difference in channel to channel attenuation @600Hz [1, 2]			3	dB
Ph	Difference in phase shift between the two channels @600Hz [1, 2]			5	Deg

System Measurement Error Budget for Voltage and Current Channel.

Temperature Range: -20ºC to +65ºC; Output data rate is 1kHz, VCC = 3.3V, chopping enabled.

Table 42. System Measurement Error Budget for Gains 5 and 25

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Err	System measurement error [3, 4]			±0.6	1	%
	Measurement error due to PGA gain drift	From device evaluation			±0.5	%
	Measurement error due to VREF drift				±0.4	%
	Measurement error due to non-linearity of PG	Tested by distortion measurements			±0.025	%

Notes:

1. These specifications are defined by taking one channel as reference and measured on the other channel.
2. Guaranteed by design.
3. System measurement error due to noise, individual block parameter drifts and non linearity. Based on evaluation, not tested.
4. System error due to offset is neglected because of chopper architecture.

9 4-Wire SPI Interface

The SPI interface can also be used as interface between the AS8515 and an external micro-controller to configure the device and access the status information. Micro-controller begins communication with the SPI configured as a slave. The SPI protocol is very simple and the length of each frame is an integer multiple of byte except when a transmission is started. Basically each frame has 1 command bits, 5 address/ configuration bits, 1 or more data bytes. SPI clock polarity settings depend on the value of the SCLK on the CS falling edge. This setting is done on each start of the SPI transaction. During the transaction SPI clock polarity will be fixed to the settings done. On the CS falling edge the values on SCLK signal decide setting of the active SPI clock edge for data transfer (see Table 43).

Table 43. CS and SCLK

CS[1]	SCLK	Description
FALL	LOW	Serial data transferred on rising edge of SPI clock. Sampled at falling edge of SPI clock.
FALL	HIGH	Serial data transferred on falling edge of SPI clock. Sampled at rising edge of SPI clock.
ANY	ANY	Serial data transfer edge is unchanged.

1. Pin CST is used to program top device and pin CSB is used to program bottom device.

9.1 SPI Timing Parameters

Table 44. 4-Wire Serial Port Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
BR_{SPI}	Bit rate				250	Kbps
T_{SCLKH}	Clock high time		2			µs
T_{SCLKL}	Clock low time		2			µs
Write Timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
T_{CSH}	CS hold time		20			ns
Read Timing						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns
Timing parameters when entering 4-Wire SPI mode (for determination of CLK polarity)						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns

9.1.1 SPI Frame

A frame is formed by a first byte for command and address/configuration and a following bit stream that can be formed by an integer number of bytes. Command is coded on the 1 first bit, while address is given on LSB 5 bits (see Table 45).

Table 45. Command Bits

Command Bits			Register Address or Transmission Configuration				
C0	Reserved	Reserved	A4	A3	A2	A1	A0

C0	Command	<A4:A0>	Description
0	WRITE	ADDRESS	Writes data byte on the given starting address
1	READ	ADDRESS	Reads data byte from the given starting address

If the command is read or write, one or more bytes follow. When the micro-controller sends more bytes (keeping CS LOW and SCLK toggling), the SPI interface increments the address of the previous data byte and writes/reads data to/from consecutive addresses.

9.1.2 Write Command

For Write command C0 = 0.

After the command code C0 and two reserved bits, the address of register to be written has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred, always from the MSB to the LSB. For each data byte following the first one, used address is the incremented value of the previously written address. Each bit of the frame has to be driven by the SPI master on the SPI clock transfer edge and the SPI slave on the next SPI clock edge samples it. These edges are selected as per clock polarity settings. In the following figures two examples of write command (without and with address self-increment.

Figure 26. Protocol for Serial Data Write with Length = 1

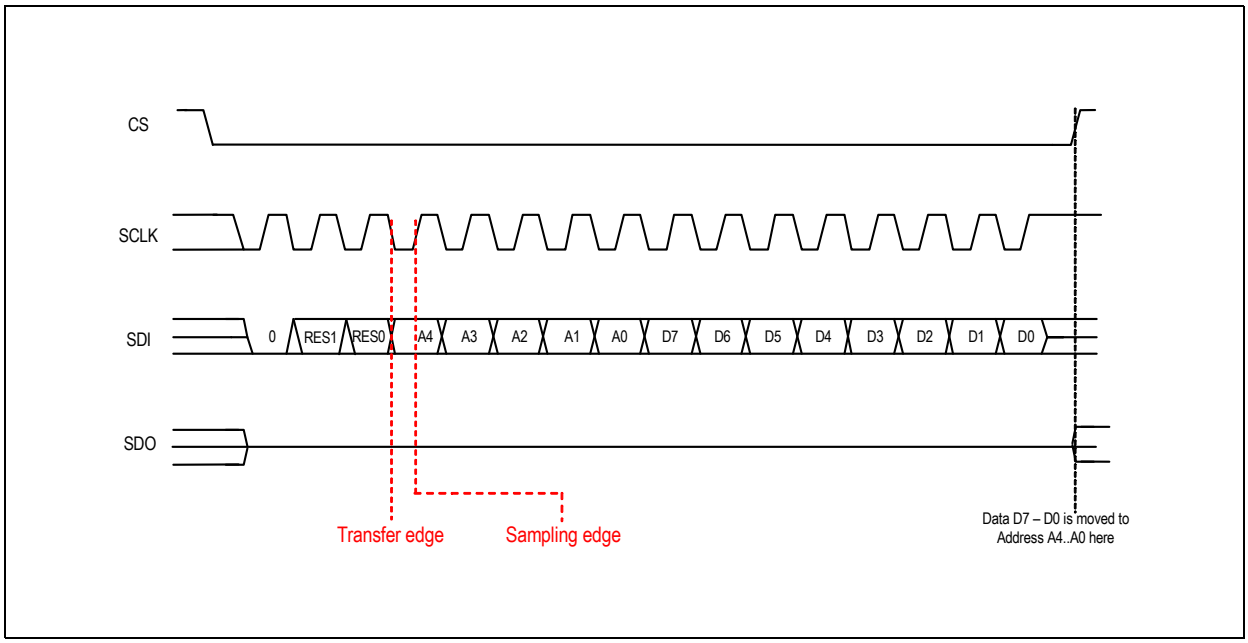
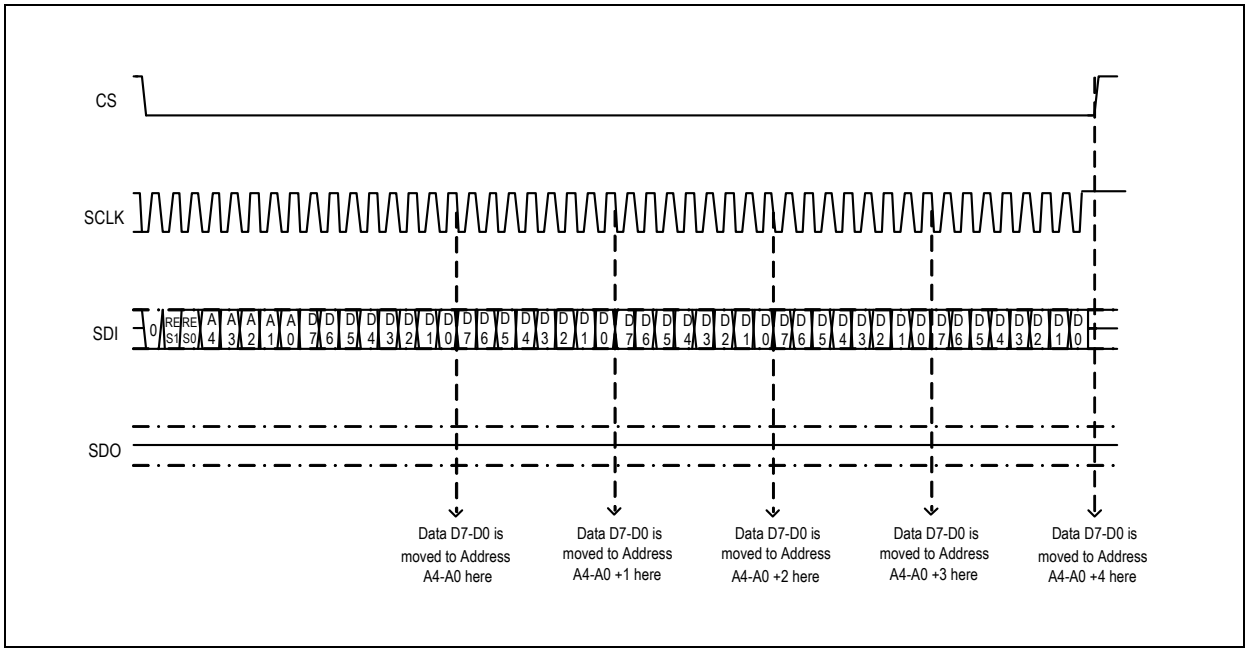


Figure 27. Protocol for Serial Data Write with Length = 4



9.1.3 Read Command

For Read command C0=1.

After the command code C0 and two reserved bits, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB. To transfer more bytes from consecutive addresses, SPI master has to keep active the SPI CS signal and the SPI clock as long as it desires to read data from the slave. Each bit of the command and address sections of the frame have to be driven by the SPI master on the SPI clock transfer edge and the SPI slave on the next SPI clock edge samples it. Each bit of the data section of the frame has to be driven by the SPI slave on the SPI clock transfer edge and the SPI master on the next SPI clock edge samples it. These edges are selected as per clock polarity settings. In the following figures, two examples of read command (without and with address self-increment) have been shown.

Figure 28. Protocol for Serial Data Read with Length = 1

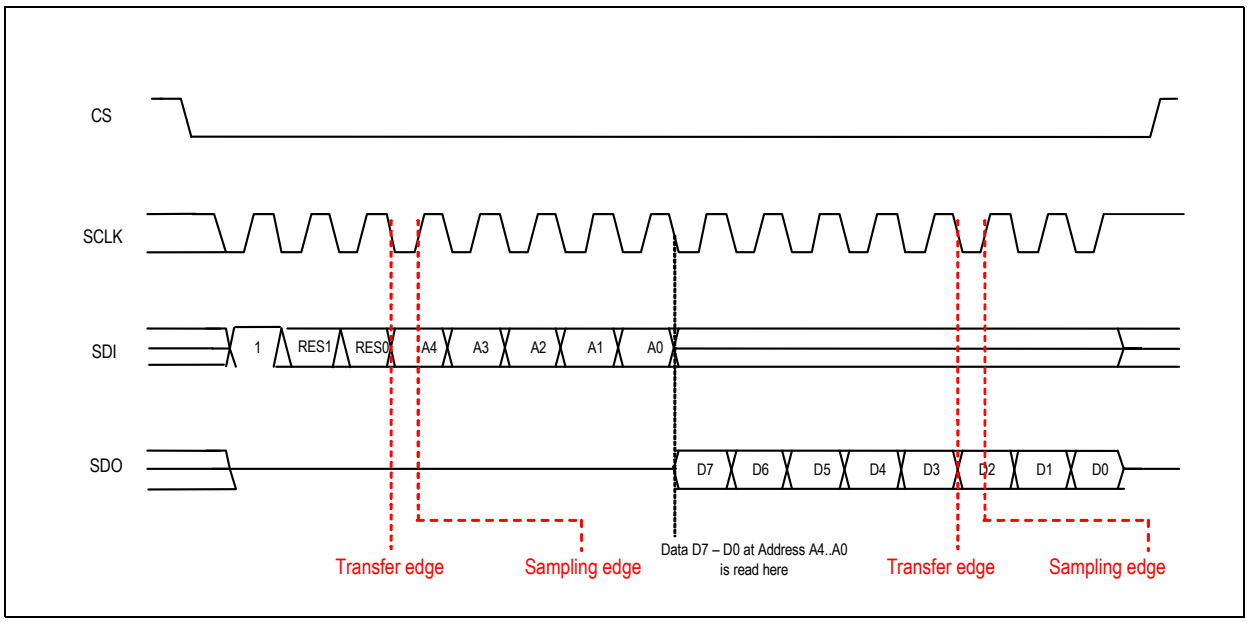
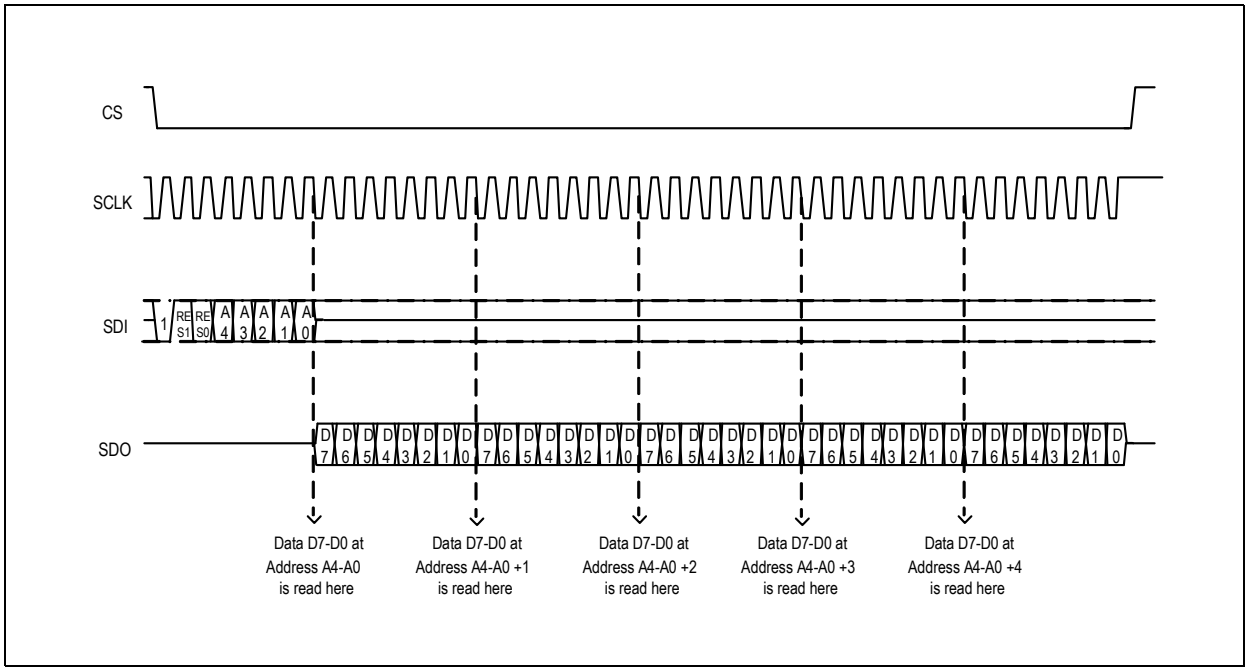


Figure 29. Protocol for Serial Data Read with Length = 4



9.1.4 Timing

In the following figures timing waveforms and parameters are exposed.

Figure 30. Timing for Writing

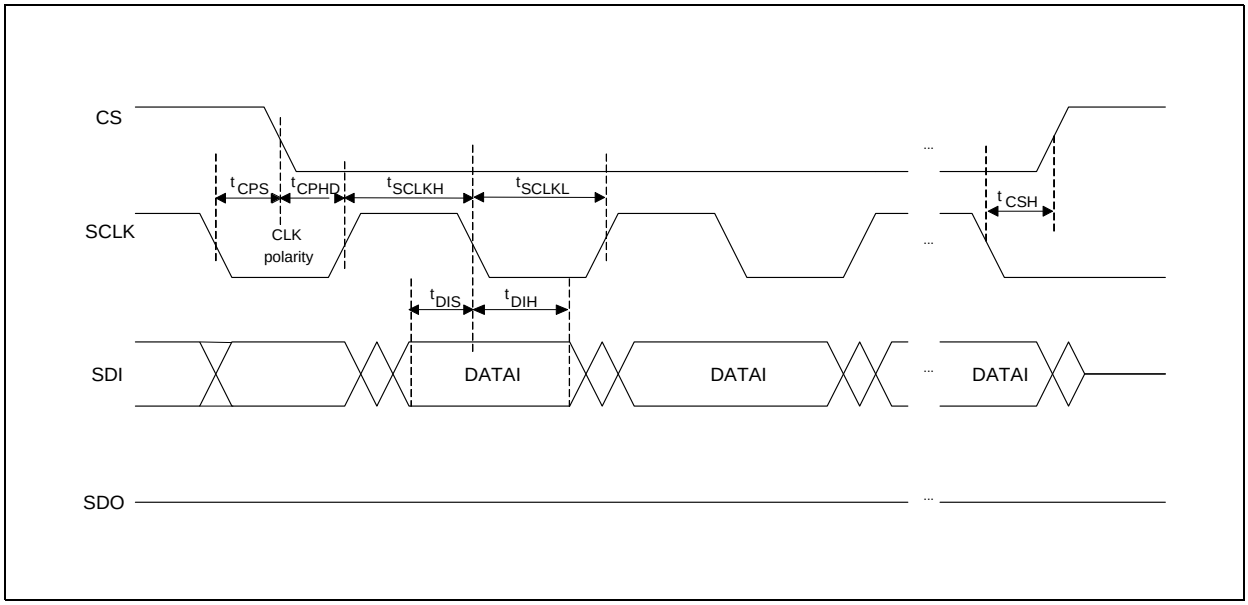
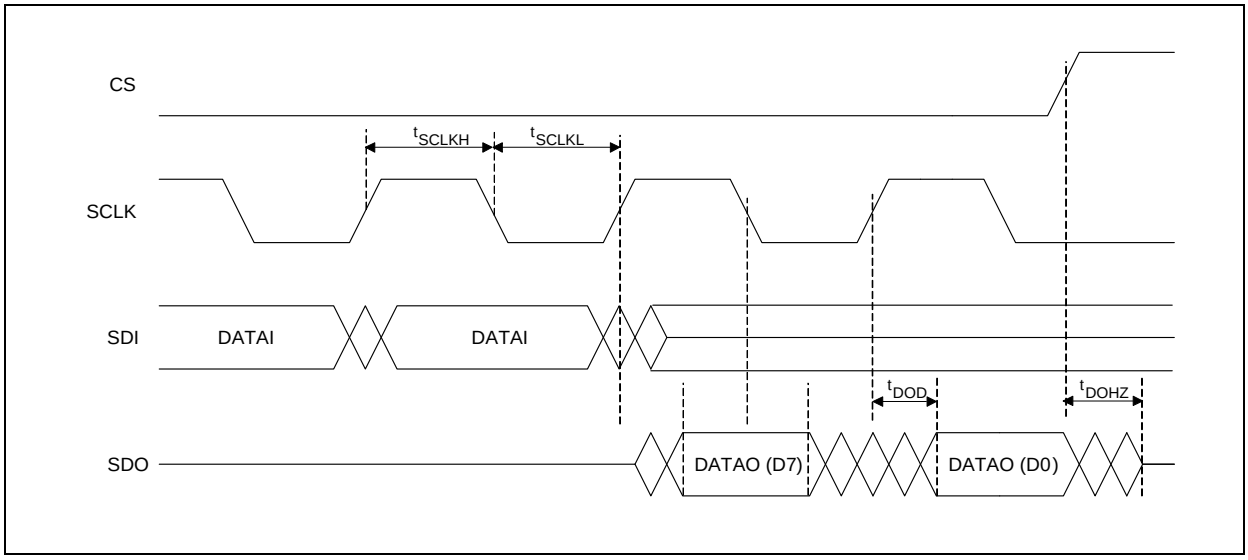


Figure 31. Timing for Reading



9.2 Bottom Die Registers

This section describes the control registers used in AS8515 *Bottom die*. Registers can be broadly classified into the following categories.

- Data access registers
- Status Registers
- Digital signal path control registers
- Digital Control registers
- Analog Control Registers

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data	
Data Access Registers					
00	DREG_I1 (ADC Data Register for Current)	0000_0000	R	D[7:0]	Denotes the Current ADC MSB Byte (ADC_I[15:8])
01	DREG_I2 (ADC Data Register for Current)	0000_0000	R	D[7:0]	Denotes the Current ADC LSB Byte (ADC_I[7:0])
02	DREG_V1 (ADC Data Register for Voltage)	0000_0000	R	D[7:0]	Denotes the Voltage ADC MSB Byte (ADC_V[15:8])
03	DREG_V2 (ADC Data Register for Voltage)	0000_0000	R	D[7:0]	Denotes the Voltage ADC LSB Byte (ADC_V[7:0])
Status Registers					
04	STATUS_REG	0000_0000	R	D[7]	NOM1/NOM2 Data Ready
				D[6]	NOM2 Threshold Crossover
				D[5]	SBM1 Data Ready
				D[4]	SBM2 Threshold Crossover
				D[3]	APOR status
				D[2]	Data from current channel updated
				D[1]	Data from voltage channel updated
				D[0]	Reserved

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
Digital Signal Path Control Registers for Current Channel						
05	DEC_REG_R1_I	0100_ 0101	R/W	D[7]	This bit selects decimation rate is used for current channel. Default is 0 (Down Sampling Rate is 64)	
					0	Down Sampling Rate is 64
					1	Down Sampling Rate is 128
				D[6:5]	These two bits select division ratio of oversampling frequency clock MOD_CLK to be used as chopper clock, CHOP_CLK. Default is “10” (divide by 512)	
					00	Chopper Clock Always High
					01	Divide by 256
					10	Divide by 512
					11	Divide by 1024
				D[4:1]	These four bits select the decimation ratio of second CIC stage. Default is “0010” (equal to 4)	
					0000	1
					0001	2
					0010	4
					0011	8
					0100	16
					0101	32
					0110	64
					0111	128
					1000	256
					1001	512
					1010	1024
					1011	2048
					1100	4096
					1101	8192
					1110	16384
					1111	32768
				D[0]	CIC1 Saturation Interrupt Mask Control. Default is 1	
					0	Unmask
					1	Mask

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
06	DEC_REG_R2_I	1100_0101	R/W	D[7]	I-Channel Enable, Default 1=enable	
				D[6]	V-Channel Enable, Default 1=enable	
				D[5]	Interrupt polarity	
					0	Active high
					1	Active low
				D[4]	. Interrupt Mask Control for Current Channel Data Ready Interrupt on INT pin (Default is 0)	
					0	Unmasked
					1	Masked
				D[3:2]	These two bits select the source of output 16-bit data in Normal mode from Current channel. Default is 01	
					00	FIR / MA Output
					01	CIC2 Output
					10	Dechop/Demod Output
					11	CIC1 Output
				D[1:0]	These two bits select the source of output 16-bit data in SBM mode from Current channel. Default is 01	
					00	FIR / MA Output
					01	CIC2 Output
					10	Dechop/Demod Output
					11	CIC1 Output
07	FIR CTL_REG_I	0000_0100	R/W	D[7]	This bit selects FIR / MA Filter in Current channel. Default is 0 (FIR)	
					0	FIR
					1	MA Filter
				D[6:3]	These bits select the number of data samples for averaging in MA filter in Current channel. Default is 0000 (bypass)	
					0000	bypass
					0001	1
					0011	3
					0111	7
					1111	15
				D[2:1]	These two bits select the Measurement Path architecture in both Current and Voltage channels. Default is 10 (Dechopper after CIC)	
					00	Demodulator after CIC1
					01	Demodulator before CIC1
					10	Dechopper after CIC1 (preferred and suggested)
					11	Demodulator before CIC1 with settled sample
				D[0]	Reserved. Default 0. Do not change	

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
Digital Control Registers						
08	CLK_REG (Clock Control Register)	0010_0000	R/W	D[7:6]	Oversampling frequency clock selection. Default is 00 (high speed (HS) internal Clock)	
					00	Internal HS Clock with No Clock Output
					01	Internal HS Clock with Clock Output
					10	External Clock
				D[5:4]	These two bits select the division ratio for HS clock/ external clock. Default is 10 (division by 4)	
					00	No division
					01	Divide by 2
					10	Divide by 4
					11	Divide by 8
				D[3:2]	These two bits select the division ratio of HS clock, by which it should be divided before providing it on CLK pin. Default is 00 (No Division)	
					00	No Division
					01	Divide by 2
					10	Divide by 4
					11	Divide by 8
				D[1]	This bit selects the division ratio of LS clock	
					0	LS _CLK undivided (Low Speed clock)
					1	LS _CLK divide by 2
				D[0]	Reserved	
09	RESET_REG (Reset Control Register)	1100_0000	R/W	D[7]	Entire device can be soft reset by writing “0” into this register bit. This bit will take a default 1 value on coming out of Reset	
				D[6]	Measurement Path can be soft reset by writing “0” into this register bit. This bit will take a default 1 value after Measurement Path is reset.	
				D[5:0]	Reserved	

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
0A	MOD_CTL_REG (Mode Control Registers)	0000_0000	R/W	D[7:6]	These two bits select the operating mode of the Device. Default is 00 (Normal Mode 1)	
					00	Normal Mode 1
					01	Normal Mode 2
					10	Standby Mode 1
					11	Standby Mode 2
				D[5:3]	These three bits select the number of cycles to be ignored before comparison with the set threshold in Standy Mode. Default is 000 (3 cycles of data)	
					000	3 cycles of data
					001	4 cycles of data
					010	5 cycles of data
					011	6cycles of data
					100	7 cycles of data
					101	8 cycles of data
					110	9 cycles of data
					111	10 cycles of data
				D[2]	This bit controls the CHOP_CLK availability on CHOP_CLK pin. Default is 0	
					0	Disabled
					1	Enabled
				D[1]	Enabling the MEN pin to indicate transition from Standby to Normal Mode.	
					0	Disabled
					1	Enabled
				D[0]	This bit is used to take the device from STOP state to any of the Modes based on D[7:6] selection of this register.	
					0	Retain in STOP state
					1	Enables transition to Normal or Standby Modes.
0B	MOD_Ta_REG1 (Ta Control Register)	1000_0000		D[7]	Unit of Ta in SBM1/SBM2. Default is 1	
					0	Unit is in milliseconds
					1	Unit is in seconds
				D[6:0]	MSB value of Ta	
0C	MOD_Ta_REG2 (Ta Control Register)	0000_0000	R/W	D[7:0]	Unit of Ta in SBM1/SBM2 LSB value of Ta	
0D	MOD_ITH_REG1 (Current Threshold Register)	0000_0000	R/W	D[7:0]	MSB bits of 16 bits SBM2 threshold register	
0E	MOD_ITH_REG2 (Current Threshold Register)	0000_0000	R/W	D[7:0]	LSB bits of 16 bits SBM2 threshold register	

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
0F	MOD_TMC_REG1 (T_{MC} Control Registers)	0000_0000	R/W	D[7:0]	MSB value of number of data samples to be dropped from ADC before sending Interrupt in NOM2	
10	MOD_TMC_REG2 (T_{MC} Control Register)	0000_0000	R/W	D[7:0]	LSB value of number of data samples to be dropped from ADC before sending Interrupt in NOM2	
11	NOM_ITH_REG1	0000_0000	R/W	D[7:0]	Eight MSB bits of NOM2 current threshold register	
12	NOM_ITH_REG2	0000_0000	R/W	D[7:0]	Eight LSB bits of NOM2 current threshold register	
Analog Control Registers						
13	PGA_CTL_REG (PGA Control Registers)	0101_0000	R/W	D[7:6]	Setting of Gain G of Current Channel PGA. Default is 01 (G = 25)	
					00	5
					01	25
					10	40
					11	100
				D[5:4]	Setting of Gain G in Voltage channel. Default is 01 (G = 25)	
					00	5
					01	25
					10	40
					11	100
				D[3:0]	Reserved	
14	PD_CTL_REG_1 (Power Down Control Register)	1100_1111	R/W			
				D[7]	0	Disable Chopper clock to Current channel
					1	Enable Chopper clock to Current channel
				D[6]	0	Disable Chopper clock to Voltage channel
					1	Enable Chopper clock to Voltage channel
				D[5]	Reserved	
				D[4]	Reserved	
				D[3]	0	Disable Current channel PGA
					1	Enable Current channel PGA
				D[2]	0	Disable Current channel ΣΔ Modulator
					1	Enable Current channel ΣΔ Modulator
				D[1]	0	Disable Voltage channel PGA
					1	Enable Voltage channel PGA
				D[0]	0	Disable Voltage channel ΣΔ Modulator
					1	Enable Voltage channel ΣΔ Modulator

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
15	PD_CTL_REG_2 (Power Down Control Register)	1111_0011	R/W	D[7]	0	Disable CIC1 of both channels
					1	Enable CIC1 of both channels
				D[6]	0	Disable CIC2 of both channels
					1	Enable CIC2 of both channels
				D[5]	0	Disable Dechopper in both channels
					1	Enable Dechopper in both channels
				D[4]	0	Disable FIR in both channels
					1	Enable FIR in both channels
				D[3]	0	Do not bypass PGA in Current Channel Default 0
					1	Bypass PGA in Current Channel
				D[2]	0	Do not bypass PGA in Voltage Channel Default 0
					1	Bypass PGA in Voltage Channel
				D[1]	0	Disable Current Channel Chopper
					1	Enable Current Channel Chopper
				D[0]	0	Disable Voltage Channel Chopper
					1	Enable Voltage Channel Chopper
16	PD_CTL_REG_3 (Power Down Control Register)	1111_1000		D[7]	0	Disable Common Mode Reference
					1	Enable Common Mode Reference
				D[6]	0	Disable Internal Current Source
					1	Enable Internal Current Source
				D[5]	0	Disable Internal temperature sensor
					1	Enable Internal temperature sensor
				D[4]	Reserved. (Default 1) Do not change	
				D[3]	Reserved. (Default 1) Do not change	
				D[2]	0	Data Output in binary numbering system
					1	Data Output in 2's complement numbering system
				D[1]	Reserved. (Default 0) Do not change	
				D[0]	Reserved	

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
17	ACH_CTL_REG (Analog Channel Selection Register)	0000_0000	R/W	D[7:6]	These bits specify the selection of voltage/temperature in Voltage Channel Default is 00 (Voltage Channel)	
					00	Voltage Channel
					01	External Temperature Channel ETR
					10	External Temperature Channel ETS
					11	Internal Temperature Channel
				D[5]	Reserved. (Default 0) Do not change	
				D[4]	Internal current source switch enable. Default is 0 **Note:** D4 bit is used for Enabling current source to the channel selected by bits D[7,6] of this register.	
					0	Disabled
					1	Enabled
				D[3]	Enable/disable Internal current source to RSHH pin of Current channel	
					0	Disabled
					1	Enabled
				D[2]	Enable/disable current source switch to RSHL pin of Current channel	
					0	Disabled
					1	Enabled
				D[1:0]	Reserved	
18	ISC_CTL_REG (Current Source Setting Register)	0000_0000	R/W	D[7:3]	These three bits specify the selection of magnitude of current from the Internal current source. Default is 00000 (0µA).	
					00000	0µA
					00001	8.5µA
					00010	17µA
					00100	34.5µA
					01000	68µA
					10000	135µA
					11111	270µA
				D[2:0]	Reserved	
19	OTP_EN_REG	0000_0000	R/W	D[7]	1	Reserved (default = 1) Do not change
				D[6:0]	Reserved	
44	STATUS_REG_2	0000_0000	R	D[7]	Status indicating data saturation in Current channel	
				D[6]	Status indicating data saturation in Voltage channel	
				D[5:0]	Reserved	

Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
Digital Signal path control registers for Voltage Channel						
45	DEC_REG_R1_V	0100_ 0101	R/W	D[7]	Selection of Decimation ratio for Voltage/Temperature channel. Default is 0 (Down Sampling Rate is 64)	
					0	Down Sampling Rate is 64
					1	Down Sampling Rate is 128
				D[6:5]	Division of oversampling clock, which is used as Chopper Clock. Default is 10 (divide by 512)	
					00	Chopper Clock Always High
					01	Divide by 256
					10	Divide by 512
					11	Divide by 1024
				D[4:1]	Decimation ratio of CIC2. Default is 0010 (4)	
					0000	1
					0001	2
					0010	4
					0011	8
					0100	16
					0101	32
					0110	64
					0111	128
					1000	256
					1001	512
					1010	1024
					1011	2048
					1100	4096
					1101	8192
					1110	16384
					1111	32768
				D[0]	CIC1 Saturation Interrupt Mask Control. Default is 1	
					0	Unmasked
					1	Masked

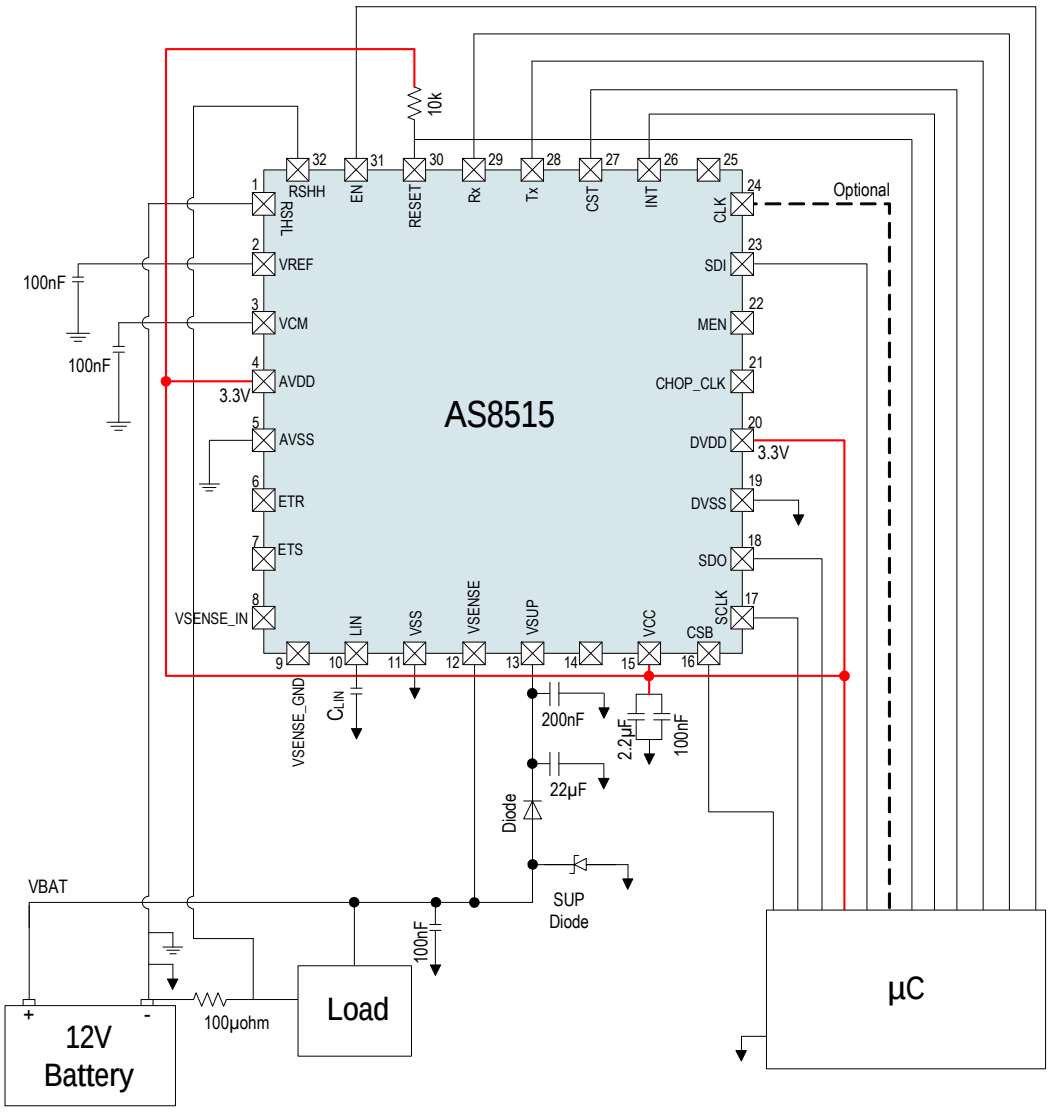
Table 46. Control Registers

Addr in HEX	Register Name	POR Value	R/W	8-bit Control / Status Data		
46	DEC_REG_R2_V	0000_0100	R/W	D[7:5]	Reserved	
				D[4]	Interrupt Mask Control for Voltage channel data Ready Interrupt on INT pin (Default is 0)	
					0	Unmasked
					1	Masked
				D[3:2]	These two bits select the source of output 16-bit data in Normal mode from Voltage channel. Default is 01	
					00	FIR / MA Output
					01	CIC2 Output
					10	Dechop/Demod Output
					11	CIC Output
				D[1:0]	Reserved	
47	FIR CTL_REG_V	0000_0000	R/W	D[7]	This bit selects FIR / MA Filter in Voltage channel. Default is 0 (FIR)	
					0	FIR
					1	MA Filter
				D[6:3]	These bits select the number of data samples for averaging in MA filter in Voltage channel. Default is 0000 (bypass)	
					0000	bypass
					0001	1
					0011	3
					0111	7
					1111	15
				D[2:0]	Reserved	

Note: All the registers from address 0x19 to 0x2C are read-only.

10 Application Information

Figure 32. Application Diagram



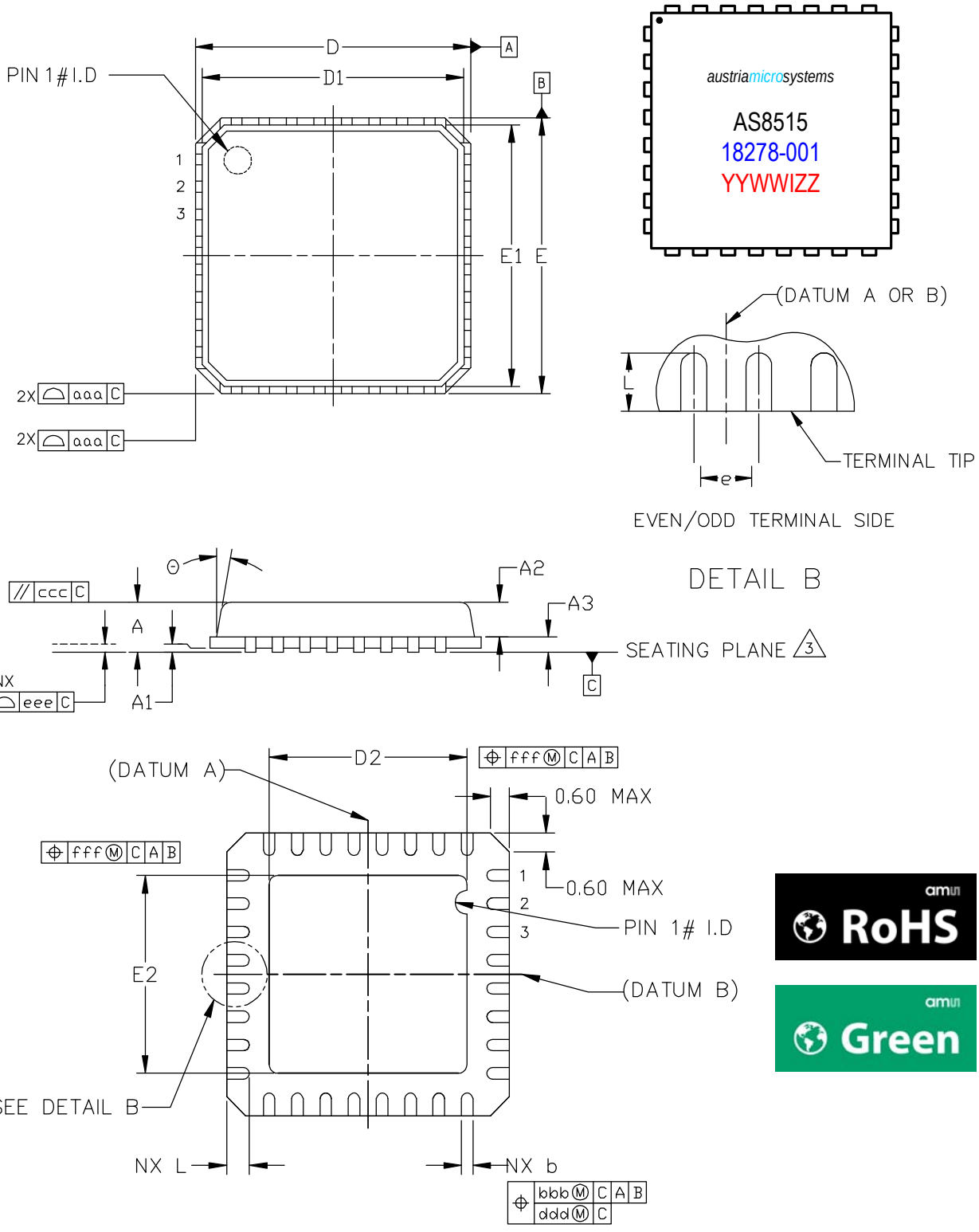
Note: VSENSE_IN, VSENSE_GND, MEN, and CHOP_CLK should be left unconnected.

Note: Keep the differential input signal lines short, symmetric, and as close as possible. Use of PCB shielding layers is recommended, but consider Eddy currents for fast changes in shunt current and related parasitic signal / ground shift generation.

11 Package Drawings and Markings

The devices are available in a 32-pin MLF (5x5 mm) package.

Figure 33. Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.30	0.40	0.50
θ	0°	-	14°
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D1		4.75 BSC	
E1		4.75 BSC	

Symbol	Min	Nom	Max
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M -1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Bilateral coplanarity zone applies to the exposed pad as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Marking: YYWWIZZ.

YY	WW	I	ZZ
Last two digits of the manufacturing year	Manufacturing Week	Plant Identifier	Traceability Code

Revision History

Revision	Date	Owner	Description
0.1	Dec 16, 2011	zmo/mbr	Initial draft
0.2	Jan 25, 2012	zmo	Updated table information on LIN Driver (page 23) Pins 10, 11 updated in the file (Pin Assignments, Figure 32)
0.3	Mar 07, 2012		Updated power dissipation info in Absolute Maximum Ratings (page 7)
0.4	Aug 14, 2012		Updated Table 14, Figure 32.
0.5	Nov 22, 2012	zmo/mbr	Updated Operating Conditions, Electrical Characteristics, Ordering Information, Figure 12. Table 27, Table 29, Table 30, Table 42.

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 47.

Table 47. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS8515-ZMFP	Data acquisition system with power management and LIN transceiver	Tape & Reel (5000 pcs)	32-pin MLF (5x5 mm)
AS8515-ZMFM		Tape & Reel (500 pcs)	

Note: All products are RoHS compliant and ams green.
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For further information and requests, please contact us mailto: sales@ams.com
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