AS5311

High Resolution Magnetic Linear Encoder

Preliminary Data Sheet

1 General Description

The AS5311 is a contactless high resolution magnetic linear encoder for accurate linear motion and off-axis rotary sensing with a resolution down to <0.5µm. It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing on a single chip, packaged in a small 20-pin TSSOP package.

A multi-pole magnetic strip or ring with a pole length of 1.0mm is required to sense the rotational or linear motion. The magnetic strip is placed above the IC at a distance of typ. 0.3mm.

The absolute measurement provides instant indication of the magnet position within one pole pair with a resolution of 488nm per step (12-bit over 2.0mm). This digital data is available as a serial bit stream and as a PWM signal.

Furthermore, an incremental output is available with a resolution of 1.95 µm per step. An index pulse is generated once for every pole pair (once per 2.0mm).The travelling speed in incremental mode is up to 650mm/second.

An internal voltage regulator allows the AS5311 to operate at either 3.3 V or 5 V supplies.

Depending on the application the AS5311 accepts multi-pole strip magnets as well as multi-pole ring magnets, both radial and axial magnetized (see Figure 1 and Figure 3).

The AS5311 is available in a Pb-free TSSOP-20 package and qualified for an ambient temperature range from -40°C to +125°C.

2 Key Features

- Two 12-bit digital absolute outputs :
  - Serial interface and
  - Pulse width modulated (PWM) output
- Incremental output with Index
- “red-yellow-green” indicators monitor magnet placement over the chip

3 Applications

- Micro-Actuator feedback
- Servo drive feedback
- Robotics
- Replacement of optical encoders

Figure 1. AS5311 with Multi-pole Magnetic Strip for Linear Motion Sensing

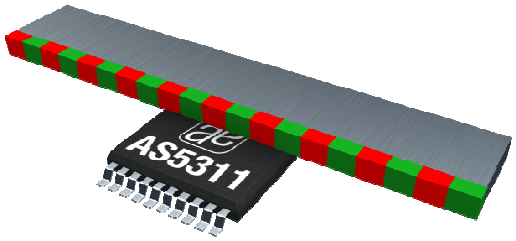


Figure 2. Block Diagram of AS5311

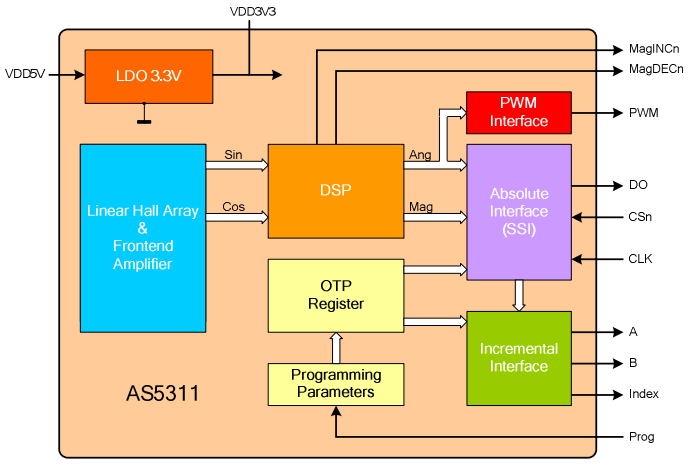
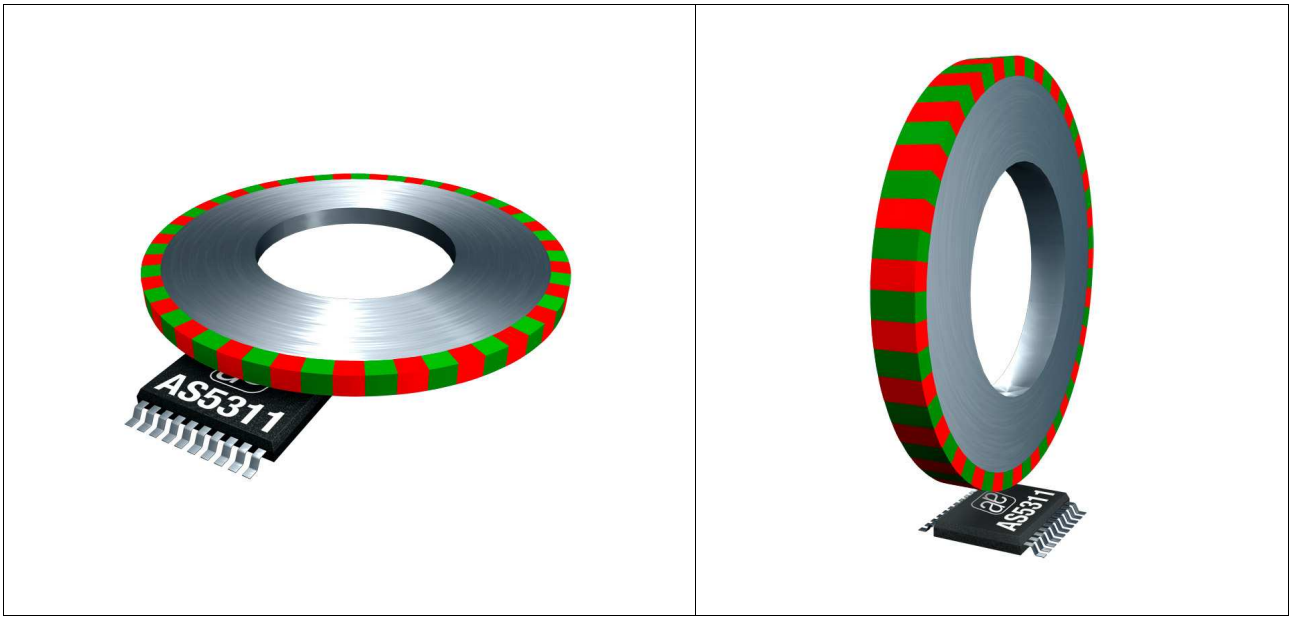


Figure 3. AS5311 with Multi-pole Ring Magnets for Off-axis Rotary Motion Sensing



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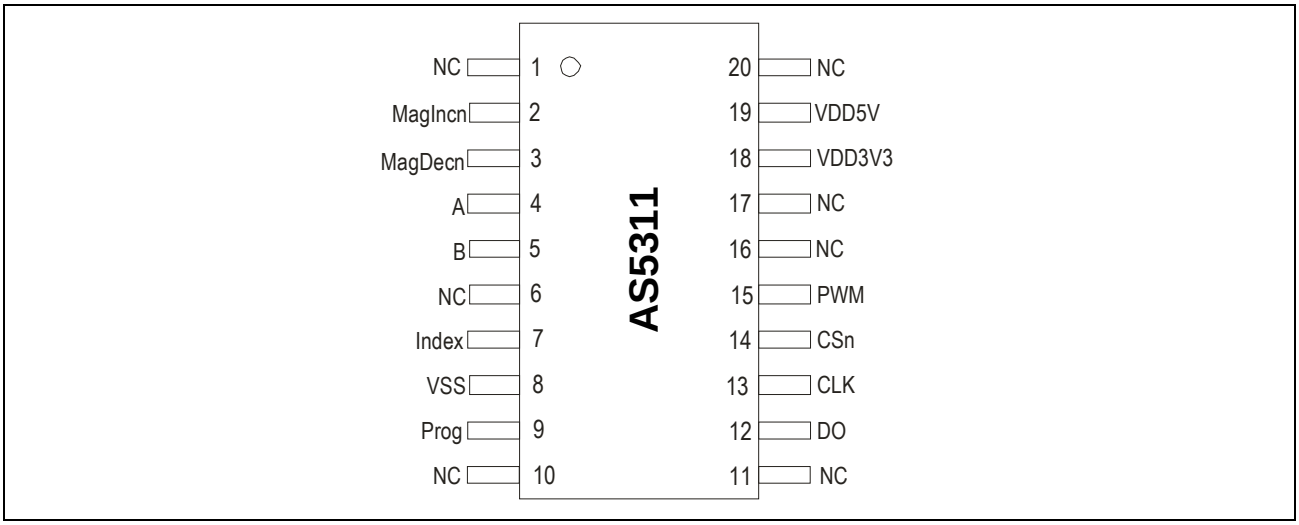
5 Pinout

5.1 Pin Assignments

Figure 4. AS5311 Pin Configuration, TSSOP-20



5.2 Pin Description

Pin 4(A), 5(B) and 7(Index) are the incremental outputs. The incremental output has a resolution of 10-bit per pole pair, resulting in a step length of 1.95µm.
Note that Pin 14 (CSn) must be low to enable the incremental outputs.

Pins 12, 13 and 14 are used for serial data transfer. Chip Select (CSn; active low) initiates serial data transfer. CLK is the clock input and DO is the data output. A logic high at CSn puts the data output pin (DO) to tri-state and terminates serial data transfer. CSn must be low to enable the incremental outputs. See 7.1.1 for further options.

Pin 8 is the supply ground pin. Pins 18 and 19 are the positive supply pins.
For 5V operation, connect the 5V supply to pin 19 and add a 2µ2…10µF buffer capacitor at pin 19.
For 3.3V operation, connect both pins 18 and 19 to the 3.3V supply.

Pin 9 is used for factory programming only. It should be connected to VSS.

Pins 2 and 3 are the magnetic field change indicators, MagINCn and MagDECn (magnetic field strength increase or decrease through variation of the distance between the magnet and the device). These outputs can be used to detect the valid magnetic field range.
External pull-up resistors are required at these pins. See 6.3.2 for maximum output currents on these pins. Since they are open-drain outputs they can also be combined (wired-and).

Pin 15 (PWM) allows a single wire output of the 12-bit absolute position value within one pole pair (2.0mm). The value is encoded into a pulse width modulated signal with 1µs pulse width per step (1µs to 4097µs over one pole pair).

Pins 6, 10, 11, 16, 17 and 20 are for internal use and must not be connected.

Table 1. Pin Description

Pin	Symbol	Type	Description
1	NC	-	Must be left unconnected
2	MagINCn	DO_OD	Magnet Field **Mag**nitude **INC**rease; active low, indicates a distance reduction between the magnet and the device surface.
3	MagDECn	DO_OD	Magnet Field **Mag**nitude **DEC**rease; active low, indicates a distance increase between the device and the magnet.
4	A	DO	Incremental output A
5	B	DO	Incremental output B
6	NC	-	Must be left unconnected
7	Index	DO	Incremental output Index.
8	VSS	S	Negative Supply Voltage (GND)
9	Prog	DI_PD	OTP **Prog**ramming Input for factory programming. Connect to VSS
10	NC	-	Must be left unconnected
11	NC	-	Must be left unconnected
12	DO	DO_T	**D**ata **O**utput of Synchronous Serial Interface
13	CLK	DI, ST	**Cl**oc**k** Input of Synchronous Serial Interface; Schmitt-Trigger input
14	CSn	DI_PU, ST	**C**hip **S**elect, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ). Must be low to enable incremental outputs
15	PWM	DO	**P**ulse **W**idth **M**odulation of approx. 244Hz; 1µs/step
16	NC	-	Must be left unconnected
17	NC	-	Must be left unconnected
18	VDD3V3	S	3V-Regulator output; internally regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
19	VDD5V	S	Positive Supply Voltage, 3.0 to 5.5 V
20	NC	-	Must be left unconnected

DO_OD	digital output open drain	S	supply pin
DO	digital output	DI	digital input
DI_PD	digital input pull-down	DO_T	digital output /tri-state
DI_PU	digital input pull-up	ST	Schmitt-Trigger input

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comments
DC supply voltage at pin VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3		5	V	
Input pin voltage	-0.3	VDD5V +0.3	V	Except VDD3V3
Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge		± 2	kV	Norm: MIL 883 E method 3015
Storage temperature	-55	125	℃	Min – 67℉ ; Max +257 ℉

Parameter	Min	Max	Unit	Comments
Body temperature (Lead-free package)		260	℃	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn “matte tin”
Humidity non-condensing	5	85	%	

6.2 Operating Conditions

Table 3. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Ambient temperature	Tamb	-40		125	℃	-40℉…+257℉
Supply current	Isupp		16	21	mA	
Supply voltage at pin VDD5V Voltage regulator output voltage at pin VDD3V3	VDD5V VDD3V3	4.5 3.0	5.0 3.3	5.5 3.6	V V	5V Operation
Supply voltage at pin VDD5V Supply voltage at pin VDD3V3	VDD5V VDD3V3	3.0 3.0	3.3 3.3	3.6 3.6	V V	3.3V Operation (pin VDD5V and VDD3V3 connected)

6.3 DC Characteristics for Digital Inputs and Outputs

6.3.1 CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = internal Pull-up)

Operating conditions: T_{amb} = -40 to +125℃, VDD5V = 3.0-3.6V (3V operation) VD D5V = 4.5-5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	VIH	0.41 * VDD5V		V	Normal operation
Low level input voltage	VIL		0.13 * VDD5V	V	
Schmitt Trigger hysteresis	VIon - VIoff	1		V	
Input leakage current	ILEAK	-1	1	µA	CLK only
Pull-up low level input current	IiL	-30	-100		CSn only, VDD5V: 5.0V

6.3.2 CMOS Output Open Drain: MagINCn, MagDECn

Operating conditions: T_{amb} = -40 to +125℃, VDD5V = 3.0-3.6V (3V operation) VD D5V = 4.5-5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Max	Unit	Note
Low level output voltage	VOL		VSS+0.4	V	
Output current	IO		4 2	mA	VDD5V: 4.5V VDD5V: 3V
Open drain leakage current	IOZ		1	µA	

6.3.3 CMOS Output: PWM

Operating conditions: T_{amb} = -40 to +125℃, VDD5V = 3.0-3.6V (3V operation) VD D5V = 4.5-5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	VOH	VDD5V-0.5		V	
Low level output voltage	VOL		VSS+0.4	V	
Output current	IO		4 2	mA mA	VDD5V: 4.5V VDD5V: 3V

6.3.4 Tristate CMOS Output: DO

Operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VD D5V = 4.5-5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	VOH	VDD5V –0.5		V	
Low level output voltage	VOL		VSS+0.4	V	
Output current	IO		4	mA	VDD5V: 4.5V
			2	mA	VDD5V: 3V

6.4 Magnetic Input Specification

Operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VD D5V = 4.5 - 5.5V (5V operation) unless otherwise noted.
Two-pole cylindrical diametrically magnetised source:

Parameter	Symbol	Min	Typ	Max	Unit	Note
Pole length	Lp		1		mm	Recommended magnet: plastic or rubber bonded ferrite or NdFeB
Pole pair length	t_{mag}		2		mm	
Magnetic input field amplitude	B_{pk}	10		40	mT	Required vertical component of the magnetic field strength on the die's surface
Magnetic offset	B_{off}			± 5	mT	Constant magnetic stray field
Magnetic field temperature drift	B_{tc}			0.2	%/K	Recommended magnet: plastic or rubber bonded ferrite or NdFeB
Magnetic input field variation				±2	%	Including offset gradient
Linear travelling speed	Vabs			650	mm/ sec	Incremental output: 1024 steps / polepair including interpolation [1)]
Displacement	Disp		0.5		mm	Max. shift between defined Hall sensor center and magnet centerline (see Figure 17); depends on magnet geometries
Vertical gap	Z_{Dist}		0.3		mm	Package to magnet surface; depends on magnet strength
Recommended magnet material and temperature drift			-0.19		%/K	Plastic or rubber bonded Ferrite
			-0.12			Plastic or rubber bonded Neodymium (NdFeB)

Note [1)]: There is no upper speed limit for the absolute outputs. With increasing speed, the distance between two samples increases. The travelling distance between two subsequent samples can be calculated as:

$$sampling\_dist = \frac{v}{fs}$$

where: sampling_distance = travelling distance between samples in mm
v = travelling speed in mm/sec
fs = sampling rate in Hz (see 6.5 below)

6.5 Electrical System Specifications

Operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0~3.6V (3V operation) VD D5V = 4.5~5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution, absolute outputs	RES_{abs}		12		bit / polepair	0.488 um/step (12bit / 2mm pole pair)
Resolution, incremental outputs	RES_{inc}		10		bit / polepair	1.95 um/step (10bit / 2mm pole pair)
Integral non-linearity (optimum)	INL_{opt}			± 5.6	µm	Maximum error with respect to the best line fit. Ideal magnet T_{amb} =25 °C.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Integral non-linearity (over temperature)	INL_{temp}			± 10	µm	Maximum error with respect to the best line fit. Ideal magnet T_{amb} = -30 to +70 ℃.
Differential non-linearity	DNL			±0.97	µm	10bit, no missing codes
Transition noise	TN			0.6	µm RMS	1 sigma
Power-on reset thresholds On voltage; 300mV typ. hysteresis Off voltage; 300mV typ. hysteresis	 V_{on} V_{off}	 1.37 1.08	 2.2 1.9	 2.9 2.6	V	 DC supply voltage 3.3V (VDD3V3) DC supply voltage 3.3V (VDD3V3)
Power-up time	t_{PwrUp}			20	ms	Until status bit OCF = 1
System propagation delay absolute output :	t_{delay}			96	µs	Delay of ADC, DSP and absolute interface
System propagation delay incremental output	t_{delay}			384	µs	Including interpolation delay at high speeds
Internal sampling rate for absolute output	f_S	9.90	10.42	10.94	kHz	T_{amb} = 25℃
		9.38	10.42	11.46		T_{amb} = -40 to +125℃,
Hysteresis, incremental outputs	Hyst		2		LSB	No Hysteresis at absolute serial outputs
Read-out frequency	CLK			1	MHz	Max. clock frequency to read out serial data

Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.
Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.
Transition Noise (TN) is the repeatability of an indicated position.

6.6 Timing Characteristics

6.6.1 Synchronous Serial Interface (SSI)

Operating conditions: T_{amb} = -40 to +125℃, VDD5V = 3.0~3.6V (3V operation) VD D5V = 4.5~5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data output activated (logic high)	t DO active			100	ns	Time between falling edge of CSn and data output activated
First data shifted to output register	tCLK FE	500			ns	Time between falling edge of CSn and first falling edge of CLK
Start of data output	T CLK / 2	500			ns	Rising edge of CLK shifts out one bit at a time
Data output valid	t DO valid			413	ns	Time between rising edge of CLK and data output valid
Data output tristate	t DO tristate			100	ns	After the last bit DO changes back to “tristate”
Pulse width of CSn	t CSn	500			ns	CSn = high; To initiate read-out of next angular position
Read-out frequency	fCLK	>0		1	MHz	Clock frequency to read out serial data

6.6.2 Pulse Width Modulation Output

Operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0~3.6V (3V operation) VD D5V = 4.5~5.5V (5V operation) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Note
PWM frequency	f PWM	232	244	256	Hz	Signal period = 4098µs ±5% at Tamb = 25°C
		220	244	268		= 4098µs ±10% at Tamb = -40 to +125°C
Minimum pulse width	PW MIN	0.9	1	1.1	µs	Position 0d =0µm
Maximum pulse width	PW MAX	3892	4097	4301	µs	Position 4095d = 1999.5µm

7 Detailed Description

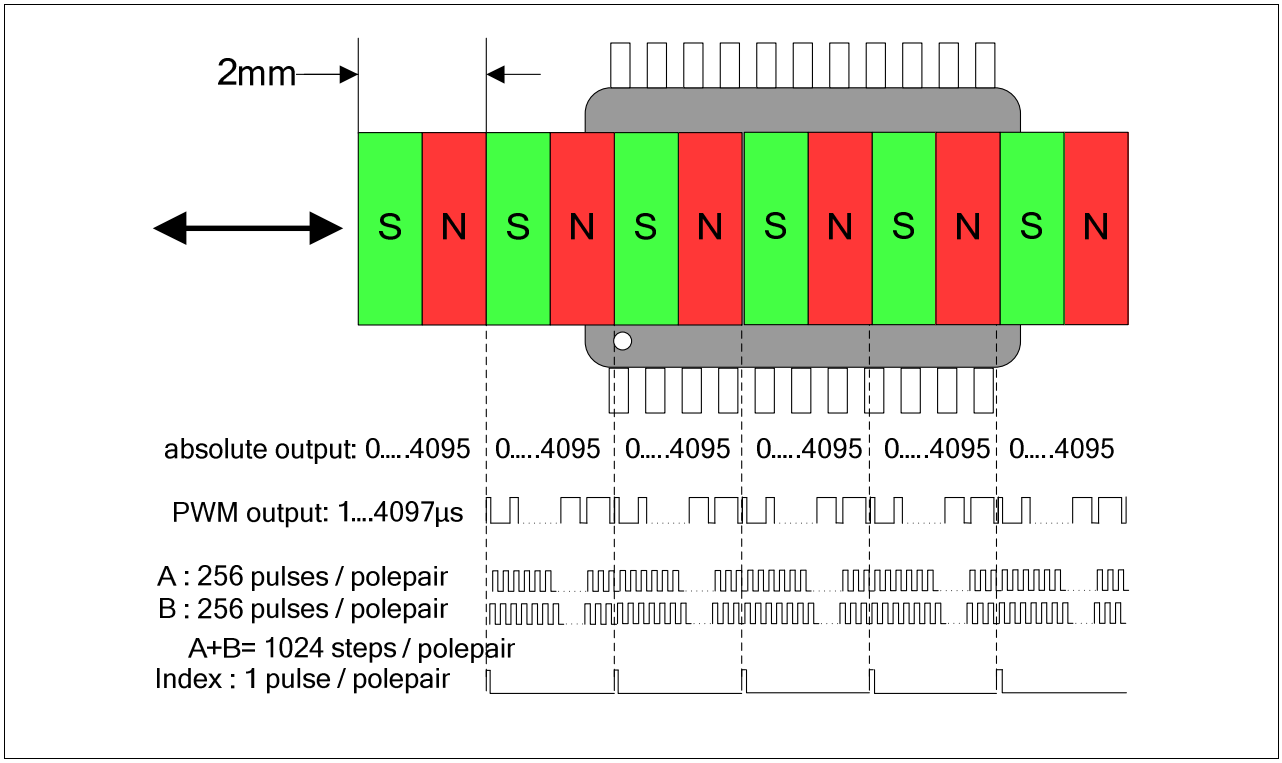
The different types of outputs relative to the magnet position are outlined in Figure 5 below. The absolute serial output counts from 0….4095 within one pole pair and repeats with each subsequent pole pair.

Likewise, the PWM output starts with a pulse width of 1µs, increases the pulse width with every step of 0.488µm and reaches a maximum pulse width of 4097µs at the end of each pole pair.

An index pulse is generated once for every pole pair.

256 incremental pulses are generated at each output A and B for every pole pair. The outputs A and B are phase shifted by 90 electrical degrees, which results in 1024 edges per pole pair. As the incremental outputs are also repeated with every pole pair, a constant train of pulses is generated as the magnet moves over the chip.

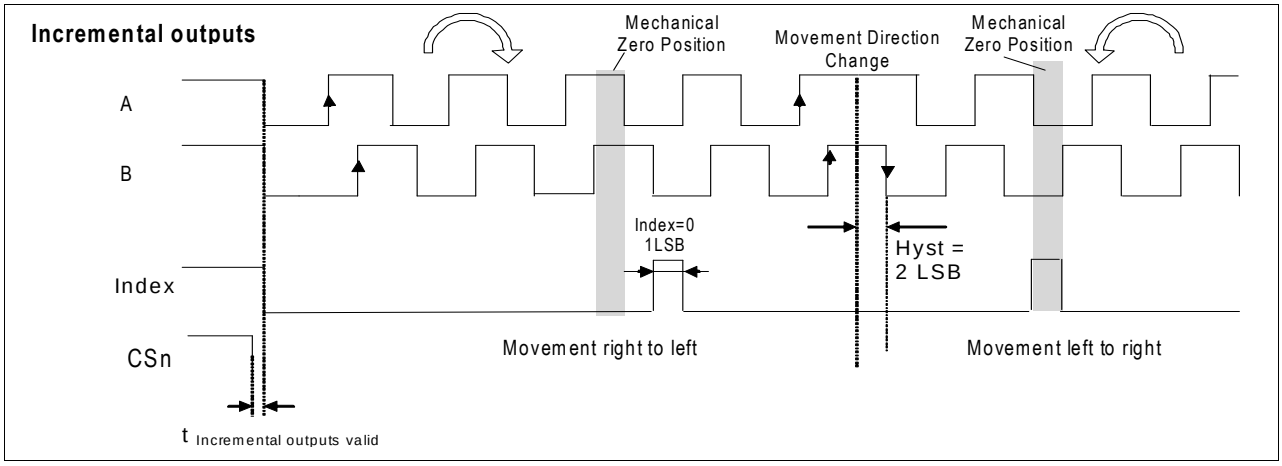
Figure 5. AS5311 Outputs Relative to Magnet Position



7.1 Incremental Outputs

Figure 6 shows the two-channel quadrature output of the AS5311. Output A leads output B when the magnet is moving from right to left and output B leads output A when the magnet is moving from left to right (see Figure 14).

Figure 6. Incremental Outputs



7.1.1 Incremental Power-up Lock Option

After power-up, the incremental outputs can optionally be locked or unlocked, depending on the status of the CSn pin:

CSn = low at power-up:

CSn has an internal pull-up resistor and must be externally pulled low ($R_{ext} \leq 5k\Omega$). If Csn is low at power-up, the incremental outputs A, B and Index will be high until the internal offset compensation is finished.

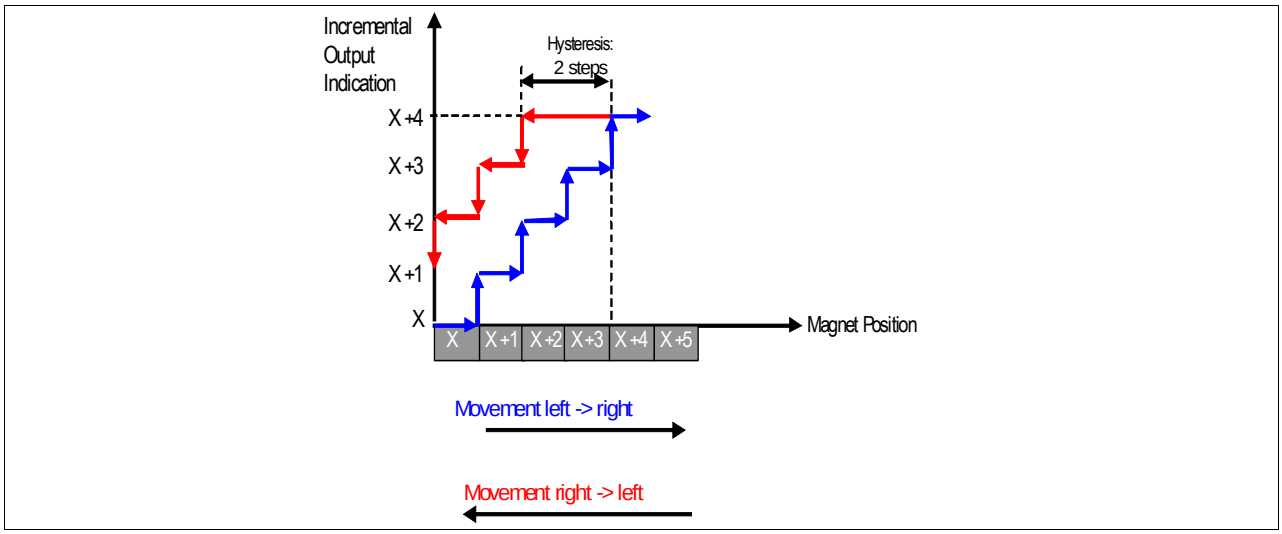
This unique state may be used as an indicator for the external controller to shorten the waiting time at power-up. Instead of waiting for the specified maximum power up-time (see 6.5), the controller can start requesting data from the AS5311 as soon as the state (A=B=Index = high) is cleared.

CSn = high or open at power-up:

In this mode, the incremental outputs (A, B, Index) will remain at logic high state, until CSn goes low or a low pulse is applied at CSn. This mode allows intentional disabling of the incremental outputs until for example the system microcontroller is ready to receive data.

7.2 Incremental Output Hysteresis

Figure 7. Hysteresis Illustration

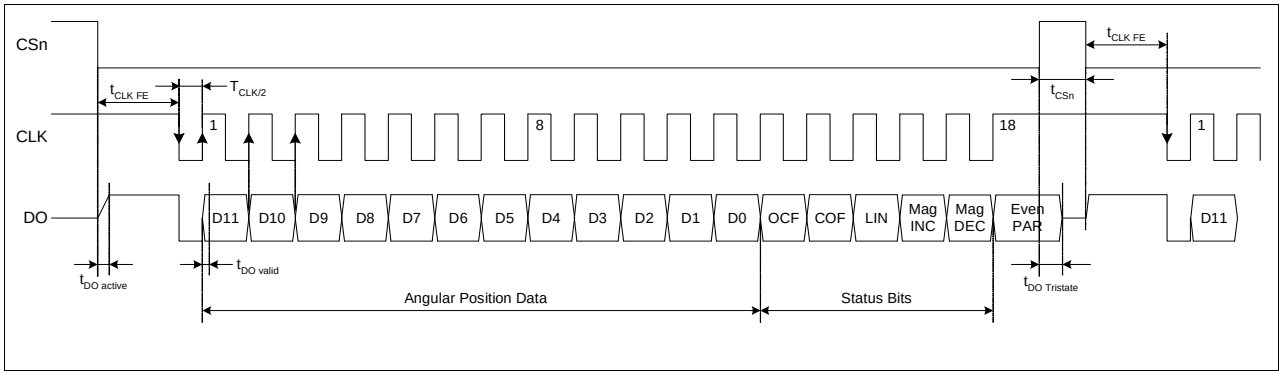


To avoid flickering incremental outputs at a stationary magnet position, a hysteresis is introduced.
In case of a movement direction change, the incremental outputs have a hysteresis of 2 LSB. For constant movement directions, every magnet position change is indicated at the incremental outputs (see Figure 6). If for example the magnet moves from position „x+3“ to „x+4“, the incremental output would also indicate this position accordingly.
A change of the magnet's movement direction back to position „x+3“ means, that the incremental output still remains unchanged for the duration of 2 LSB, until position „x+2“ is reached. Following this movement, the incremental outputs will again be updated with every change of the magnet position.

7.3 Synchronous Serial Interface (SSI)

The Serial interface allows data transmission of the 12-bit absolute linear position information (within one pole pair = 2.0mm). Data bits D11:D0 represent the position information with a resolution of 488nm (2000µm / 4096) per step.
CLK must be high at the falling edge of CSn.

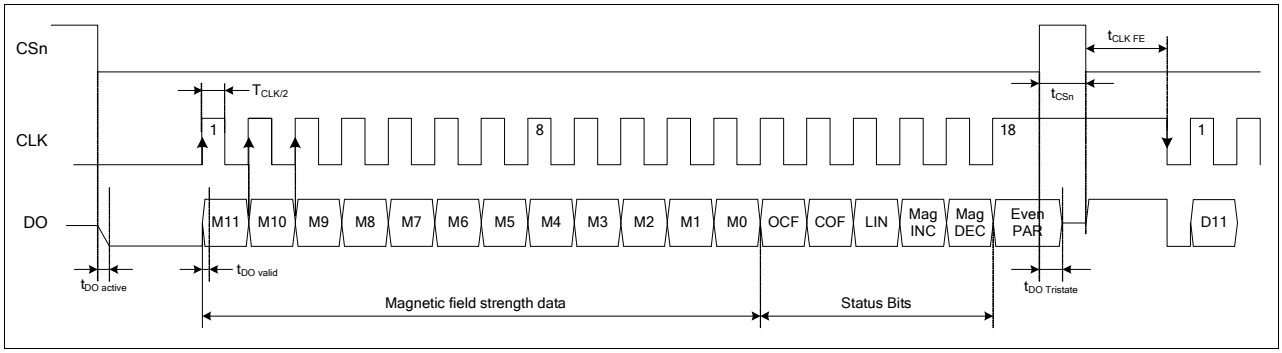
Figure 8. Synchronous Serial Interface with Absolute Angular Position Data



If CLK is low at the falling edge of CSn, the first 12 bits represent the magnitude information, which is proportional to the magnetic field strength. This information can be used to detect the presence and proper distance of the magnetic strip by comparing it to a known good value (depends on the magnet material and distance).
The automatic gain control (AGC) maintains a constant MAGnitude value of 3F hex (="green" range). If the MAG value is <>3F hex, the AGC is out of the regulating range ("yellow" or "red" range). See Table 5 for more details.

A value of zero or close to zero indicates a missing magnet.

Figure 9. Synchronous Serial Interface with Magnetic Field Strength Data



If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time $t_{CLK\ FE,}$ data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 18 bits, if CLK is high at the falling edge of CSn (Figure 8), the first 12 bits are the absolute distance information D[11:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease).
- If CLK is low at the falling edge of CSn (Figure 9), the first 12 bits contain the magnitude information (range = 00…7F hex) and the subsequent bits contain the status bits (see above)
- A subsequent measurement is initiated by a “high” pulse at CSn with a minimum duration of t_{CSn}.

7.3.1 Data Contents

D11:D0 absolute linear position data (MSB is clocked out first)

M11:M0 magnitude / magnetic field strength information (MSB is clocked out first)

OCF (**O**ffset **C**ompensation **F**inished), logic high indicates the finished Offset Compensation Algorithm

COF (**C**ordic **O**verflow), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D11:D0 (likewise M11:M0) is invalid.
This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN (**Lin**earity Alarm), logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D11:D0 may still be used, but can contain invalid data. This warning can be resolved by increasing the magnetic field strength.

Even Parity bit for transmission error detection of bits 1…17 (D11…D0, OCF, COF, LIN, MagINC, MagDEC)

Data D11:D0 is valid, when the status bits have the following configurations:

Table 4. Status Bit Outputs

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	even checksum of bits 1:17
			0	1	
			1	0	
			1*)	1*)	

*) MagInc=MagDec=1 is only recommended in YELLOW mode (see Table 5)

7.4 Absolute Output Jitter and Hysteresis

Note that there is no hysteresis or additional filtering at the absolute output. This allows a determination of the magnet's absolute position within one pole pair down to submicron range.
Due to the intentionally omitted hysteresis and due to noise (e.g. from weak magnetic fields), the absolute output may jitter when the magnet is stationary over the chip.
In order to get a stable 12-bit absolute reading, two common methods may be implemented to reduce the jitter.

7.4.1 Adding a Digital Hysteresis

The hysteresis feature of the incremental outputs is described in 7.2. An equivalent function can be implemented in the software of the external microcontroller. The hysteresis should be larger than the peak-to-peak noise (=jitter) of the absolute output in order to mask it and create a stable output reading.
Remark: the 2-bit hysteresis on the incremental output (=3.9µm) is equivalent to a hysteresis of 8LSB on the absolute output.

7.4.2 Implementing Digital Filtering

Another useful alternative or additional method to reduce jitter is digital filtering. This can be accomplished simply by averaging, for example a moving average calculation in the external microcontroller. Averaging 4 readings results in 6dB (=50%) noise and jitter reduction. An average of 16 readings reduces the jitter by a factor of 4.
Averaging causes additional latency of the processed data. Therefore it may be useful to adjust the depth of averaging depending on speed of travel. For example using a larger depth when the magnet is stationary and reducing the depth when the magnet is in motion.

7.5 Z-axis Range Indication ("Red/Yellow/Green" Indicator)

The AS5311 provides several options of detecting the magnet distance by indicating the strength of the magnetic field. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins 1 and 2) and as status bits in the serial data stream (see Figure 8). Additionally the LIN status bit indicates the non-recommended "red" range. The MAGnitude register provides additional information about the strength of the magnetic field (see Figure 9).
The digital status bits MagINC, MagDec, LIN and the hardware pins MagINCn, MagDECn have the following function:

Table 5. Magnetic Field Strength Red-Yellow-Green Indicators

Status Bits			MAG	Hardware Pins		
Mag INC	Mag DEC	LIN	M11.. M0	Mag INCn	Mag DECn	Description
0	0	0	3F hex	Off	Off	No distance change Magnetic input field OK (GREEN range, ~10…40mT peak amplitude)
0	1	0	3F hex	Off	Off	Distance increase; this state is a dynamic state and only active while the magnet is moving away from the chip. Magnitude register may change but regulates back to 3F hex.
1	0	0	3F hex	Off	Off	Distance decrease; this state is a dynamic state and only active while the magnet is moving towards the chip. Magnitude register may change but regulates back to 3F hex.
1	1	0	20 hex-5F hex	On	Off	YELLOW range: magnetic field is ~3.4….54.5mT. The AS5311 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	<20 hex >5F hex	On	On	RED range: magnetic field is <3.4mT (MAG <20) or >54.5mT (MAG >5F). It is still possible to operate the AS5311 in the red range, but not recommended.
All other combinations				n/a	n/a	Not available

8 Pulse Width Modulation (PWM) Output

The AS5311 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the relative linear position of the magnet within one pole pair (2.0mm). This cycle repeats after every subsequent pole pair:

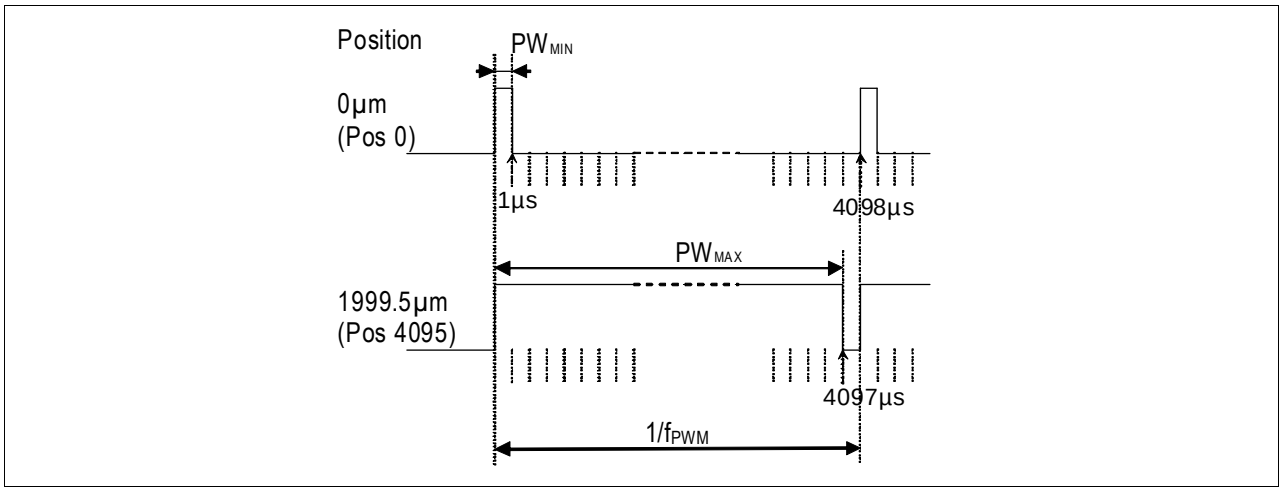
$$Position = \frac{t_{on} \cdot 4098}{(t_{on} + t_{off})} - 1$$

for digital position = 0 – 4094

Exception: A linear position of 1999.5µm = digital position 4095
will generate a pulse width of t_{on} = 4097µs and a pause t_{off} = 1µs

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be cancelled by measuring the complete duty cycle as shown above.

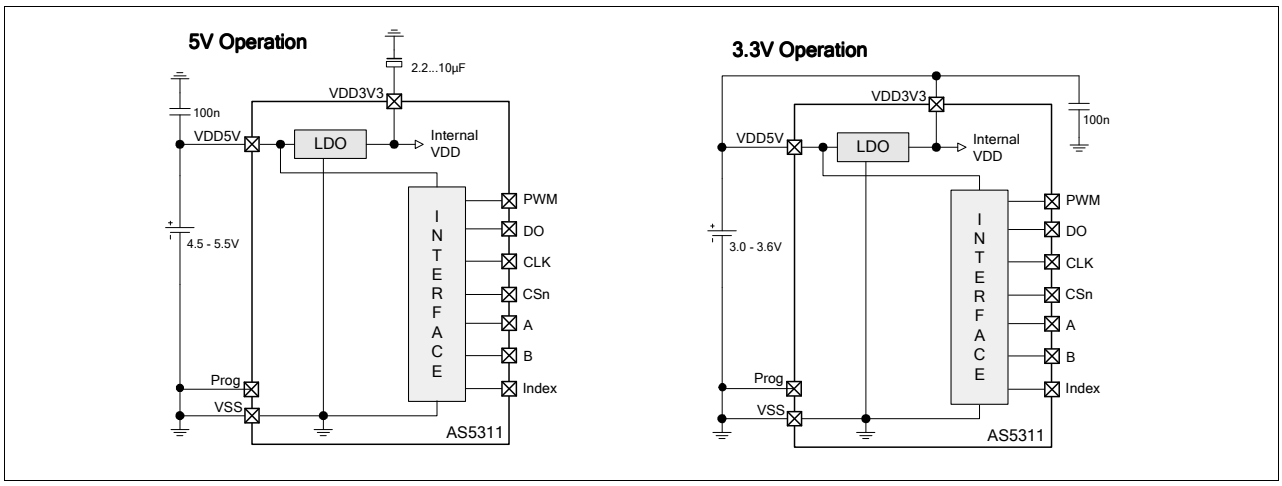
Figure 10. PWM Output Signal



9 3.3V / 5V Operation

The AS5311 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The internal supply voltage is always taken from the output of the LDO, meaning that the internal blocks are always operating at 3.3V.
For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 11).
For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 2.2...10µF capacitor, which is supposed to be placed close to the supply pin.
The VDD3V3 output is intended for internal use only It must not be loaded with an external load.
The output voltage of the digital interface I/O's corresponds to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin.
A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

Figure 11. Connections for 5V and 3.3V Supply Voltages



10 Magnet Specifications

10.1 Magnetization

The AS5311 accepts magnetic multi-pole strip or ring magnets with a pole length of 1.0mm. Recommended magnet materials include plastic or rubber bonded ferrite or Neodymium magnets.
It is not recommended to use the AS5311 with other pole lengths as this will create additional nonlinearities.

Figure 12. Additional Error from Pole Length Mismatch

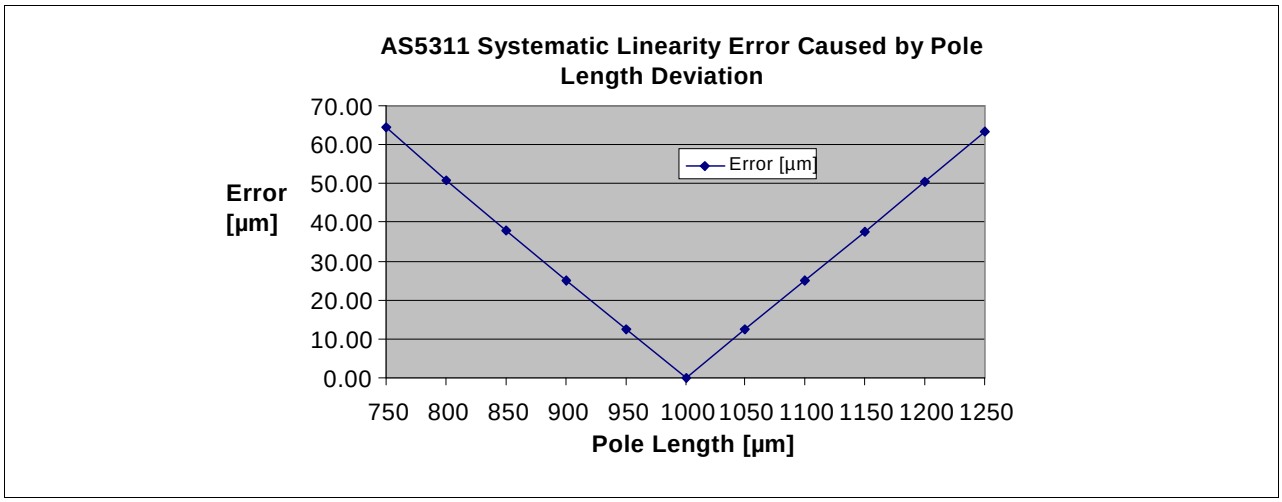


Figure 12 shows the error caused by a mismatch of pole length. Note that this error is an additional error on top of the chip-internal INL and DNL errors (see 6.5). For example, when using a multi-pole magnet with 1.2mm pole length instead of 1.0mm, the AS5311 will provide 1024 incremental steps or 4096 absolute positions over 2.4mm, but with an additional linearity error of up to 50µm.
The curvature of ring magnets may cause linearity errors as well due to the fact that the Hall array on the chip is a straight line while the poles on the multi-pole ring are curved. These errors decrease with increasing ring diameter. It is therefore recommended to keep the ring diameter measured at the location of the Hall array at 20mm or higher.

10.2 Position of the Index Pulse

An index pulse is generated when the North and South poles are placed over the Hall array as shown in Figure 14.
The incremental output count increases when the magnet is moving to the left, facing the chip with pin#1 at the lower left corner (see Figure 14, top drawing). At the same time, the absolute position value increases.
Likewise, the position value decreases when the magnet is moved in the opposite direction.

10.3 Mounting the Magnet

10.3.1 Vertical Distance

As a rule of thumb, the gap between chip and magnet should be ½ of the pole length, that is Z=0.5mm for the 1.0mm pole length of the AS5311 magnets. However, the gap also depends on the strength of the magnet. Typical gaps for AS5311 magnets range from 0.3 to 0.6mm (see 6.4).
The AS5311 automatically adjusts for fluctuating magnet strength by using an automatic gain control (AGC). The vertical distance should be set such that the AS5311 is in the “green” range. See 7.5 for more details.

10.3.2 Alignment of Multi-pole Magnet and IC

When aligning the magnet strip or ring to the AS5311, the centerline of the magnet strip should be placed exactly over the Hall array. A lateral displacement in Y-direction (across the width of the magnet) is acceptable as long as it is within the active area of the magnet. See Figure 14 for the position of the Hall array relative to Pin #1.
Note: the active area in width is the area in which the magnetic field strength across the width of the magnet is constant with reference to the centerline of the magnet (see Figure 13).

10.3.3 Lateral stroke of Multi-pole Strip Magnets

The lateral movement range (stroke) is limited by the area at which all Hall sensors of the IC are covered by the magnet in either direction. The Hall array on the AS5311 has a length of 2.0mm, hence the total stroke is

maximum lateral Stroke = Length of active area – length of Hall array

Note: active area in length is defined as the area containing poles with the specified 1.0mm pole length. Shorter poles at either edge of the magnet must be excluded from the active area (see Figure 13).

Figure 13. Active Area of Strip Magnet

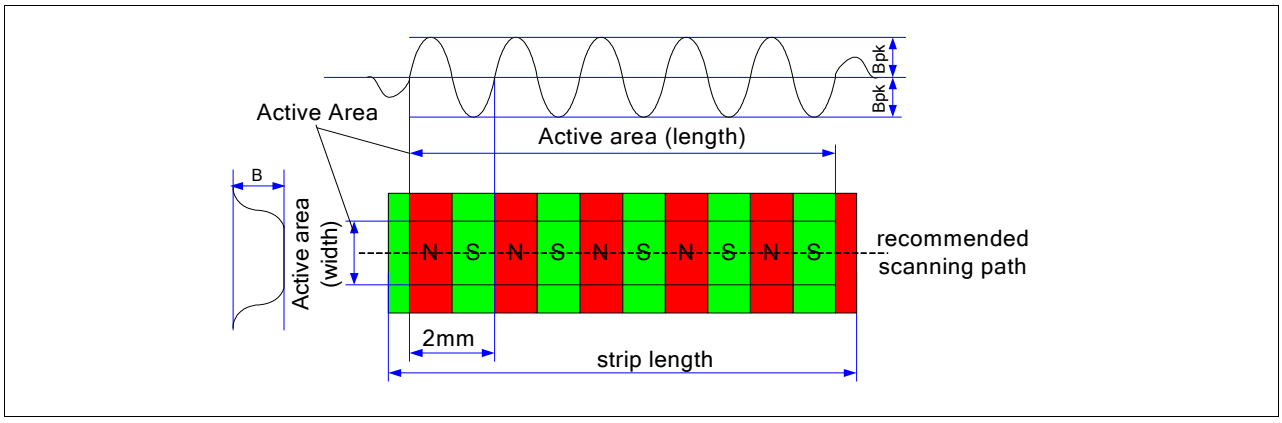
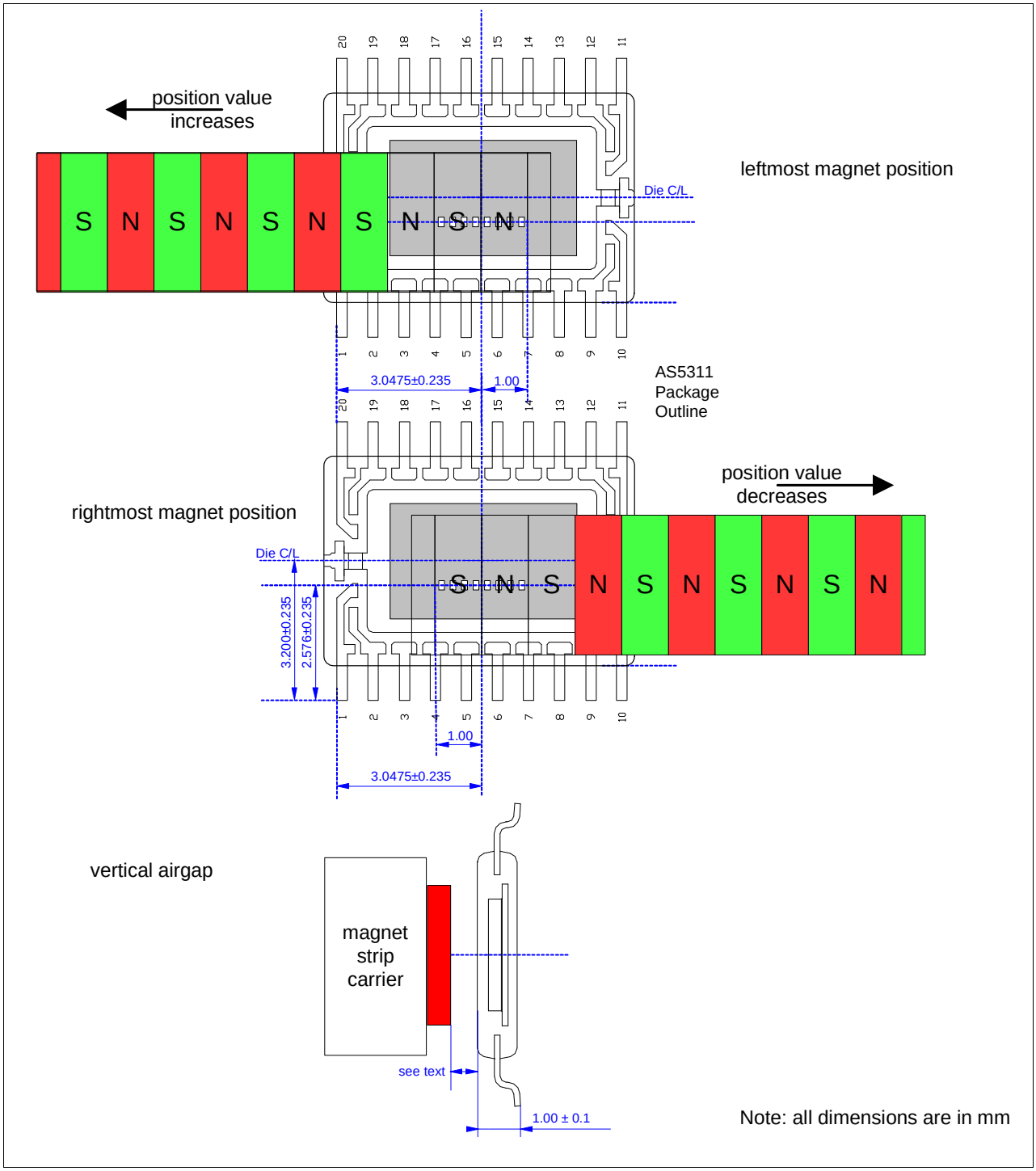


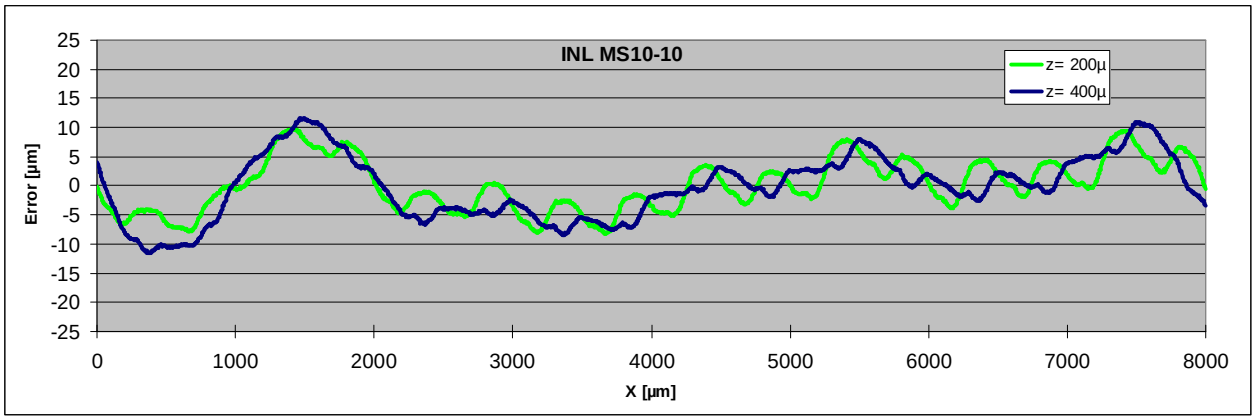
Figure 14. Alignment of Magnet Strip with AS5311 Sensor IC



11 Measurement Data Example

Figure 15 shows typical test results of the accuracy obtained by a commercially available multi-pole magnetic strip.
The graph shows the accuracy over a stroke of 8mm at two different vertical gaps, 0.2mm and 0.4mm. As displayed, the accuracy is virtually identical (about +/- 10µm) for both airgaps due to the automatic gain control of the AS5311 which compensates for airgap changes.
The accuracy depends greatly on the length and strength of each pole and hence from the precision of the tool used for magnetization as well as the homogeneity of the magnet material. As the error curve in the example below does not show a repetitive pattern for each pole pair (each 2.0mm), this is most likely an indication that the pole lengths of this particular sample do not exactly match. While the first pole pair (0...2mm) shows the greatest nonlinearities, the second pole (2…4mm) is very precise, etc…

Figure 15. Sample Test Results of INL at Different Airgaps

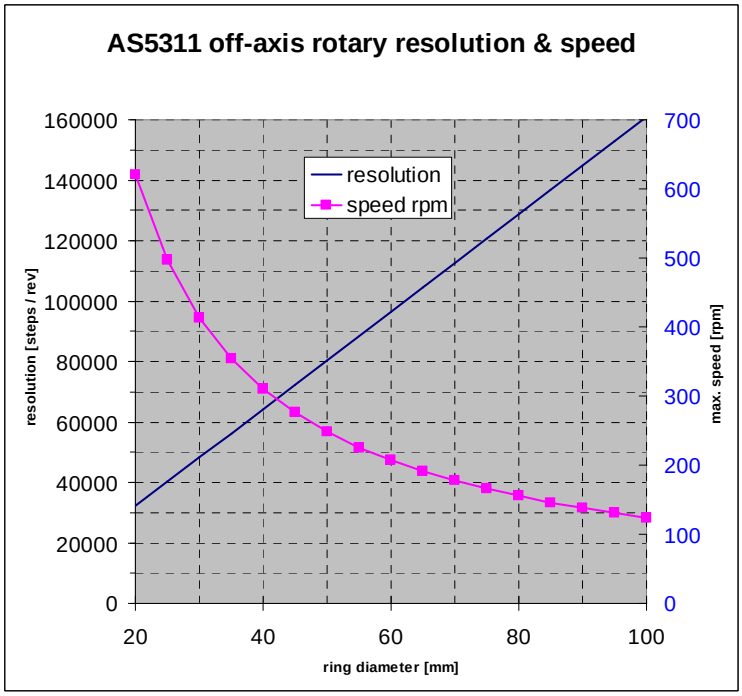


Note: The magnet sample used in Figure 15 is a 10-pole plastic bonded ferrite magnet as shown in Figure 13. The corresponding magnet datasheet (MS10-10) is available for download from the austriamicrosystems website, magnet samples can be ordered from the austriamicrosystems online web shop.

12 AS5311 Off-axis Rotary Applications

The AS5311 can also be used as an off-axis rotary encoder, as shown in Figure 3. In such applications, the multi-pole magnetic strip is replaced by a multi-pole magnetic ring. The ring can have radial or axial magnetization.

Figure 16. Angular Resolution and Maximum Speed versus Ring Diameter



In off-axis rotary applications, very high angular resolutions are possible with the AS5311.
The number of steps per revolution increases linearly with ring diameter.
Due to the increasing number of pulses per revolution, the maximum speed decreases with increasing ring diameter.

Example:
a magnetic ring with 41.7mm diameter has a resolution of 65536 steps per revolution (16-bit) and a maximum speed of 305 rpm

Res [bit]	Steps / Rev.	Ring Diameter [mm]	Max Speed [rpm]
15	32768	20.9	609
16	65536	41.7	305
17	131072	83.4	152

The number of incremental steps per revolution can be calculated as:

$$incremental\_steps = 1024 * nbr\_polepairs$$

$$incremental\_steps = \frac{1024 * d * \pi}{2}$$

Note that the circumference (d*π) must be a multiple of one polepair = 2mm, hence the diameter of the magnet ring may need to be adjusted accordingly:

$$d = \frac{nbr\_polepairs * 2mm}{\pi}$$

The maximum rotational speed can be calculated as:

$$\max\_rot\_speed = \frac{\max\_lin\_speed * 60}{d * \pi} = \frac{39000}{d * \pi}$$

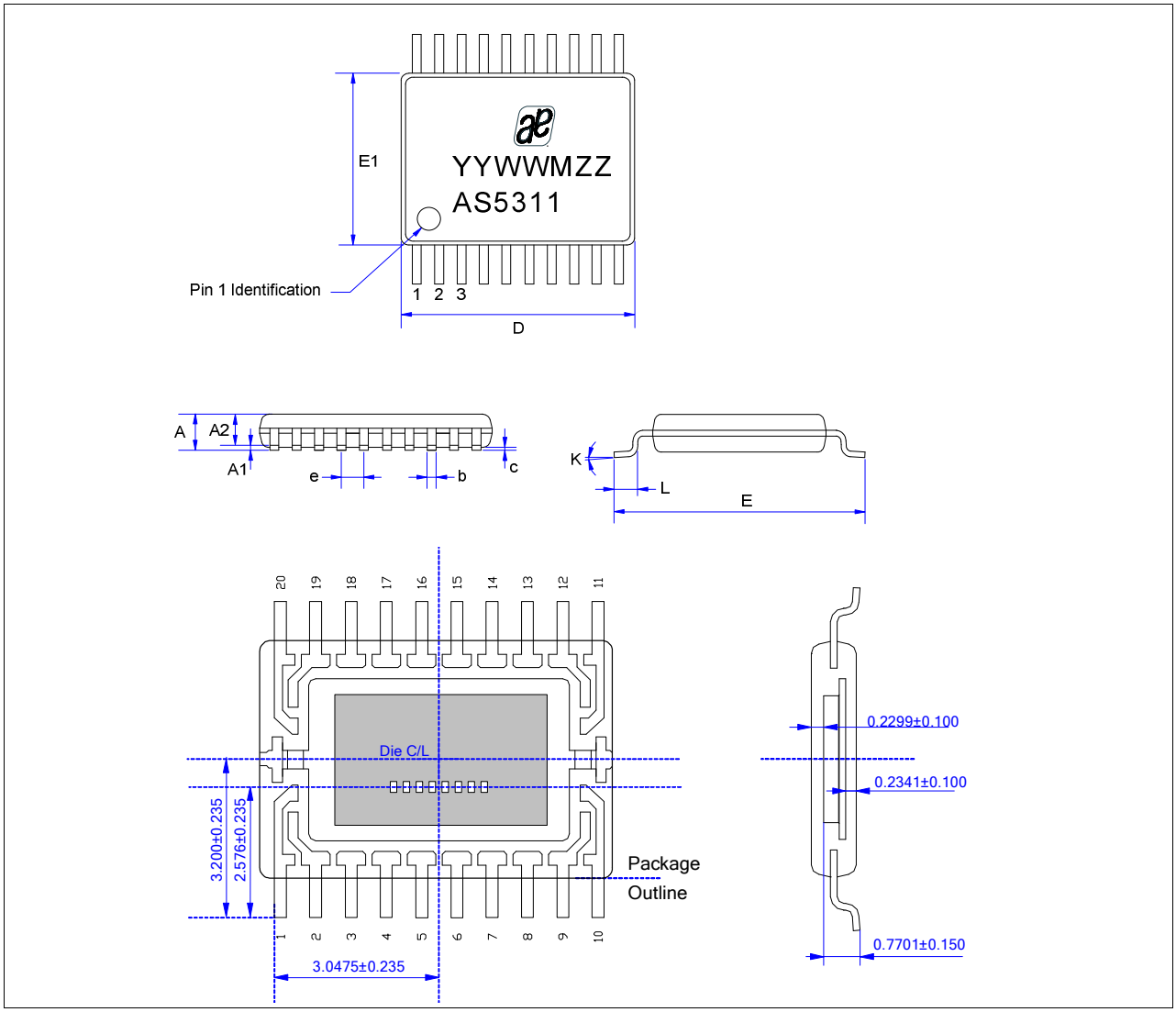
where nbr_polepairs = the number of pole pairs at the magnet ring
d = diameter of the ring in mm; the diameter is taken at the locus of the Hall elements underneath the magnet
max_rot_speed = maximum rotational speed in revolutions per minute rpm :
max_lin_speed = maximum linear speed in mm/sec (=650 mm/s for AS5311)

Note: further examples are shown in the “Magnet Selection Guide”, available for download from the austriamicrosystems website
http://www.austriamicrosystems.com/eng/Products/Magnetic-Encoders/Linear-Encoders

13 Package Drawings and Marking

20 Lead Thin Shrink Small Outline Package – **TSSOP20**

Figure 17. AS5311 Package Dimensions and Hall Array Location



Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.10	-	-	0.043
A1	0.05	-	0.15	0.002	-	0.006
A2	0.85	0.90	0.95	0.033	0.035	0.037
b	0.19	-	0.30	0.007	-	0.012
c	0.09	-	0.20	0.004	-	0.008
D	6.40	6.50	6.60			
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65			.0256		
K	0°	-	8°	0°	-	8°
L	0.50	0.60	0.75	0.019	0.024	0.030

Marking: AYWWIZZ

A: Pb-Free Identifier
Y: Last Digit of Manufacturing Year
WW: Manufacturing Week
I: Plant Identifier
ZZ: Traceability Code

JEDEC Package Outline Standard:
MO – 153

Thermal Resistance $R_{th(j-a)}$:
89 K/W in still air, soldered on PCB.

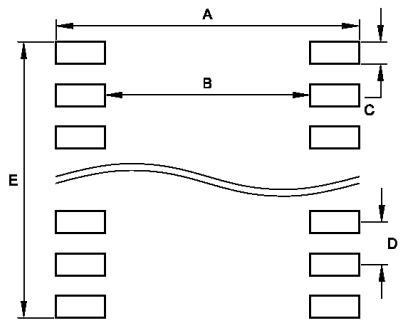
IC's marked with a white dot or the letters "ES" denote Engineering Samples

14 Ordering Information

Delivery: Tape and Reel: 1 reel = 1000 devices
1 reel = 4500 devices
Tubes: 1 box = 100 tubes à 74 devices

Order # AS5311ASSU for delivery in tubes
Order # AS5311ASST for delivery in tape and reel

15 Recommended PCB Footprint



Recommended Footprint Data		
	mm	inch
A	7.00	0.276
B	5.00	0.197
C	0.38	0.015
D	0.65	0.026
E	6.23	0.245

16 Revision History

Revision	Date	Owner	Description
1.01	26-Jun-09	jja, jlu	Recommended footprint data updated
1.02	09-Apr-10	agt	Delivery information updated
1.03	24-Sep-10	agt	Fig.9 updated
1.04	14-March-11	mub	Table 4. Parity bit change 1…17 IC Marking Fig. 17

17 Copyrights

18 Disclaimer

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