

AS3636

Preliminary Datasheet, Confidential

Xenon Driver IC with LED Driver and Life Time Counter

General Description

The AS3636 is a highly integrated photoflash charger including IGBT driver, inductive DCDC boost autofocus/ video LED driver, an indicator LED driver and it includes system level ESD protection and a breakable fuse.

The AS3636 includes flash timeout, over- and undervoltage, overtemperature and LED short circuit protection functions. To reduce production test time a broken transformer or a broken coil is detected.

The AS3636 is controlled by an I²C interface with a dedicated STROBE input. Additionally the TORCH input controls the torch function. An interrupt output is available to signal an error condition to the controller.

The device includes 11 Bytes EEPROM, and an automatic life time counter to count the number of flashes performed.

The AS3636 is available in a space-saving WL-CSP package and operates over the -30°C to +85°C temperature range.

Warning: Lethal voltages are present on applications using AS3636! Do not operate without training to handle high voltages.

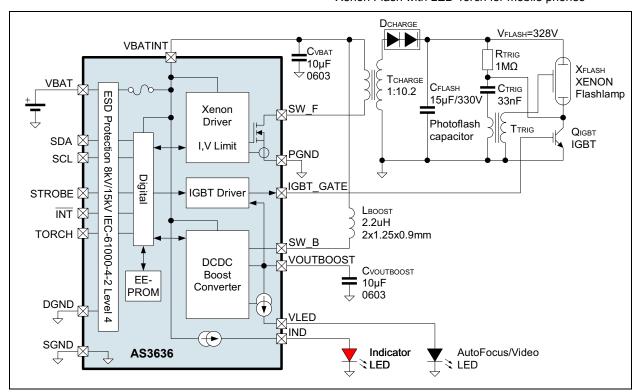
Figure 1. AS3636 Typical Operating Circuit

2 Key Features

- Xenon driver
 - Adjustable recharge timings
 - Adjustable current limits
 - In-production trimmable end of charge voltage
 - Photosensor support
- IGBT Driver
 - Trimmable IGBT voltages
 - Trimmable IGBT driving waveform
 - Internal flash duration timer
 - External STROBE input
- DCDC Boost Converter
 - Autofocus/video LED current source
 - Voltage supply for IGBT
- Integrated one time breakable fuse in supply path
- Integrated system level ESD protection according to IEC-61000-4-2 Level 4 (8kV contact, 15kV air dis-
- Available in tiny WL-CSP Packages 4x4 balls 0.5mm pitch, 2.0 x 2.15 x 0.6 mm

3 Applications

Xenon Flash with LED Torch for mobile phones

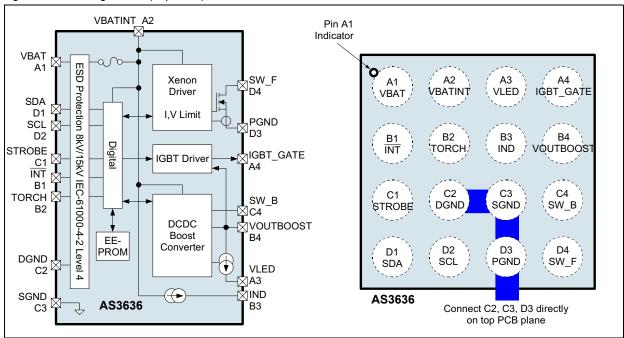




4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View)



Pin Description

Table 1. Pin Description for AS3636

Pin Number	Pin Name	Description
A1	VBAT	Power supply voltage input
A2	VBATINT	Fuse output and internal power supply input - make a short connection to capacitor CVBAT
А3	VLED	Autofocus (AF) / Torch LED output
A4	IGBT_GATE	Drive signal output for IGBT Transistor
B1	ĪNT	Interrupt output, open drain, active low
B2	TORCH	Torch signal input pin; internal pulldown resistor; connect to GND if not used
В3	IND	(Red) Indicator LED output - connect to GND if not used (set ILP=0)
B4	VOUTBOOST	DCDC Boost converter output - make a short connection to CVOUTBOOST
C1	STROBE	Strobe signal input pin to synchronize the flash pulse - usually connected to the camera processor; internal pulldown resistor to GND
C2	DGND	Digital ground supply - connect directly to ground (GND)
C3	SGND	Analog signal ground - connect directly to ground (GND)
C4	SW_B	DCDC Boost converter switching node - connect to coil LBOOST
D1	SDA	serial data input for I ² C interface
D2	SCL	serial clock input for I ² C interface
D3	PGND	Power ground for Xenon and DCDC Boost - connect directly to ground (GND)
D4	SW_F	Xenon DCDC converter switching node - connect to transformer TCHARGE



5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3, "Electrical Characteristics," on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VBAT, VBATINT to GND	-0.3	+7.0	V	
SDA, SCL, STROBE, INT, TORCH, IGBT_GATE, SW_B, VOUTBOOST, VLED, IND to GND	-0.3	VBATIN T + 0.3	٧	max. 7.0V
SW_F to GND	-0.3	+55.0	V	
VOUTBOOST to SW_B	-0.3		V	Note: Diode between VOUTBOOST and SW_B
SGND, DGND, PGND to GND	0.0	0.0	٧	Connect SGND, DGND and PGND to GND directly below the pad (short connection required)
Input Pin Current without causing latchup	-100	+100 +lin	mA	Norm: EIA/JESD78
Continuous Power Dissipation (T _A = +70°C)				
Continuous power dissipation		1	W	Рт ¹
Continuous power dissipation derating factor		14.7	mW/°C	PDERATE ²
Electrostatic Discharge				
		±15000	V	Air Discharge to
ESD pins VBAT, SDA, SCL, STROBE, INT,		110000	v	module; IEC 61000 -4 -2 test bench ³
TORCH		±8000	V	Contact Test to module;
		10000	,	IEC 61000 -4 -2 test bench ³
ESD HBM		±2000	V	Norm: MIL 883 E Method 3015
ESD CDM		±500	V	Norm: JEDEC JESD 22-C101C
ESD MM		±100	V	Norm: JEDEC JESD 22-A115-A level A
Temperature Ranges and Storage Condition	S			
Junction Temperature		+150	°C	Internally limited (overtemperature protection)
Storage Temperature Range	-55	+125	ô	
Humidity	5	85	%	Non condensing
Body Temperature during Soldering		+260	°C	according to IPC/JEDEC J-STD-020C
Fuse				
Fuse Melting time - IFUSE_LIMIT		1000	ms	at 1.5A
1 doc Welling lifte if ool_Liwif	typ.	100	ms	at 2A
Fuse operating current - IFUSE		650	mA	

Depending on actual PCB layout and PCB used; for peak power dissipation during flashing see document 'AS3636 Thermal Measurements'

^{2.} PDERATE derating factor changes the total continuous power dissipation (PT) if the ambient temperature is not 70°C. Therefore for e.g. TAMB=85°C calculate PT at 85°C = PT - PDERATE * (85°C - 70°C)

^{3.} Assembled on PCB board (requires capacitor CVBAT); system test for completed module (fully capsuled), no permanent interruption of operation; proper layout required



6 Electrical Characteristics

VBAT = +2.7V to +5.5V, TAMB = -30°C to +85°C, unless otherwise specified. Typical values are at VBAT = +3.7V, TAMB = +25°C, unless otherwise specified.

Table 3. Electrical Characteristics

VBAT VBATFUNCT IONAL ISHUTDOWN ² ISTANBY ¹	Supply Voltage Supply Voltage Shutdown Current Standby Current Current when AS3636	AS3636 functionally working, but not all parameters fulfilled Shutdown or standby mode, VBAT<3.7V	2.7	3.7	4.4	V
VBATFUNCT IONAL ISHUTDOWN ² ISTANBY ¹ ISTROBEWAI T	Supply Voltage Shutdown Current Standby Current	parameters fulfilled Shutdown or standby mode, VBAT<3.7V		3.7		V
IONAL ISHUTDOWN ² ISTANBY ¹ ISTROBEWAI T	Shutdown Current Standby Current	parameters fulfilled Shutdown or standby mode, VBAT<3.7V	2.3			
ISTANBY ¹ ISTROBEWAI	Standby Current	Shutdown or standby mode, VBAT<3.7V			5.5 ¹	V
ISTROBEWAI T	-			0.5	1.0	
T	Current when A C2626	0°C < TAMB < 50°C		0.5	TBD	μA
TAMB	is waiting for strobe	DCDC operating, IGBT driver enabled		5		mA
TAIVID	Operating Temperature		-30	25	85	°C
		Falling V∨ın	2.1	2.2	2.3	V
Vuvlo	Undervoltage Lockout	Rising V∨ıN	Vuvlo +0.05	Vuvlo +0.1	Vuvlo +0.15	V
Тоутемр	Overtemperature Protection	Junction temperature		144		°C
TOVTEMPHY ST	Overtemperature Hysteresis	Junction temperature		5		°C
Fuse	,		l			
RFUSE	Fuse resistance	Fuse melting times: see Table 2 on page 3			0.2	Ω
EEPROM						
tee_write	EEPROM writing time		10	14.5	24	ms
Xenon Capac	citor Charger					
VTRIPRANGE F	Programming range of VTRIP	6 bit programming measured on pin SW_F Allows in-circuit trimming of the final charged voltage VFLASH on capacitor CFLASH	28.5		34.8	٧
VtripΔ	Comparator trip	VFLASH=328V, TJ=15°C50°C using nominal valued components	-0.5		+0.5	%
VIRIPA	voltage accuracy	VFLASH=328V using nominal valued components	-1.5		+0.5	%
η	Charging Efficiency	System Target only; depends on external components used	60			%
Vsw	Maximum voltage on pin SW				50	V
		Accuracy at typical setting	-10%	750	+10%	mA
Isw	Switching current limit	Adjustable range by register switch_current_selection (see page 29)		750	900	mA
teoc_det		end of charge comparator trigger time - see Figure 4, "AS3636 Internal Circuit," on page 9	128	138	148	ns
DCDC Step U	Jp Converter					
Vvoutboos	DCDC Boost output Voltage (pin	Voltage feedback mode (e.g. if used for IGBT driver)	4.75	5.0	5.25	V
Т	VOUTĔOÖST)	Current feedback mode; max. VVOUTBOOSTMAX	VLED+0.4			V



Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Тур	Max	Unit	
fclk	Operating Frequency	All internal timings are derived from this oscillator	-7.5% -5.0%	2.0	+7.5% +5.0%	MHz	
AF LED Driv	ver		TJ=0°C - 75°C			0.070	
IVLED	VLED current source output	Adjustable by AF_LED limited to Max_LED_	10.0		80.0	mA	
lvled∆	VLED current source accuracy			-7.5		+7.5	%
VVLED	VLED forward voltage			1.7		3.6	V
VVLED_COM P	Current Source Compliance	VOUTBOOST-VLED current compliance	source voltage		200	350	mV
Red privacy	indicator LED (pin INI	D)		•			
lind	IND current source output	adjustable by IND_LE	_	2		16	mA
lindΔ	IND current source accuracy	VBATINT > 2.7V, indicator LEC between 1.3V and 2.4V (e.g	forward voltage . use red LED)	-10		+10	%
IGBT Driver	(pin IGBT_GATE)			i			
RIGBT_GATE	Output driver series resistance	measured at IGBT_fall_spee V(IGBT_GATE)=0	ed2zero=50mA, 0.8V	17	20	23	Ω
	resistance	all current settings and ou	tput voltages	17	20		Ω
IIGBT_RISE	IGBT_GATE rise current	For a IGBT with 10nF gate cap in 0.5V/µs(5mA)8V/µs(80m/ IGBT_rise_and_fall_	10		80	mA	
ligbt_fall	IGBT_GATE fall current	IGBT_fall_speed2zero, IGBT Driving to VVoutBOOST (typ. voltage feedback n	_fall2zero_slow 5.0V, DCDC in	5		80	mA
Protection a	and Fault Detection Fu	nctions		l			
VVOUTBOOS TMAX	DCDC Boost maximum voltage	in current feedback	mode	4.75		5.5	V
	Current Limit for coil		00b		0.25		
ILIMIT	LBOOST (Pin SW_B) measured at 50%	coil_peak_current=	01b	-10%	0.3	+10%	Α
ILIWII I	PWM duty cycle ³		10b	1070	0.35	1070	, ,
	. Trini daty by olo		11b		0.4		
VVLEDSHOR T	AF LED short circuit detection voltage	Voltage measured on լ	oin VLED		1.2	1.65	V
VVLEDOPEN	AF LED open circuit detection voltage	Voltage measured on p	oin VLED		4.0		V
VINDSHORT	Indicator LED short circuit detection voltage	Voltage measured on		0.7	1.2	V	
IIND_OUT OPEN	IND current open detection	Detection threshold for op detection on pin		45		% of IIND_O UT	
Digital Inter	face						
VIH	High Level Input Voltage	Pins SDA, SCL, TO	1.26		VBAT	V	
VIL	Low Level Input Voltage	T IIIS SDA, SOL, TO	0.0		0.54	V	



Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition		Min	Тур	Max	Unit
VIHSTROBE	High Level Input Voltage	Pin STROBE	0.74		VBAT	V	
VILSTROBE	Low Level Input Voltage	FIII 3 TROBE	0.0		0.54	V	
Vol	Low Level Output Voltage	Pins INT and SDA; Ic	oL=3mA			0.2	V
ILEAK	Leakage current	Pins SDA, SCL, I	NT	-10		+10	μΑ
Rpulldown	Pulldown resistor to	Pins TORCH and STROBE	at 1.8V	35	48	65	kΩ
TH OLLBOWN	GND	Tillo TOTOTT and OTTOBE	at 1.2V		37.5		kΩ
tDEBTORCH	TORCH debounce time			6.3	9	11.7	ms
tstrobe_min	STROBE minimum timing				200		ns
I ² C mode tir	nings - see Figure 3 or	n page 7					
ttimeout	SCL timeout	In active mode, if SCL is low f device enters shutdown mode "AS3636 operating mode,"	e - see Figure 5,	35		100	ms
fsclk	SCL Clock Frequency			30		400k	Hz
t _{BUF}	Bus Free Time Between a STOP and START Condition			1.3			μs
t _{HD:STA}	Hold Time (Repeated) START Condition ⁴			0.6			μs
t_{LOW}	LOW Period of SCL Clock			1.3			μs
t _{HIGH}	HIGH Period of SCL Clock			0.6			μs
tsu:sta	Setup Time for a Repeated START Condition			0.6			μs
t _{HD:DAT}	Data Hold Time ⁵			0		0.9	μs
t _{SU:DAT}	Data Setup Time ⁶			100			ns
t_R	Rise Time of Both SDA and SCL Signals			20 + 0.1C _B		300	ns
t _F	Fall Time of Both SDA and SCL Signals			20 + 0.1C _B		300	ns
tsu:sto	Setup Time for STOP Condition			0.6			μs
C _B	Capacitive Load for Each Bus Line	C _B — total capacitance of one	e bus line in pF			400	pF
C _{I/O}	I/O Capacitance (SDA, SCL)					10	pF
	r Parameters - only users on page 37	e transformers approved by a	ustriamicrosyst	ems, se	e Reco	mmend	ed
LPRIMARY	Primary Inductance			6			μH
LLEAK	Primary Leakage Inductance					0.4	μH
				1			



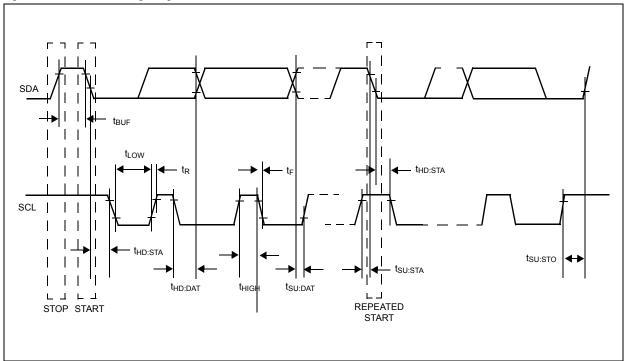
Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Тур	Max	Unit
N	Turns Ratio	for VFLASH=330V (final charged voltage on CFLASH)		10.2		
VISOLATION	Isolation Voltage		500			٧
ISATURATION	Primary Saturation Current		0.84			Α
RPRIMARY	Primary Winding Resistance				0.4	Ω
RSECUNDAR Y	Secondary Winding Resistance				60	Ω

- 1. The overvoltage protection of the DCDC step up converter (pin VOUTBOOST) will trigger above 5.4V thus shutting down the DCDC converter.
- 2. ISHUTDOWN or ISTANBY includes leakage current for SW_B and SW_F.
- 3. Due to slope compensation of the current limit, ILIMIT changes with duty cycle.
- 4. After this period, the first clock pulse is generated.
- 5. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 6. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Timing Diagrams

Figure 3. I²C mode Timing Diagram





7 Typical Operating Characteristics

VBAT = 3.7V, TAMB = +25°C (unless otherwise specified)

Charging Waveform (VFLASH vs. time at 2.7V, 3.7V, 4.2V; IVBAT vs. time)

Charging time (time[s] vs. VVBAT)

VFLASH Output voltage vs. VVBAT (at -30°C, 25°C, 85°C)

VFLASH Output voltage vs. TAMB

Switching waveform details (single cycle: Vsw_F, IVBAT)

IGBT Drive waveforms for short pulses (e.g. 5µs) STROBE, IGBT_GATE vs. time

DCDC Boost Efficiency vs. VVBAT

DCDC Boost Application Efficiency (PLED/PVBAT) vs. VVBAT

IVBAT startup for Torch/AF LED

IVLED output vs. TAMB in Assist mode

Oscillator frequency fclk vs. TAMB

TBD



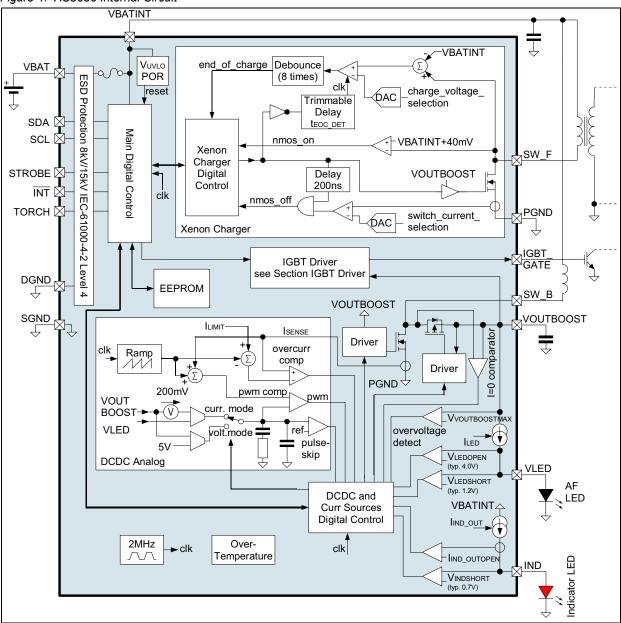
8 Detailed Description

The AS3636 is a highly integrated photoflash charger with build in IGBT driver, inductive DCDC boost autofocus/video LED driver, an indicator LED driver and it includes system level ESD protection and a breakable fuse. The integrated fuse will be blown if there is short circuitry in the module ¹. It is not reversible.

Note: The AS3636 uses a WL-CSP (wafer level chip scale package) to optimize the PCB area required and minimize the module size. Therefore the actual DIE is visible (and it is not molded in plastic as for other packages like QFN or DFN) and the AS3636 is sensitive to external light. It has to be protected from direct light from the Xenon tube.

Internal Circuit

Figure 4. AS3636 Internal Circuit

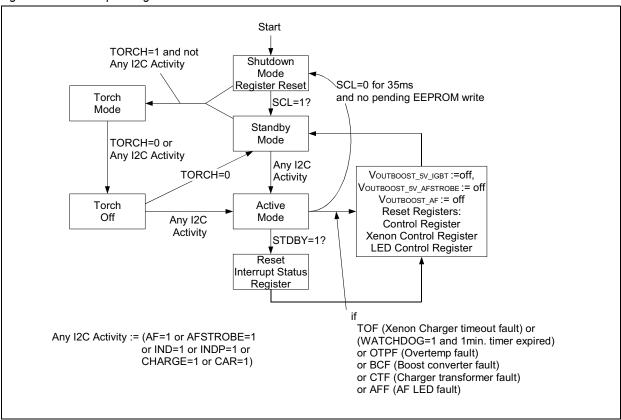


1. The purpose is to fulfill the IEC60065 safety requirements (see section 14.5.4).



Operating modes

Figure 5. AS3636 operating mode

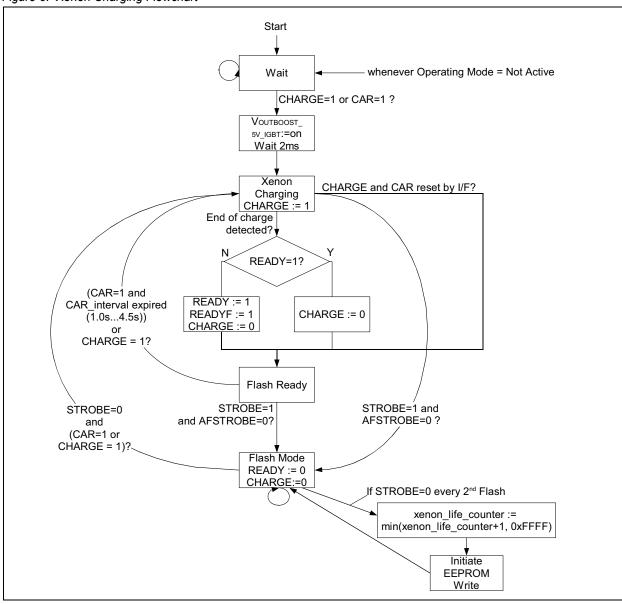


The internal operating modes are chosen according to the flowchart in Figure 5. The xenon charging procedure is described in Figure 6.

The AS3636 wakes up from shutdown mode by sensing its bus. If SCL raises, the AS3636 enters standby modes and the I²C interface is operating. If any activity is sensed (any of the register bits AF, AFSTROBE, IND, INDP, CAR or CHARGE is set), the AS3636 enters active mode.



Figure 6. Xenon Charging Flowchart



Upon setting of CHARGE (see page 26) or CAR, VOUTBOOST is boosted to 5V², the Xenon capacitor charging is started. Once finished, charging is stopped (CHARGE is reset), READY and READYF s set and the interrupt line INT is pulled low (if not disabled by READYFI). Upon STROBE³ a flash is started.

Upon release of STROBE and if the register bit CAR⁴=1 an automatic recharge cycle is started.

Every second flash cycle, the internal life time counter(xenon_life_counter_MSB and xenon_life_counter_LSB) inside the EEPROM (see EEPROM Writing Cycle on page 13) is updated to count the number of flash for the attached Xenon tube.

If no flash is triggered for CAR_interval time (can be set between 1.0s to 4.5s) and CAR = 1, the capacitor is automatically recharged.

^{2.} Using the internal signal Voutboost_5v_IGBT - see DCDC Boost Converter VOUTBOOST on page 12

^{3.} Using the register bit STROBE or the input signal STROBE

^{4.} Capacitor Automatic Recharge



Standby mode is entered upon following conditions and Xenon Control Register, LED Control Register, Control Register and Interrupt Status Register⁵ are reset to their default:

- 1. STDBY is set to 1
- 2. Any fault condition (TOF, CTF, BCF, OTPF, AFF or ILF)
- 3. No flash is triggered within one minute and WATCHDOG=1

By writing '1' into register RESET, all registers can be reset to their default.

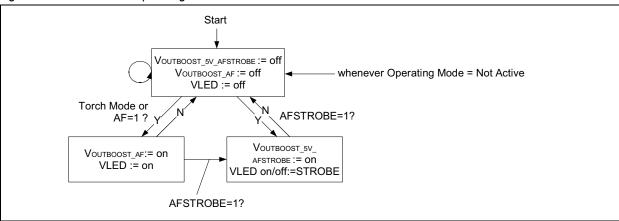
In active mode, if SCL = 0 for 35ms and an EEPROM write is not pending, all registers are reset to their default values and shutdown mode is entered reducing current consumption to a minimum.

Autofocus (AF) LED on pin VLED operating modes

The AF LED can be enabled with the TORCH input or the AF register bit or gated by the STROBE input if AFSTROBE is set. If AFSTROBE is used, the DCDC converter is always run at $5V^6$ to allow for immediate reaction to the STROBE input signal (within μ s). The AFSTROBE register bit has priority over AF signal or TORCH input.

If AF or AFSTROBE is used and WATCHDOG=1, the AF LED and DCDC boost converter is automatically disabled after one minute. Any read or write access to any AS3636 register resets this watchdog timer.

Figure 7. Autofocus LED operating modes

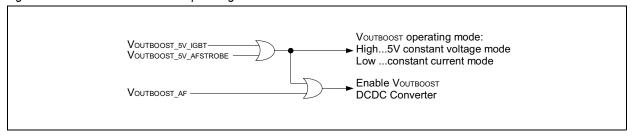


If the AF LED on pin VLED is switched on (as shown in Figure 7, by setting the pin TORCH=H or with the register bit AF and AFSTROBE) the current through the LED is defined by Max_LED_current (for TORCH=H) and AF_LED_current (for AF and AFSTROBE); if PWM=1, then the AF_LED_current current is PWM modulated with a duty cycle defined by AF_LED_PWM.

DCDC Boost Converter VOUTBOOST

VOUTBOOST is used for the IGBT driver and for the autofocus (AF) LED. Therefore it supports 5V constant voltage output and a constant current mode (where the 5V voltage output has priority) as shown in Figure 8:

Figure 8. DCDC Boost converter operating modes



^{5.} Interrupt Status Register is only reset if STDBY is set by the interface

^{6.} Using the internal signal Voutboost_sv_AFSTROBE - see DCDC Boost Converter VOUTBOOST

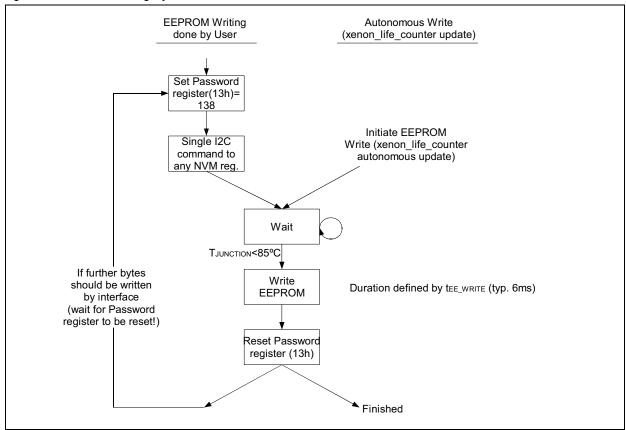


EEPROM Writing Cycle

The internal EEPROM is updated under the following two conditions:

- 1. Life Time Counter: The automatic procedure for update of the internal life time counter is shown in Figure 9; the update of the xenon_life_counter_MSB (see page 28) and xenon_life_counter_LSB is done every 2nd flash cycle (see Figure 5 on page 10) increasing the value by one⁷. The counter does not run over 0xFFFFh.
- 2. NVM Register update: Any update to a NVM register⁸ (See Register Map on page 35) through the interface has to be started by writing 138d to the Password_register. Then the NVM can be written. Do not read or write NVM register during the life time counter is updated. If further bytes should be written, the user shall wait until the Password_register is reset by the AS3636 as shown in Figure 9⁹.

Figure 9. EEPROM Writing Cycle



If the junction temperature exceeds 85° C, the EEPROM writing is postponed until the internal temperature drops (An I^{2} C read to this register will return the old value during this time). Then the writing cycle is automatically executed. See austriamicrosystems application note 'AN3636_In-Production_Trimming_xvx.pdf' for a detailed description of the trimming parameters and procedure.

^{7.} Allow minimum 48ms between updates of the xenon life time counter. Updates happen every 2nd flash pulse.

^{8.} The xenon life time counter (xenon life counter MSB and xenon life counter LSB) cannot be changed.

^{9.} Do not initiate an EEPROM writing cycle during flash as this might collide with the xenon life time counter update.

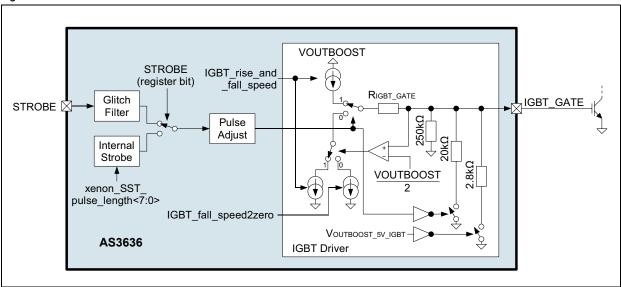


IGBT Driver

The IGBT Driver shown in Figure 10 has an internal glitch filter to filter out short spikes with a length of up to tstrobe_Min. After this filter, the strobe pulse can be adjusted in timing (see IGBT Pulse Timing adjustment on page 14). The actual IGBT driver consists of three current source. One is connected to VOUTBOOST to driver the IGBT_GATE high. The two other current sources drive the IGBT_GATE low, where the falling edge is divided into two sections:

- 1. IGBT rise and fall speed control the edge from VOUTBOOST to VOUTBOOST/2
- 2. IGBT_fall_speed2zero control the remaining part from VOUTBOOST/2 to GND.

Figure 10. IGBT Driver internal circuit



If the STROBE pulse is longer than 2ms, a timeout timer fault is raised and the strobe pulse is stopped - see Xenon charger and strobe timeout fault (TOF) on page 19.

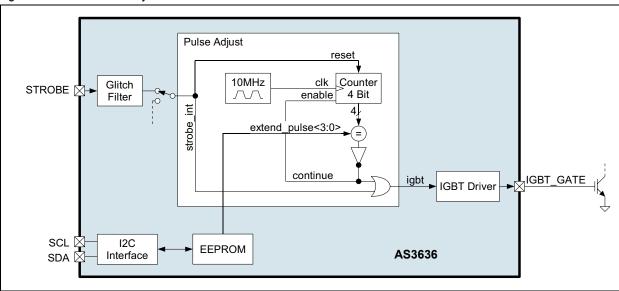
IGBT Pulse Timing adjustment

The IGBT pulse timing can be extended by a programmable duration to allow the fine adjustment of the light output from the Xenon tube during flash especially for light pulses with very short time typically used for pre-flash pulses (typically about 5µs). This adjustment can be performed on a module by module basis thus accurately trimming the light output energy over production for pre-flash pulses.

The internal circuit for this pulse adjustment is shown in Figure 11:

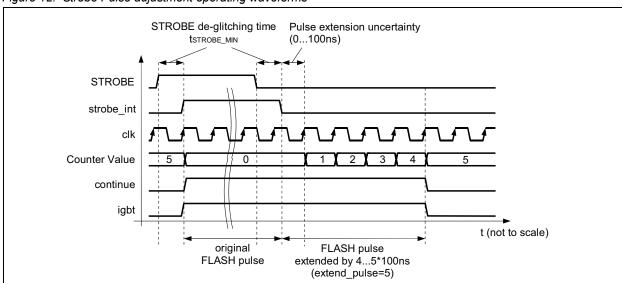


Figure 11. Strobe Pulse adjustment internal circuit



The circuit operates as shown in Figure 12:

Figure 12. Strobe Pulse adjustment operating waveforms



Note: As the internal oscillator is used for pulse adjustment, which is asynchronous to the external signal from STROBE, there is an uncertainty of one clock period in the actual timing extension.

If extend_pulse (see page 29)=0, the pulse adjust circuit is disabled.



Photosensor Detection circuit

The AS3636 supports an external photosensor to detect the reflected light from the Xenon flash. If the reflected light reaches a configurable threshold, the flash pulse is stopped (IGBT_GATE=0). Figure 13 shows the application circuit.

Figure 13. Photosensor detection circuit

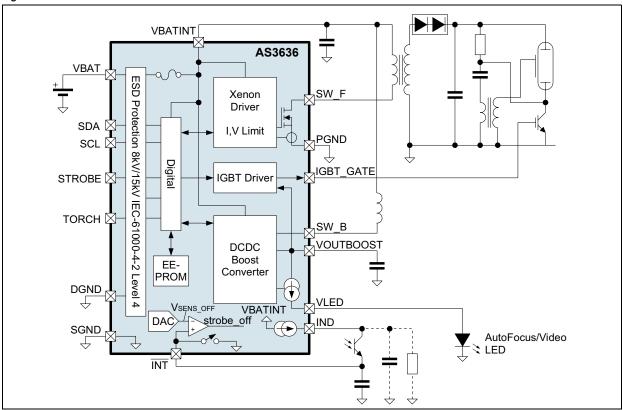
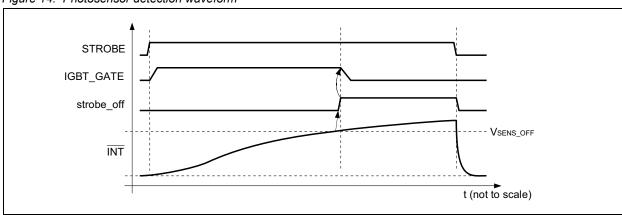


Figure 14 shows a typical waveform:

Figure 14. Photosensor detection waveform



The photosensor detection circuit is enabled by setting phsens_on=1 (this also disables the indicator LED fault detection ILF). Set Interrupt Mask Register=0 to disable the interrupt logic ¹⁰. The indicator LED current source is used to power the photosensor and can be enabled by setting IND=1, ILP=1 and IND_LED_current=11b. The detection threshold Vsens_off is adjustable by register vsens_off_voltage from 1.1V to 1.7V.

^{10.} The pin $\overline{\text{INT}}$ is re-used for the photo-sensor input.



Self Testing

The AS3636 supports internal self testing to allow the verification of the device together with all its external components in a completed system.

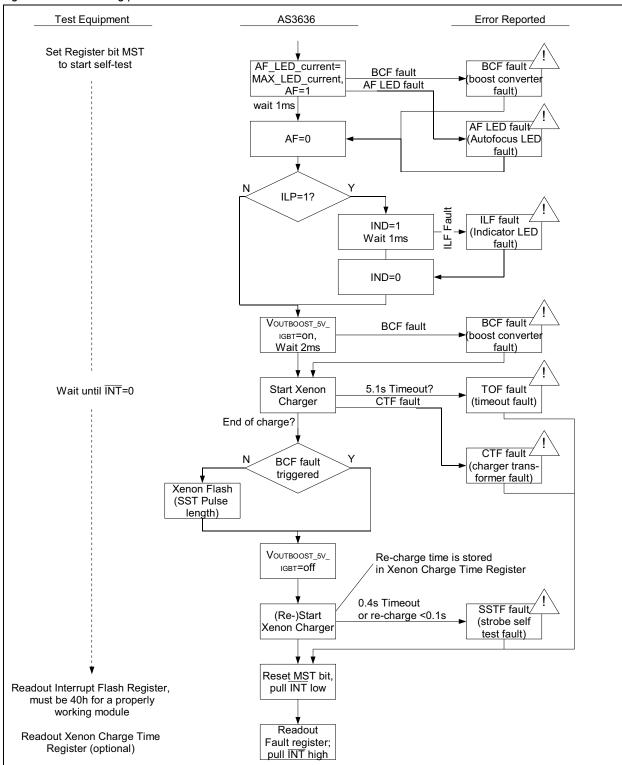
Self testing is initiated in active mode¹¹ by setting the register bit MST (see page 24) and it executes the flow described in Figure 15¹². After the INT signal is low, the test equipment can readout the fault register - for a properly working module, it will read 40h (only register bit READYF set).

^{11.} For entering active mode see Figure 5, "AS3636 operating mode," on page 10 (e.g. after charging)

^{12.}A running self test can only be stopped by writing MST=0 and afterwards STDBY=0; the last step in the procedure is still exectued.



Figure 15. Self Testing procedure





Protection and Fault Detection Functions

The protection functions protect the AS3636 and the external devices against physical damage. In case of a failure a register bit is set. The fault bits are cleared by a readout of the Interrupt Status Register (see page 35). If enabled by the Interrupt Mask Register (see page 35), any fault condition will raise an interrupt by pulling INT low. The interrupt output INT return to open drain, once the fault condition is cleared.

Indicator LED fault (ILF)

If the indicator LED is enabled, an indicator LED fault is triggered under the following conditions:

- 1. In case of no or a broken LED and the current through pin IND is below IND_OUTOPEN.
- 2. If the LED is shorted and the voltage on IND does not reach VINDSHORT.

If one of these conditions is detected the bit ILF is set but the current source is not disabled ¹⁴.

Charge transformer fault (CTF)

If the Xenon charger is started and the AS3636 detects a too low inductance ¹⁵ of the transformer, the Xenon is stopped and the bit CTF is set.

Boost converter fault (BCF)

To limit the maximum current from the battery, the DCDC converter limits its current through the coil to ILIMIT. If within a single cycle ILIMIT is reached and afterwards (still in the same cycle) the current through the coil reaches zero, a shorted coil is assumed. If this condition is detected, the DCDC is stopped, the current source is disabled (if enabled) and the bit BCF is set.

Xenon charger and strobe timeout fault (TOF)

During every charging of the Xenon capacitor, the register charge_time monitor the charge time. If the register reaches FFh, the Xenon charger is stopped and the bit TOF is set.

The register TOF is also set, if the strobe length (from pin STROBE) exceeds 2ms¹⁶. In this case, the IGBT_GATE is switched off automatically.

Overtemperature fault (OTPF)

If the AS3636 junction temperature exceeds TOVTEMP the register bit OTPF is set. The bit OTPF is automatically reset, once the junction temperature drops below TOVTEMP-TOVTEMPHYST.

Autofocus LED fault (AFF)

If the autofocus LED (pin VLED) is enabled, an autofocus LED fault is triggered under the following conditions:

- 1. If the LED is shorted and the voltage on VLED does not reach VVLEDSHORT.
- 2. If the voltage on VLED stays below VVLEDOPEN.

If one of these conditions is detected, the DCDC converter is stopped, the current source is disabled and the bit AFF is set.

Xenon strobe self test fault (SSTF)

The xenon strobe is only used upon self testing - for details see section Self Testing on page 17. The fault bit is set if the re-charge time for the Xenon charger is above 0.4s or below 0.1s.

Supply undervoltage Protection

If the voltage on the pin VBATINT (=battery voltage) is or falls below VuvLo, the AS3636 is kept in shutdown state and all registers are set to their default state.

^{13.}Except overtemperature protection fault OTPF.

^{14.}To avoid erroneously disabling of the indicator current source due to short voltage drops on the supply.

^{15.}An inductance below $0.5\mu H$ will be detected as a fault. Above $3.5\mu H$, a valid transformer is detected.

^{16.} The exact duration can vary between 930 µs to 2.15 ms.



I²C Serial Data Bus

The AS3636 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS3636 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The AS3636 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 16):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

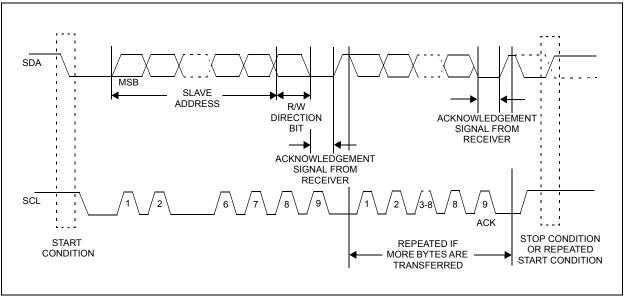
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.



Figure 16. Data Transfer on I²C Serial Bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

- 1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
- 2. Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS3636 can operate in the following two modes:

- 1. Slave Receiver Mode (Write Mode): Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 17). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS3636 address, which is 0101000, followed by the direction bit (R/W), which, for a write, is 0. ¹⁷ After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS3636 acknowledges the slave address + write bit, the master transmits a register address to the AS3636. This sets the register pointer on the AS3636. The master may then transmit zero or more bytes of data, with the AS3636 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
- 2. Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3636 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 18 and Figure 19). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS3636 address, which is 0101000, followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS3636 then begins to transmit data starting with the register address pointed to by the register pointer. If the register

^{17.} The address for writing to the AS3636 is 50h = 01010000b

^{18.} The address for read mode from the AS3636 is 51h = 01010001b



pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS3636 must receive a "not acknowledge" to end a read.

Figure 17. Data Write - Slave Receiver Mode

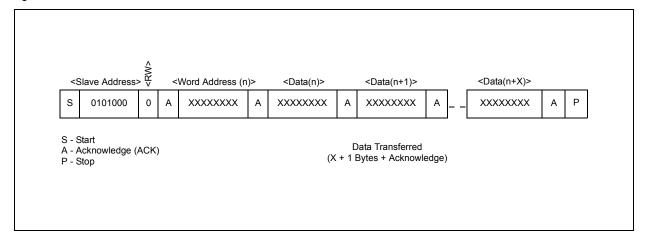


Figure 18. Data Read (from Current Pointer Location) - Slave Transmitter Mode

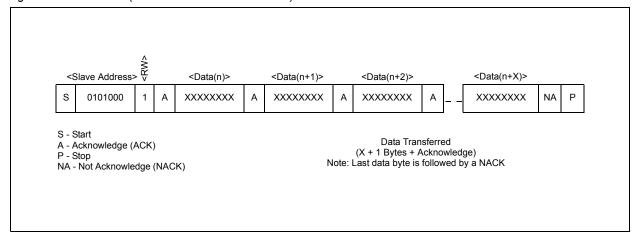
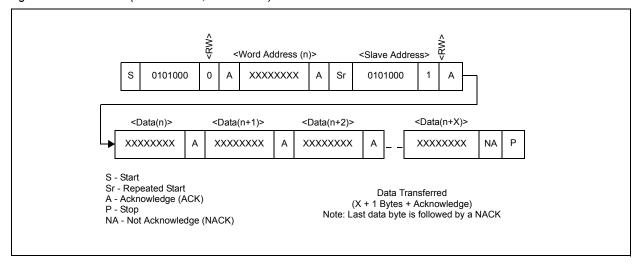


Figure 19. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit





Register Description

Table 4. IC Info Register

Addr: 00h		IC Info Register						
		This register has a fixed content and can be used to verify the l ² C communication						
Bit	Bit Name	Default	efault Access Description					
3:0	IC_model	0010b	R	Fixed ID				
7:4	IC_manufacturer_ID	0001b	R	Fixed Manufacturer ID				

Table 5. IC Version Control Register

	Addr: 01h		IC Version Control Register					
			Design Round Identification					
Bit	Bit Name	Default	Access	Description				
3:0	Design_round	NA	R	Internal number; don't use in software				
7:4		0h	R	always 0, don't use				

Table 6. Module Info Reg.A

	Addr: 02h		Module Info Reg.A					
			Module identification - written by module manufacturer					
Bit	Bit Name	Default	Access	ccess Description				
					Module Sample Type			
			R	00	Technology Sample			
1:0	Module_Type	NVM		R	01	Engineering Sample		
						10	Commercial Sample	
				11	Mass Production			
4:2	Module_Generation	NVM	R	Module Generation				
7:5	Module_Manufacturer_ID	NVM	R		Module Manufacturer			

Table 7. Module Info Register B

	Addr: 03h		Module Info Register B					
Addr. 0311		Module identification - written by module manufacturer						
Bit	Bit Name	Default	Access	Description				
3:0	Module_Major_Version	NVM	R	Module Manufacturer Version				
7:4	Module_Project_Number	NVM	R	Module Manufacturer Project Code				



Table 8. Control Register

	Addm: O4b				Control Register								
	Addr: 04h				Operating mode of AS3636								
Bit	Bit Name	Default	Access		Description								
					Watchdog timer enable								
				0	No watchdog timer								
0	WATCHDOG	HDOG 1	1 R/W	1 R/W	1 R/W	1 R/W	1 R/W	1	After one minute after charging is finished the AS3636 automatically enters standby mode; any read or write access to any AS3636 register resets this one minute watchdog timer				
					Strobe input usage (level sensitive)								
1	AFSTROBE	0	R/W	0	STROBE input is used for Xenon flash								
	•	1000	1	STROBE input is used for AF LED on/off; LED current is defined by LED Current Register with no PWM									
					Module Self Testing								
2	MST 0	0	0 R/W	R/W	0	Read: No module test running Write: Writing '0' stops a running self test							
					1	Writing '1' to this register starts the module self test procedure; when the test is finished MST is automatically cleared - see Self Testing on page 17							
					TORCH pin status (used for module testing)								
3	TORCH_S	0	R	R	R	R	R	R	R	R	R	0	low
				1	high								
5:4		00b	R		always 0, don't use								
					Reset of all registers								
6	RESET	0	R		always reads back '0'								
O	112021		W	0	no action								
			• • • • • • • • • • • • • • • • • • • •	1	all registers are reset to their default								
					Standby mode								
			R/W					0	normal operation (all modes are possible)				
7	STDBY	0		1	Writing '1' writes defaults to Xenon Control Register, LED Control Register and eventually to the Control Register. The AS3636 enters standby mode and clears the bit STDBY								

Table 9. Interrupt Mask Register

	Addr: 05h		Interrupt Mask Register					
Addi. Voli		Mask Interrupts (interrupt output INT, open drain, active low)						
Bit	Bit Name	Default	Access	ess Description				
					Indicator LED fault interrupt			
0	ILFI	1	R/W	1 R/W	R/W	1 R/W	0	Disabled
							1	Enabled
					Xenon Charger Transformer fault interrupt			
1	CTFI	1	R/W	0	Disabled			
					1	Enabled		



Table 9. Interrupt Mask Register (Continued)

	Addr: 05h		Interrupt Mask Register						
			Mask Interrupts (interrupt output INT, open drain, active low)						
Bit	Bit Name	Default	Access		Description				
				DO	CDC Boost converter (VOUTBOOST) fault interrupt				
2	BCFI	1	R/W	0	Disabled				
				1	Enabled				
				•	Xenon Charger Timeout fault interrupt				
3	TOFI	1	R/W	0	Disabled				
				1	Enabled				
	4 OTPFI 1		R/W	•	Over Temperature protection fault interrupt				
4		1		0	Disabled				
				1	Enabled				
					Autofocus LED (VLED) fault interrupt				
5	AFFI	1	R/W	0	Disabled				
				1	Enabled				
					Xenon charger ready interrupt				
6	READYFI	1	R/W	0	Disabled				
				1	Enabled				
					Xenon Strobe Self test fault interrupt				
7	SSTFI	1	R/W	0	Disabled				
				1	Enabled				

Table 10. Interrupt Status Register

				Interrupt Status Register		
Addr: 06h		Interrupts status (interrupt output $\overline{\text{INT}}$, open drain, active low); reading this register automatically clears the interrupt; see Protection and Fault Detection Functions on page 19				
Bit	Bit Name	Default	Access		Description	
					Indicator LED fault interrupt	
0	ILF	0	R/SC ¹	0	no interrupt	
				1	interrupt occurred	
	CTF	0	R/SC ¹		Xenon Charger Transformer fault interrupt	
1				0	no interrupt	
				1	interrupt occurred	
			R/SC ¹	D	CDC Boost converter (VOUTBOOST) fault interrupt	
2	BCF	0		0	no interrupt	
				1	interrupt occurred	
		0			Xenon Charger or Strobe Timeout fault interrupt	
3	TOF		R/SC ¹	0	no interrupt	
				1	interrupt occurred	



Table 10. Interrupt Status Register (Continued)

			Interrupt Status Register					
Addr: 06h		Interrupts status (interrupt output $\overline{\text{INT}}$, open drain, active low); reading this register automatically clears the interrupt; see Protection and Faul Detection Functions on page 19						
Bit	Bit Name	Default	Access	Description				
				Over Temperature protection fault interrupt				
4	OTPF	0	R/SC ¹	0 no interrupt				
				1 interrupt occurred				
			Autofocus LED (VLED) fault interrupt					
5	AFF	0	R/SC ¹	0 no interrupt				
				1 interrupt occurred				
				Xenon charger ready interrupt flag				
6	READYF	0	R/SC ¹	0 no interrupt				
				1 interrupt occurred				
				Xenon Strobe Self test fault interrupt				
7	SSTF	0	R/SC ¹	0 no interrupt				
				1 interrupt occurred				

^{1.} R/SC = Read, self clear: Upon readout, the register bit is automatically cleared.

Table 11. Xenon Control Register

Addr: 07h		Xenon Control Register						
	Addi. 0711		Control Xenon Charger and Re-charging					
Bit	Bit Name	Default	Access		Description			
					Xenon charging			
0	CHARGE	0	R/W	0	Read: no charging; Write: writing '0' to CHARGE stops charging			
				1	Read: Xenon charger running; Write: writing '1' to CHARGE starts charging			
	READY	0	R		Xenon Charger Finished charging			
1				0	not ready for flash			
				1	ready for flash; a flash strobe automatically resets READY			
					Strobe test pulse enable			
			R	0	Input pin STROBE ¹ =0			
2	STROBE	0		1	Input pin STROBE ¹ =1			
				0	IGBT strobe flash is controlled by STROBE pin			
			W	1	A Xenon flash test pulse of length Xenon SST Pulse Length Register is generated			



Table 11. Xenon Control Register (Continued)

	Addr: 07h		Xenon Control Register					
			Control Xenon Charger and Re-charging					
Bit	Bit Name	Default	Access	ess Description				
	CAR	0	R/W		Xenon Charger automatic recharge			
3				0	no automatic recharge			
				1	automatic recharge enabled - see Figure 5 on page 10			
7:4		0000b	R		always 0, don't use			

^{1.} Reading register bit STROBE only returns valid results, if Voutboost_5v_IGBT or Voutboost_5v_AFSTROBE is set. Voutboost_5v_IGBT is set during or after Xenon charging (see Figure 6 on page 11), Voutboost_5v_AFSTROBE is set if AFSTROBE is set (see Figure 7 on page 12).

Table 12. Xenon CAR Interval Register

	Addr: 08h		Xenon CAR Interval Register					
			Xenon automatic Re-charging Timer					
Bit	Bit Name	Default	Access	cess Description				
				Xe	non Re-charging Timer see Figure 5 on page 10			
				000	1.0s			
				001	default 1.5s			
				010	2.0s			
2:0	CAR_interval ¹	001b	R/W	011	2.5s			
				100	3.0s			
				101	3.5s			
				110	4.0s			
				111	4.5s			
7:3		00h	R		always 0, don't use			

^{1.} The first recharge interval can be shorter than selected due to an synchronization to an internal timer. The recharge time is always measured from start of recharge to the next start of recharge.



Table 13. Xenon Charge Time Register

	Addr: 09h		Xenon Charge Time Register					
			Measure last xenon charging time					
Bit	Bit Name	Default	Default Access Description					
			Xen	on charging time; register content is valid if READY=1				
				00h	0-20ms			
				01h	20-40ms			
				02h	40ms-60ms			
7:0	charge_time	00h	R	03h	60ms-80ms			
				FEh	5080-5100ms			
				FFh	>5100ms Xenon charger time out fault was triggered - see TOF			

Table 14. Xenon SST Pulse Length Register

	Addr: 0Ah		Xenon SST Pulse Length Register					
			Xenon strobe test pulse length					
Bit	Bit Name	Default	Access		Description			
		NVM		STF	define Xenon strobe pulse length for register bit ROBE=1 and for Xenon module self testing - see Self Testing on page 17			
	vernen SST nulse lengt			00h	don't use			
7:0	xernon_SST_pulse_lengt h ¹		R	01h	1μs			
				02h	2μs			
				FFh	255µs			

^{1.} The resulting timing can vary by $+1\mu s$ /-0 μ s (excluding the variation of the internal oscillator), therefore use this internal pulse generator only for self testing.

Table 15. Xenon Life Time Register MSB

	Addr: 0Bh		Xenon Life Time Register MSB					
			xenon_life_counter_MSB					
	Bit	Bit Name	Default	Access	Description			
	7:0	xenon_life_counter_MSB	NVM	R	Count the number of flash double-pulses performed and store in NVM - see AS3636 operating mode on page 10 counter stops at FFFFh			

Table 16. Xenon Life Time Register LSB

	Addr: 0Ch		Xenon Life Time Register LSB					
			xenon_life_counter_LSB					
	Bit	Bit Name	Default	Access	Description			
	7:0	xenon_life_counter_LSB	NVM	R	Count the number of flash double-pulses performed and store in NVM - see AS3636 operating mode on page 10 counter stops at FFFFh			



Table 17. Xenon Config Register A

	Addr: 0Dh		Xenon Config Register A					
			Define the end of charge detection voltage					
Bit	Bit Name	Default	Access		Description			
			Define the Xenon end of charge detection voltage (measured on pin SW_F)					
		NVM		00h	28.5V			
5:0	charge_voltage_selection		R	01h	28.6V			
	0 _ 0 _			02h	28.7V			
			3Fh	34.8V				
7:6		00b	R		always 0, don't use			

Table 18. Xenon Config Register B

	Addr: 0Eh		Xenon Config Register B					
			Define the peak current limit for the Xenon charger					
Bit	Bit Name	Default	Access		Description			
					Peak current limit measured on pin SW_F			
				000	375mA			
				001	450mA			
				010	525mA			
2:0	switch_current_selection ¹	NVM	R	011	600mA			
				100	675mA			
				101	750mA			
				110	825mA			
				111	900mA			
				Extend the timing for the IGBT strobe pulse - see IGBT Pulse Timing adjustment				
				0h	no pulse extension			
				1h	100ns			
6:3	extend pulse	NVM	R	2h	200ns			
	_			3h	300ns			
				Eh	1400ns			
				Fh	1500ns			
	IGBT_fall2zero_slow	NVM		Defir	ne together with IGBT_fall_speed2zero IGBT driver fall speed for final switch-off (VOUTBOOST/2 to 0V)			
7			R/W	0	full current - see IGBT_fall_speed2zero			
				1	half current - see IGBT_fall_speed2zero			

^{1.} Take care to set the peak current limit to fit to the Xenon charger transformer used - if the peak current limit is set too low, efficiency will drop and eventually end of charge will not be reached anymore.



Table 19. Xenon Config Register C

	Addr: 0Fh	Xenon Config Register C						
	Addr. UFII	De	fine IGBT	drive	er parameters and SW_B switch current limits			
Bit	Bit Name	Default	Access	Description				
					Define IGBT driver fall speed for final switch-off (VOUTBOOST/2 to 0V)			
					IGBT_fall2zero_slow = 0 1			
				000	1V/μs (10mA) 0.5V/μs (5mA)			
				001	2V/μs (20mA) 1V/μs (10mA)			
2:0	IGBT_fall_speed2zero ¹	NVM	R	010	3V/μs (30mA) 1.5V/μs (15mA)			
				011	4V/μs (40mA) 2V/μs (20mA)			
				100	5V/µs (50mA) 2.5V/µs (25mA)			
				101	6V/µs (60mA) 3V/µs (30mA)			
				110	7V/µs (70mA) 3.5V/µs (35mA)			
				111	8V/μs (80mA) 4V/μs (40mA)			
				Define IGBT switch-on speed and switch-off down to VOUTBOOST/2				
				000	1V/µs (10mA)			
				001	2V/μs (20mA)			
	IGBT_rise_and_fall_spee			010	3V/μs (30mA)			
5:3	d ²	NVM	R	011	4V/µs (40mA)			
				100	5V/μs (50mA)			
				101	6V/μs (60mA)			
				110	7V/µs (70mA)			
				111	8V/µs (80mA)			
				[DCDC Boost Coil Peak current setting (pin SW_B)			
				00	250mA			
7:6	coil_peak_current	NVM	R	01	300mA			
				10	350mA			
				11	400mA			

^{1.} Assuming a 10nF capacitance. The timings scale by the gate capacitance of the IGBT

^{2.} Assuming a 10nF capacitance. The timings scale by the gate capacitance of the IGBT



Table 20. LED Current Register

	A dalas 40b				LED Current Register			
	Addr: 10h		AF LED and indicator LED current and PWM settings					
Bit	Bit Name	Default	Access		Description			
				AF LED Current settings				
				000	10mA			
				001	15mA			
				010	20mA			
2:0	AF_LED_current ¹	000b	R/W	011	28mA			
				100	37mA			
				101	50mA			
				110 65mA				
				111	80mA			
					AF LED PWM setting			
				000	1/32			
				001	2/32			
			R/W	010	3/32			
5:3	AF_LED_PWM ²	000b		011	5/32			
				100	8/32			
				101	12/32			
				110	20/32			
				111	32/32			
					Indicator LED current setting			
				00	2mA			
7:6	IND_LED_current	00b	R/W	01	4mA			
				10	8mA			
				11	16mA			

- 1. AF_LED_current setting is automatically limited to Max_LED_current (see page 32)
- 2. The internal PWM generator output frequency is 31.25kHz (to avoid audible noise)

Table 21. LED Control Register

	Addr: 11h		LED Control Register					
Addi. IIII			Control AF LED and indicator LED operating mode					
Bit	Bit Name	Default	Access	Description				
				Indicator LED on/off				
				0	off			
0	0 IND ¹ 0 F	R/W	1	if ILP=0: use VLED output with AF_LED_current and AF_LED_PWM duty cycle				
				if ILP=1: use IND output with IND_LED_current				



Table 21. LED Control Register (Continued)

	A -1-1 44 b	LED Control Register						
	Addr: 11h		Contr	ol AF	LED and indicator LED operating mode			
Bit	Bit Name	Default	Access		Description			
				100ms Indicator LED pulse				
				0	no pulse			
1	INDP ²	0	R/W	R/W	1	if ILP=0: 100ms pulse on VLED output with AF_LED_current and AF_LED_PWM duty cycle		
				1	if ILP=1: 100ms pulse on IND output with IND_LED_current			
					AF LED PWM enable if AF=1(pin VLED)			
2	PWM	0	R/W	0	no PWM			
				1	AF LED PWM with AF_LED_PWM			
					AF LED on/off (pin VLED)			
3	AF ³	0	R/W	0	off			
	, ,			1	enabled AF LED with AF_LED_current; if PWM=1 use AF_LED_PWM duty cycle			
7:4		0000b	R		always 0, don't use			

- 1. If IND=1 and INDP=1, IND=1 has priority
- 2. After the 100ms pulse, the register INDP is automatically reset
- 3. Do not operate AF=1 and (IND or INDP=1) at the same time

Table 22. LED Configuration Register

	Addr: 12h	LED Configuration Register						
	Addr. 1211		Set max	im AF	LED current and configure indicator type			
Bit	Bit Name	Default	Access		Description			
					AF LED Maximum current limit			
				000	10mA			
			001	15mA				
				010	20mA			
2:0	Max_LED_current	NVM	R	011	28mA			
				100	37mA			
				101	50mA			
			-	110	65mA			
			111	80mA				
6:3		0h	R		always 0, don't use			



Table 22. LED Configuration Register (Continued)

	A .d.d 4.0 ls	LED Configuration Register						
	Addr: 12h		Set max	im AF	LED current and configure indicator type			
Bit	Bit Name	Default	Access	Description				
				Maximum Peak current limit measured on pin SW_F if automatic peak current regulation is performed				
				000	No peak current regulation done - default			
				001	450mA			
	switch_current_selection			010	525mA			
5:3	5:3max	NVM	R	011	600mA			
				100	675mA			
				101	750mA			
				110	825mA			
				111	900mA			
					Double value for switch_current_selection			
6	switch_current_boost	NVM	R	0	I(SW_F) =switch_current_selection			
				1	I(SW_F) = 2 * switch_current_selection			
			R/W		Indicator LED present; applies when indicator is switched on (IND=1)			
7	7 ILP NVM	NVM		0	use VLED output with AF_LED_current and AF_LED_PWM duty cycle			
			1	use IND output with IND_LED_current; ILF (indicator LED fault) detection is enabled				

Table 23. Password Register

	Addr: 13h	Password Register EEDPOM writing password look register						
Bit	Bit Name	Default		EEPROM writing password lock register Description				
			R/W	Un-lock register for EEPROM writing - see EEPROM Writing Cycle on page 13				
7:0	Password_register	00h		138d	Read: EEPROM writing pending Write: Unlock EEPROM writing for next I ² C command			
				0137d, 139d255d	EEPROM writing locked			

Table 24. Photosensor Register

		Photosensor Register						
	Addr: 18h	External Photosensor control - see Photosensor Detection circuit on page 16						
Bit	Bit Name	Default	Default Access Description					
			R/W	Adjust photosensor off - voltage				
6:0	vsens off voltage	00h		0	VSENS_OFF = 1.1V			
0.0	6:0 vseris_oii_voitage	OOH		•••				
				127d	VSENS_OFF = 1.7V			



Table 24. Photosensor Register (Continued)

	Addr: 18h		Photosensor Register External Photosensor control -						
Bit	Bit Name	See Photosensor Detection circuit on page 16 Default Access Description							
				Enable the pho	otosensor detection circuit - see Photosensor Detection circuit on page 16				
7	phsens_on 0	R/W	0	disabled					
				1	photosensor circuit enabled				

Table 25. Xenon Voltage ADC

	Addr: 18h	Xenon Voltage ADC						
	Addr. 1011		Measu	ire last charge	ed voltage of the Xenon charger			
Bit	Bit Name	Default	Default Access Description					
		00h		scaled volta	ured voltage on Xenon charger (represents age on CFLASH) - only valid during charging RGE=1) ¹ or right after end of charge			
6:0	6:0 xenon_charge_voltage 00h	R	0	Vsw_r=lowest reading				
			00h R	•••				
				127d	Vsw_r=highest reading			
				Xenon Cha	arge ADC on - measures voltage on SW_F			
7	xenon adc on	0	R/W	0	disabled			
				1	Internal ADC running if xenon charger running (CHARGE=1)			

^{1.} For reading of xenon_charge_voltage, CHARGE should be set to '0'. If reading of xenon_charge_voltage is required during CHARGE=1, read xenon_charge_voltage twice and compare the results. If both readings show the same result, the value is valid, otherwise re-start the readout.



9 Register Map

Table 26. Register Map

Register Definition	Addr	Default				Cor	ntent				
Name			b7	b6	b5	b4	b3	b2	b1	b0	
IC Info Register	00h	12h	0	0	0	1	0	0	1	0	
IC Version Control Register	01h	0Xh	0 0 0 Design_round								
Module Info Reg.A	02h	NVM	Module	Module_Manufacturer_ID Module_Generation Module_Type							
Module Info Register B	03h	NVM	Мо	odule_Pro	ject_Num	ber	М	odule_Ma	ajor_Versio	on	
Control Register	04h	01h	STDBY	RESET	0	0	TORCH _S	MST	AFSTR OBE	WATCH DOG	
Interrupt Mask Register	05h	FFh	SSTFI	READY FI	AFFI	OTPFI	TOFI	BCFI	CTFI	ILFI	
Interrupt Status Register	06h	00h	SSTF	READY F	AFF	OTPF	TOF	BCF	CTF	ILF	
Xenon Control Register	07h	00h	0	0	0	0	CAR	STROB E	READY	CHARG E	
Xenon CAR Interval Register	08h	01h	0	0 0 0 0 CAR_interval							
Xenon Charge Time Register	09h	00h				charg	e_time				
Xenon SST Pulse Length Register	0Ah	NVM			xer	non_SST_	_pulse_ler	ngth			
Xenon Life Time Register MSB	0Bh	NVM			xe	non_life_d	counter_M	SB			
Xenon Life Time Register LSB	0Ch	NVM			хе	non_life_o	counter_L	SB			
Xenon Config Register A	0Dh	NVM	0	0		cha	arge_volta	ge_select	tion		
Xenon Config Register B	0Eh	NVM	IGBT_fall2 zero_slow		extend	l_pulse		switch_	_current_s	election	
Xenon Config Register C	0Fh	NVM	coil_pea	k_current	IGBT_ris	se_and_fa	all_speed	IGBT_	_fall_spee	d2zero	
LED Current Register	10h	00h	IND_LE	O_current	AF	LED_PW	VM	AF_	_LED_cur	rent	
LED Control Register	11h	00h	0	0	0	0	AF	PWM	INDP	IND	
LED Configuration Register	12h	NVM	ILP switch_current_selection_m ax Max_LED_current						rrent		
Password Register	13h	00h				Passwore	d_register				
General Purpose OTP 1	14h	NVM				User	defined				
General Purpose OTP 2	15h	NVM				User	defined				



Table 26. Register Map (Continued)

Register Definition	Addr	Default	Content								
Name			b7	b7 b6 b5 b4 b3 b2 b1 b0							
Photosensor Register	18h	00h	phsens _on	vsens_off_voltage							
Xenon Voltage ADC	19h	00h	xenon_ adc_on	xenon_charge_voltage							

NVM...Non Volatile Memory using internal EEPROM; for programming see EEPROM Writing Cycle on page 13, don't read or write during life time counter updates

Upon delivery the EEPROM default value are set according to Table 27:

Table 27. EEPROM default settings

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Module Info Reg.A	02h	05h	Module	_Manufac	turer_ID	Modu	ıle_Genei	ation	Module	e_Type
Module Info Register B	03h	00h	Мо	Module_Project_Number				on		
Xenon SST Pulse Length Register	0Ah	08h		xernon_SST_pulse_length						
Xenon Life Time Register MSB	0Bh	00h		xenon_life_counter_MSB						
Xenon Life Time Register LSB	0Ch	00h	xenon_life_counter_LSB							
Xenon Config Register A	0Dh	00h	0 0 charge_voltage_selection							
Xenon Config Register B	0Eh	86h	IGBT_fall2 extend_pulse switch_current				_current_s	election		
Xenon Config Register C	0Fh	80h	coil_peal	k_current	IGBT_ris	se_and_fa	II_speed	IGBT_	_fall_spee	d2zero
LED Configuration Register	12h	07h	ILP switch_current_selection_m			rrent				
General Purpose OTP 1	14h	00h	User defined							
General Purpose OTP 2	15h	00h	User defined							



10 Application Information

External Components

Transformers Tcharge and Ttrig

Following transformers are recommend for the AS3636 (due to the programming features the output voltage VFLASH can be programmed):

Table 28. Recommended Transformers

Component	Part Number	N	L	Size (mm)	Manufacturer	
	TTRN-3825H	10.2	7µH	3.8x3.8x2.5	Tokyo Coil	
	TTRN-3822H	10.2	7µH	3.8x3.8x2.2	www.tokyo-coil.co.jp	
T CHARGE	C3-T2.5R	10.2	7µH	3.4x3.4x2.5	Mitsumi www.mitsumi.co.jp	
	LDT4520T-01	10.2	10µH	4.7x4.5x2.0	TDK www.tdk.com	
T TRIG	BO-02		•	7.3x2.5(3.5)x2.2	Tokyo Coil www.tokyo-coil.co.jp	

Always check if the voltage on the pin SW_F does never exceed the AS3636 maximum Vsw (see Table 3 on page 4) specification during charging.

IGBT

As the AS3636 has an internal DCDC step up included, 2.5V and 4V IGBT can be used without limit on the supply VVBAT. The IGBT is used for two purposes:

- 1. Powering of the Xenon tube and generating together with the oscillation circuit consisting of **T**TRIG, CTRIG, RTRIG a sufficiently high trigger pulse to ignite the Xenon tube (about 3.5kV) this is accomplished by a fast rising edge of the gate of the IGBT
- 2. Switching off the current through the Xenon tube at the end of the flash pulse to accurately control the light emitted by the flash. To protect the IGBT the switching off falling edge voltage should be less than 400V/µs (measured on the emitter of the IGBT)

Both requirements are achieved with the internal driving circuit of the AS3636. Trimming allows to adopt to different trigger coils and IGBTs.

Table 29. Recommended IGBTs

Component	Part Number	min. Drive Voltage	Size	Manufacturer	
	RJP4002ANS	2.5V	VSON-8	_	
	RJP4003ANS	4.0V	3 x 4.8mm	Renesas www.renesas.com	
	RJP4006ANS	2.5V	2.85x2.95mm		
Q IGBT	GT8G133	4.0V	TSSOP-8 3.3 x 6.4mm	Toshiba www.semicon.toshiba.co.jp	
	TIG058E8	4.0V	ECH8 2.8 x 2.9mm	Sanyo www.sanyo.com	

Photoflash Capacitor CFLASH

The photoflash capacitor stores the energy for the flash. Its capacitance define the maximum available energy. Using higher value capacitors as shown in Table 30 is possible, but will increase the charging time.



It is recommended to use low ESR capacitors to avoid loosing power during flash (it is also possible to connect two capacitors in parallel to reduce ESR):

Table 30. Recommended Photoflash Capacitors

Component	Part Number	Capacitor	Voltage size		Manufacturer
CFLASH	330FW13A6.3X20	2x13.5µF ¹	330V	Cylinder 2 x l=24mm, d=7mm	Rubycon www.rubycon.co.jp

Different capacitor values are possible to be used together with the AS3636. Lower capacitor value will reduce charging time, lower ESR capacitor will improve light output energy and reduce losses in the capacitor during the flash pulse.

Photoflash Charger rectification diode DCHARGE

The rectification diode should have very low parasitic capacitance ¹⁹ and has to withstand the operating current and reverse voltages.

Table 31. Recommended Rectification Diodes

Component	Part Number	Parasitic Capacitor	Voltage rating	Size	Manufacturer
	FVO2R80	5pF	800V	1.25x2.5mm	Origin www.origin.co.jp
D CHARGE	GSD2004S	5pF / 2	2x240V	SOT-23 2.4x3.0mm	Vishay www.vishay.com
	BAS21	5pF / 2	2x250V	SC-70 2.0x2.1mm	OnSemi www.onsemi.com

Supply Capacitor CVBAT and DCDC Boost capacitor CVOUTBOOST

Low ESR capacitors should be used to minimize VBAT ripple. Multi-layer ceramic capacitors are recommended since they have extremely low ESR and are available in small footprints. The capacitor should be located as close to the device as possible.

X5R dielectric material is recommended due to their ability to maintain capacitance over wide voltage and temperature range.

Table 32. Recommended CVBAT and CVOUTBOOST Capacitor

Component	Part Number	С	TC Code	Rated Voltage	Size	Manufacturer
C VBAT	GRM188R60J126	10μF >5.5μF @1.8V	X5R	6.3V	0603	Murata www.murata.com
CVOUTBOOST	C1608X5R 0J106M	10µF	X5R	6.3V	0603	TDK www.tdk.com

If a different output capacitor is chosen, ensure low ESR values and voltage ratings.

^{19.}A low parasitic capacitance improves charging efficiency.



Inductor LDCDC

The fast switching frequency (2MHz) of the AS3636 allows for the use of small SMDs for the external inductor. The inductor should have low DC resistance (DCR) to reduce the I²R power losses - high DCR values will reduce efficiency.

Table 33. Recommended Inductor

Part Number	L	DCR	L @ 0.5A Size		Manufacturer
LQM21PN2R2	2.2µH	240mΩ	>1.5µH	2x1.25x0.9mm (0805)	Murata www.murata.com

If a different inductor is chosen, ensure similar DCR values and at least 1.5µH inductance at 0.5A input current.

PCB Layout Guideline

Following layout recommendations apply:

- Keep the path (and area) of GND (SGND directly connected to DGND below the WL-CSP) CVBAT VBATINT

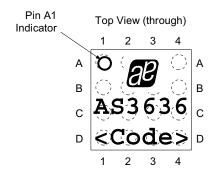
 TCHARGE(primary) SW_F GND as short as possible to minimize the leakage inductance of TCHARGE and ensure a proper supply connection for the AS3636
- 2. Keep the path (and area) of GND CVBAT LBOOST SW_B VOUTBOOST CVOUTBOOST GND as short as possible.
- 3. Place CVBAT as close as possible to the AS3636.
- 4. Ensure wide and short PCB paths for the path GND CFLASH XFLASH QIGBT GND to allow 150A to flow during the flash pulse. Connect this GND only at a single place to the main GND plane.
- 5. The IGBT has two ground connections: One ground for the driving input and one ground for the power path.
- 6. Ensure larger spacings for all high voltage paths; check with the PCB manufacturer to ensure proper minimum spacing for 320V paths and 4kV (Xenon tube trigger pin) paths.
- 7. Minimize the parasitic capacitance of the PCB on the anode of DCHARGE especially to GND and VFLASH
- 8. See austriamicrosystems "WLP-CSP-Handling-Guidelines_1V0.pdf" for proper handling, PCB layout and soldering of the WL-CSP AS3636 device.
- 9. In order to meet system level ESD protection careful routing of the ground lines, supply capacitor CVBAT and supply lines is required.

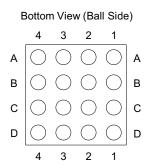
See austriamicrosystems demoboard layout (described in application note 'AN3636').



11 Package Drawings and Markings

Figure 20. 16pin WL-CSP 2x2.15mm Marking





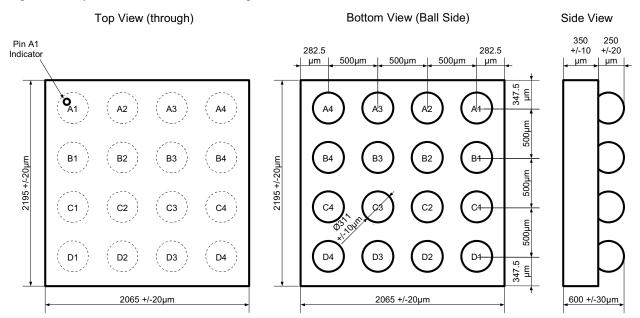
Note:

Line 1: austriamicrosystems logo

Line 2: AS3636 Line 3: <Code>

Encoded Datecode (4 characters)

Figure 21. 16pin WL-CSP 2x2.15mm Package Dimensions



The coplanarity of the balls is $40\mu m$.



12 Ordering Information

The devices are available as the standard products shown in Table 34.

Table 34. Ordering Information

Model	Description	Delivery Form	Package
AS3636-ZWLT	Xenon Driver IC with LED Driver and Life Time Counter	Tape & Reel	16-pin WL-CSP (2mm x 2.15mm) RoHS compliant / Pb-Free

Note: AS3636-ZWLT

AS3636

Z Temperature Range: -30°C - 85°C

WL Package: Wafer Level Chip Scale Package (WL-CSP) 2x2.15mm

T Delivery Form: Tape & Reel



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