AS3542

Data Sheet, Strictly Confidential

Ultra Low Power Stereo Audio Codec with System PMU

1 General Description

The AS3542 is an ultra low power stereo audio codec and is designed for Portable Digital Audio Applications.

It allows CD quality playback with up to 96dBA SNR and recording in FM quality. With one microphone (including pre-amplifier and supply for an electret microphone) and one line input, it allows connecting a variety of audio inputs. The different audio signals can be mixed via a 6-channel mixer and fed to either a headphone output for 16 /32 headsets or a line output. The audio outputs have also an auto fading implemented which performs the fade-in, fade-out as well as the transition between specific volume levels automatically with an selectable timing.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player are supplied by the AS3542. It features 2 DCDC converters for core and memory/periphery supply as well as 4 LDOs. Both DCDC converter feature DVM (dynamic voltage management) with an selectable timing for the voltage stepping. The different regulated supply voltages are programmable via the serial control interface.

The step-up converter for the backlight can operate up to 15V (with an external transistor even higher) in voltage and current control mode. An internal voltage protection is limiting the output voltage in the case of external component failures. An automatic dimming function allows a logarithmic on/off of the backlight with selectable timing.

AS3542 also contains a Li-Ion battery charger with constant current, constant voltage and trickle charging. The maximum charging current is 460mA. An integrated battery switch is separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries.

The AS3542 has an on-chip, phase locked loop (PLL) which generates the needed internal CODEC master clock. I2S Frame and shift-clock have to be applied from the processor for playback and recording.

The single supply voltage may vary from 2.7V to 5.5V.

2 Key Features

Audio

Audio power consumption:

- - 5mW: 95dB DAC to Headphone @ 1.8V, 32Ω

Sigma Delta Converters

- DAC
  - 96dB SNR ('A' weighted) @ 1.8V
- ADC
  - 85dB SNR ('A' weighted) @ 1.8V
- Sampling Frequency
  - DAC: 8-48kHz
  - ADC: 8-24kHz

High Efficiency Headphone Amplifier

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- 2x12mW @16Ω driver capability@ 1.8V supply
- THD -74dB @16Ω; 1.8V
- 2x40mW @16Ω driver capability@ 2.9V supply
- THD -77dB @16Ω; 2.9V
- headphone and over-current detection

Line Output

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- 0.6Vp @10kΩ

Microphone Input

- 3 gain pre-setting (30dB/36dB/42dB) and AGC
- 32 gain steps @1.5dB and MUTE
- supply for electret microphone
- microphone detection
- remote control by switch

Line Input

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- stereo or 2x mono

Audio Mixer

- 6 channel input/output mixer with AGC
- mixes line input and microphone with DAC
- left and right channels independent

Power Management

Voltage Generation

- step down for CPU core (0.61V-3.35V, 250mA)
- step down for peripheral (0.61V-3.35V, 250mA)
- LDO1 for AFE supply (1.7V (1.65-3.2V), 50mA)
- LDO2 for AFE supply (2.7V (2.3-3.5V), 200mA)
- LDO3 for peripherals (1.2V-3.5V, 100mA)
- LDO4 for peripherals (1.2V-3.5V, 100mA)
- separate input for LDO3
- power supply supervision & hibernation modes
- 5sec and 10sec emergency shut-down

Backlight Driver

- step up for backlight (15V)
- current control mode (1.2-36mA)
- voltage control mode
- 1 HV current sink
- automatic dimming
- over-voltage protection

Battery Charger

- automatic trickle charge (55mA)
- prog. constant current charging (55-460mA)
- prog. constant voltage charging (3.9V-4.25V)
- current limitation for USB mode
- integrated battery switch

General

Supervisor

- automatic battery monitoring with interrupt generation and selectable warning level
- automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels

General Purpose ADC

- 10bit resolution
- 19 inputs analog multiplexer

Interfaces

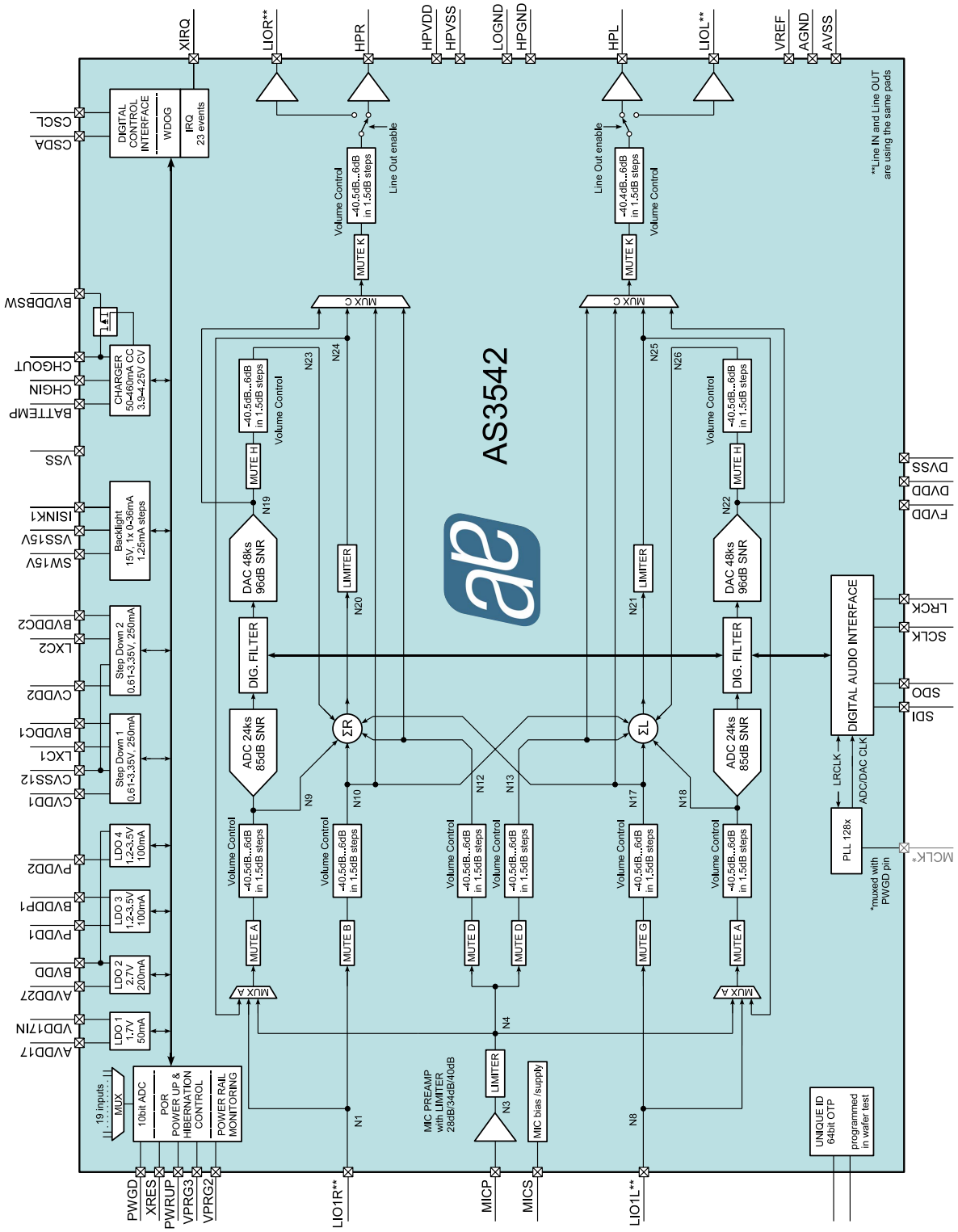
- 2 wire serial control interface
- reset pin with selectable delay, power good pin
- 64bit unique ID (OTP)
- 25 different interrupts
- Package MLF2 56 [7.0x7.0x0.85mm] 0.4mm pitch

3 Applications

Portable Digital Audio/Video Player and Recorder

PDA, Smartphone

Figure 1. Block Diagram



Contents

Revision History

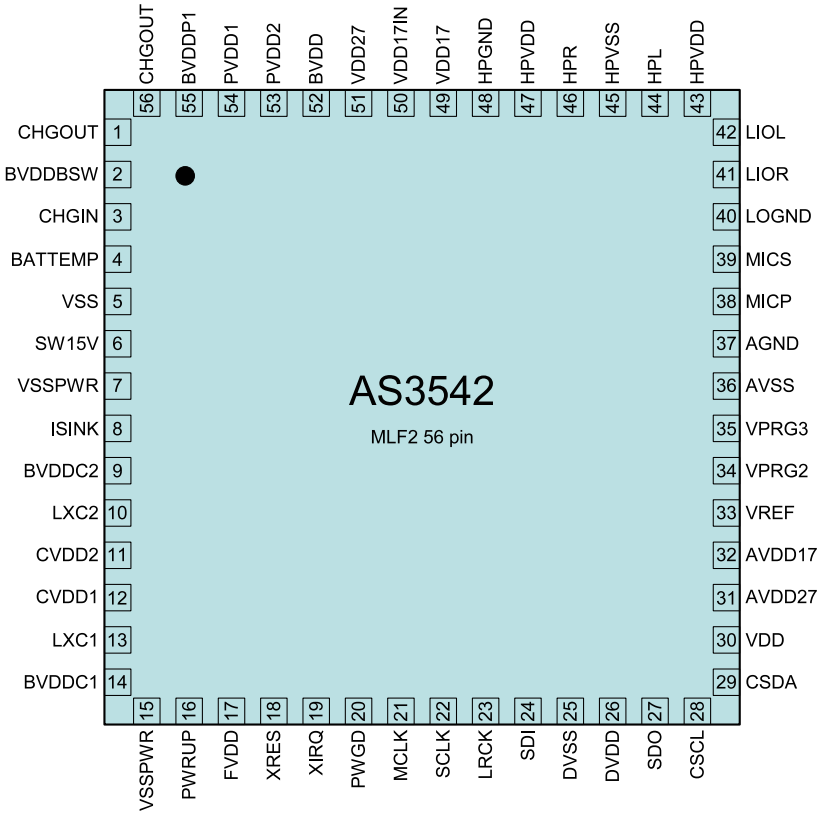
Table 1. Revision History

Revision	Date	Owner	Description
1.00	17.4.2009	pkm	official release
1.10	26.5.2009	pkm	added audio characterisation data

4 Pinout

4.1 Pin Assignment

Figure 2. Pin Assignments (Top View)



4.2 Pin Description

Table 2. Pin Description for AS3542

Pin Number	Pin Name	Type	Description
1	CHGOUT	SUP IO	Li-Ion Charger Output
2	BVDDBSW	SUP IO	Battery Switch output to be connected against BVDD
3	CHGIN	SUP IN	Li-Ion Charger Input
4	BATTEMP	ANA IO	Li-Ion Charger Battery Temp. Sensor Input
5	VSS	GND	Power Management Neg. Reference Supply
6	SW15V	DIG OUT	DCDC15V Switch Output to Coil
7	VSSPWR	GND	Power Management Neg. Supply Terminal
8	ISINK	ANA IO	DCDC15V Load Current Sink Terminal
9	BVDDC2	SUP IN	CVDD2 Step Down Pos. Supply Terminal
10	LXC2	DIG OUT	CVDD2 Step Down Switch Output to Coil
11	CVDD2	ANA IN	CVDD2 and Feedback Pin
12	CVDD1	ANA IN	CVDD1 and Feedback Pin
13	LXC1	DIG OUT	CVDD1 Step Down Switch Output to Coil
14	BVDDC1	SUP IN	CVDD1 Step Down Pos. Supply Terminal

Table 2. Pin Description for AS3542

Pin Number	Pin Name	Type	Description
15	VSSPWR	GND	Power Management Neg. Supply Terminal
16	PWRUP	DIG IN	Power Up Input
17	FVDD	SUP IN	Digital Pos. Supply (e.g. DAC, …)
18	XRES	DIG OUT	Reset Output
19	XIRQ	DIG OUT	Interrupt Request Output
20	PWGD	DIG IO	PowerUp Sequence Complete Output
21	MCLK	DIG IN	MCLK input
22	SCLK	DIG IN	I2S Shift Clock Input
23	LRCK	DIG IN	I2S Frame Clock Input
24	SDI	DIG IN	I2S Data Input to DAC
25	DVSS	GND	Digital Circuit Neg. Supply Terminal
26	DVDD	SUP IN	Digital Periphery Pos. Supply
27	SDO	DIG OUT	I2S Data Output from ADC
28	CSCL	DIG IN	2 wire SERIF Clock Input
29	CSDA	DIG IO	2 wire SERIF Data I/O
30	VDD	ANA IO	LDO output, supply input
31	AVDD27	SUP IN	Analog Pos. Supply
32	AVDD17	SUP IN	Audio Pos. Supply
33	VREF	ANA IO	DAC Reference Pin
34	VPRG2	ANA IN	Memory Supply Voltage Definition Pin
35	VPRG3	ANA IN	PowerUp Sequence Definition Pin
36	AVSS	GND	Ground (analog)
37	AGND	ANA IO	Analog Common Mode Voltage Pin
38	MICP	ANA IN	Microphone Input
39	MICS	ANA IO	Microphone Supply Output / Remote Control input
40	LOGND	ANA IO	Line Output Common Mode Voltage Pin
41	LIOR	ANA IO	Analog Line Input 1 Right Channel
42	LIOL	ANA IO	Analog Line Input 1 Right Channel
43	HPVDD	SUP IN	Headphone Supply default 1.8V (max. 3.6V)
44	HPL	ANA OUT	Headphone Output Left Channel
45	HPVSS	GND	Headphone Ground
46	HPR	ANA OUT	Headphone Output Right Channel
47	HPVDD	SUP IN	Headphone Supply default 1.8V (max. 3.6V)
48	HPGND	ANA IO	Headphone Common Mode Voltage Pin
49	VDD17	SUP IO	LDO1 Output default 1.7V
50	VDD17IN	SUP IN	LDO1 Pos. Supply Terminal
51	VDD27	SUP IO	LDO2 Output default 2.7V
52	BVDD	SUP IN	Main Battery Supply Input (2.7-5.5V)

Table 2. Pin Description for AS3542

Pin Number	Pin Name	Type	Description
53	PVDD2	ANA OUT	LDO4 Output (PVDD2)
54	PVDD1	ANA OUT	LDO3 Output (PVDD1)
55	BVDDP1	SUP IN	LDO3 Pos. Supply Terminal
56	CHGOUT	SUP IO	Li-Ion Charger Output (battery switch input)

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 11 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
5V pins	-0.5	7.0	V	Applicable for pins BVDD, BVDDC1, BVDDC2, BVDDP1, BVDDBSW, CHGIN, CHGOUT, VBUS, CSCL, CSDA, PWRUP
3V pins	-0.5	5.0	V	Applicable for pins DVDD, HPVDD, FVDD, VDD17IN, VDD, VPRG2, VPRG3
15V pins	-0.5	17	V	Applicable for pin SW15V, ISINK
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, VSS15V, CVSS12, HPVSS, AVSS, DVSS
3.3V pins with protection to AVDD27	-0.5	5.0 AVDD27	V	Applicable for pins BATTEMP, HPGND
3.3V pins with protection to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins MCLK, LRCK, SCLK, SDI, SDO, XIRQ, XRES, PWGD
3.3V pins with protection to AVDD17	-0.5	5.0 AVDD17+0.5	V	Applicable for pins LIOL/R, LOGND, VREF, AGND, MICP,MICS
3.3V pins with protection to HPVDD	-0.5	5.0 HPVDD+0.5	V	Applicable for pins HPCM, HPR/L
voltage regulator pins with protection to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD27, PVDD1/2, CVDD1, LXC1, CVDD2, LXC2
voltage regulator pins with protection to AVDD17IN	-0.5	5.0 AVDD17IN +0.5	V	Applicable for pins AVDD17
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
Continuous Power Dissipation (T_A = +70ºC)				
Continuous power dissipation		600	mW	P_T[1] for MLF56 package
Electrostatic Discharge				
Electrostatic Discharge HBM		+/-1	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Operating Temperature Range	-20	+85	ºC	
Junction Temperature		+110	ºC	
Storage Temperature Range	-50	+125	ºC	
Humidity non-condensing	5	85	%	

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Bump Temperature (soldering)				
Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
Moisture Sensitive Level	3		1	Represents a max. floor live time of 168h

1. Depending on actual PCB layout and PCB used

6 Electrical Characteristics

BVDD=+2.7V...+5.5V, T_A =-20ºC...+85ºC. Typical values are at BVDD=+3.6V, T_A=+25ºC, unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltages						
BVDDx	Battery Supply Voltage BVDD, BVDDBSW, BVDDC1, BVDDC2, BVDDP1		2.7	3.6	5.5	V
VBUS	USB VBUS Voltage			5.0	5.5	V
CHGIN	Charger Supply Voltage		4.5		5.5	V
HPVDD	HP Supply Voltage		1.8		3.6	V
DVDD	Digital Periphery Supply Voltage		1.8	2.9	3.6	V
VDD17IN	LDO1 Input Voltage		1.8		3.6	V
FVDD	Digital Supply Voltage		1.75	1.8	2.0	V
AVDD27	Analogue Supply Voltage		2.6	2.7	3.5	V
AVDD17	Analogue Supply Voltage		1.7	1.7	3.5	V
AGND	Analog Ground Voltage	Internally generated		AVDD17 /2		V
V_{DELTA-}	Difference of Negative Supplies CVSS12, VSS15V, HPVSS, AVSS, DVSS, VSS	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1		0.1	V
V_{DELTA+}	Difference of Positive Supplies	RVDD-AVDD27; AVDD17-AVDD27; FVDD-AVDD27			0	V
		HPVDD-AVDD27			0.3	V
		AVDD27-BVDD			0.1	V
POR & Watchdog						
V_{POR_ON}	Power-on Reset Activation Level	Power-on Reset activation level when DVDD decreases		2.15		V
V_{POR_OFF}	Power-on Reset Release Level	Power-on Reset release when DVDD increases		2.0		V
V_{POR_HY}	Power-on Hysteresis			100		mV
f_{LRCLK_WD}	LRCLK Watchdog		2	4.1	8	kHz
PWRUP						
t_{ON_DELAY}	Delay Time of pin PWRUP	Minimum key press time		30		ms
V_{PWRUP_L}	Input Level LOW,	Pin PWRUP, BVDD>3V			0.5	V
V_{PWRUP_H}	Input Level HIGH	Pin PWRUP, BVDD>3V	BVDD/ 3			V
		Pin PWRUP, BVDD<=3V	1			V
I_{PWRUP}	Internal Pull-down Current Source	Pin PWRUP; @2.9V	2.5	7	19	uA

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs/Outputs						
V_{DO_DL}	Digital Output Driver Capability (drive LOW)	Pins XRES, XIRQ, PWGD @ 6mA, push/pull mode only, SDO			10% DVDD	V
V_{DO_DH}	Digital Output Driver Capability (drive HIGH)	Pins XRES, XIRQ PWGD @ 6mA, push/pull mode only, SDO	90% DVDD			V
I_{PU}	Internal Pull-up Current Source	Pins XRES, XIRQ, PWGD; @ 0V		10		µA
V_{DI_L}	Digital Input Level LOW	Pin SDI, SCLK, MCLK, LRCK		30% DVDD		V
V_{DI_H}	Digital Input Level HIGH	Pin SDI, SCLK, MCLK, LRCK		70% DVDD		V
f_{CLK}	Audio Clock Frequency	LRCK according to streamed audio data	8		48	kHz
Power Requirements						
I_{REF}	Reference supply current	all regulators off, only LDO2 on		210		uA
I_{BIAS}	Audio Bias current			32		uA
I_{SUM}	Summing stage current			174		uA
I_{LIN}	Line input stage current	no signal		146		uA
I_{MIC}	Mic input stage current	no signal		643		uA
I_{MICS}	Mic Supply stage current	no load		201		uA
I_{LOUT}	Line output stage current	no load		436		uA
I_{DAC_GS}	DAC gain stage current	no signal		214		uA
I_{ADC_GS}	ADC gain stage current	no signal		1,36		mA
I_{HPH}	Headphone stage current	1.8V, no load		0,95		mA
		1.8V, Bias on, no load		1,21		
		1.8V, CM buffer on, no load		1,37		
		1.8V, Bias on, CM buffer on, no load		1,77		
		1.8V, HQ on		1,24		
I_{DAC}	DAC supply current	LRCK=48kHz		1,48		mA
		LRCK=44.1kHz		1,41		
		LRCK=32kHz		1,19		
		LRCK=16kHz		0,91		
		LRCK=8kHz		0,76		
I_{ADC}	ADC supply current	LRCK=24kHz		1,7		mA
		LRCK=22.05kHz		1,69		
		LRCK=16kHz		1,64		
		LRCK=8kHz		1,58		
		LRCK=4kHz		1,55		
I_{RTC}	RTC supply current			600		nA

6.1 Audio Specification

BVDD=+3.6V, VDD27=+2.7V, HPVDD=FVDD=1.8V, VDD17=+1.7V, f_S=48kHz, T_A=+25ºC, unless otherwise specified.

Table 5. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DAC Input to Line Output						
FS	Full Scale Output	R_L= 10kΩ, f=1kHz, 1V_{RMS} input		0,568		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		96		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, f=1kHz		95		dB
THD	Total Harmonic Distortion	1kHz -1dB FS input, R_L=10kΩ		-90		dB
CS	Channel Separation	R_L=10kΩ		62		dB
Line Input to Line Output						
FS	Full Scale Output	R_L= 10kΩ, f=1kHz, 545mV_{RMS} input		0,545		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
THD	Total Harmonic Distortion	1kHz 1V_{RMS} (-1dB FS) input, R_L=10kΩ		-81		dB
CS	Channel Separation	R_L=10kΩ		100		dB
DAC Input to HP Output						
FS	Full Scale Output	R_L=32Ω		0,560		V_{RMS}
		R_L=16Ω		0,550		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, f=1kHz		94		dB
THD	Total Harmonic Distortion	no load, f=1kHz, FS input		-87		dB
		P_{OUT}=6mW, R_L=32Ω, f=1kHz, -1dB FS		-81		dB
		P_{OUT}=12mW, R_L=16Ω, f=1kHz, -1dB FS		-78	-60	dB
CS	Channel Separation	R_L=32Ω		63		dB
		R_L= 16Ω		60		dB
Line Input to HP Output						
FS	Full Scale Output	R_L= 32Ω, f=1kHz, 545mV_{RMS}(FS) input		0,450		V_{RMS}
		R_L= 16Ω, f=1kHz, 545mV_{RMS}(FS) input		0,447		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
THD	Total Harmonic Distortion	no load, f=1kHz, 545mV_{RMS}		-77		dB
		P_{OUT}=6mW, R_L=32Ω, f=1kHz, 545mV_{RMS}		-75		dB
		P_{OUT}=12mW, R_L=16Ω, f=1kHz, 545mV_{RMS}		-75	-60	dB
CS	Channel Separation	R_L = 32Ω		77		dB
		R_L = 16Ω		66		dB
Mic Input to Line Output						
FS	Full Scale Output	f=1kHz, 27mV_{RMS} FS input		0,512		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		75		dB
THD	Total Harmonic Distortion	1kHz 27mV_{RMS} FS input		77		dB
Mic Input to ADC Output						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		80		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, f=1kHz		77		dB
THD	Total Harmonic Distortion	1kHz 27mVV_{RMS} FS input		-64		dB

7 Typical Operating Characteristics

BVDD = +3.6V, T_A = +25ºC, unless otherwise specified.

8 Detailed Description - Audio Functions

8.1 Audio Line Input

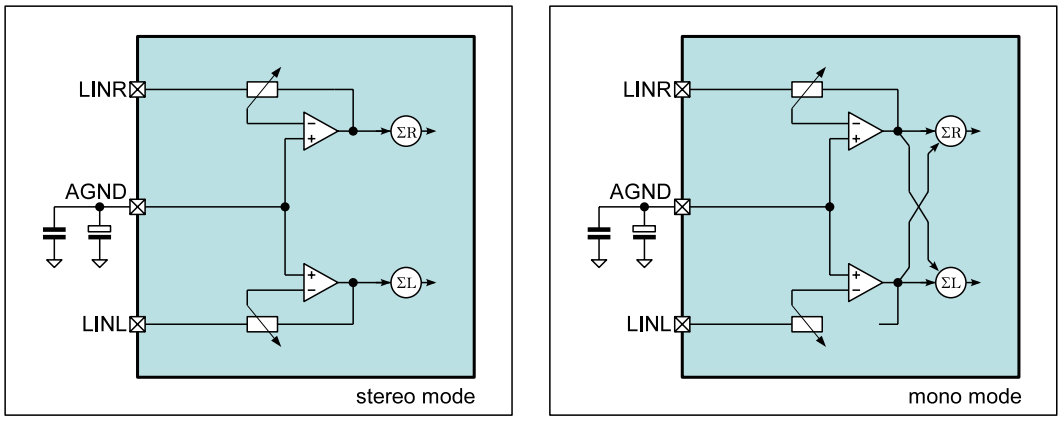
8.1.1 General

The chip features two identical line inputs. The blocks can work in 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each and MUTE. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Line Input and Line Output are sharing the same pins. Please make sure to disable the line out discharge resistors when using line input (LO_DISCHG_OFF in reg. 0Bh).

Figure 3. Line Inputs



8.1.2 Parameter

AVDD17=1.7V, AVDD27=2.7V, T_A= 25°C, unless otherwise mentioned

Table 6. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level	Pls observe gain settings. Max. peak levels at any node within the circuit shall not exceed AVDD		AVDD17 /3	AVDD17 /2	V_{PEAK}
R_{LIN}	Input Impedance	depending on gain setting		8-25		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			5		pF
A_{LIN}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB

8.1.3 Register Description

Table 7. Line Input Related Register

Name	Base	Offset	Description
LINE_IN_R	2-wire serial	0Ah	Right Line Input settings
LINE_IN_L	2-wire serial	0Bh	Left Line Input settings
AudioSet1	2-wire serial	14h	Enable/disable driver stage
AudioSet3	2-wire serial	16h	Enable/disable mixer input

Line input has to be enabled in register 14h first before other settings in register 0Ah and 0Bh can be programmed.

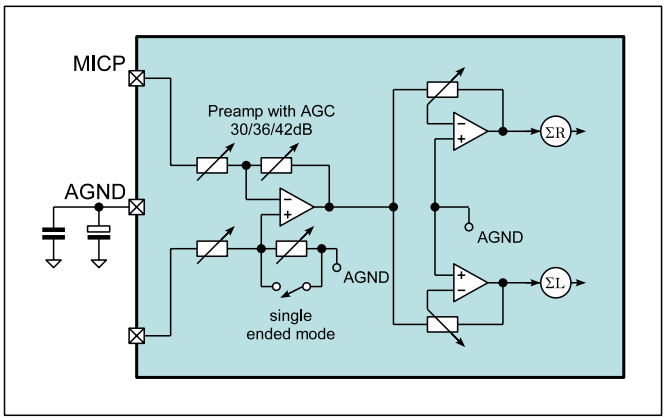
8.2 Microphone Input

8.2.1 General

The AFE offers one microphone input and one low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Please not that only single ended mode is possible for the microphone input, make sure that the MIC_MODE in reg. 06h is set for enalbing the single ended mode.

Figure 4. Microphone Input



8.2.2 Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electret microphones signal to 1Vp. The AGC has 128 steps with 0.375dB with a dynamic range of the full pre-amplifier level. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from –40.5dB to +6dB.

The stage features a soft-start function. Pre-amplifier and gain-stage settings can be set before enabling the microphone stage. After enabling the stage to gain is automatically set to the defined value by using the 128 steps of the AGC.

8.2.3 Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPCM. The supply is designed for ≤2mA and has a 6.5mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 20kOhm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPCM as headset ground the HP–stage gives the interrupt. After enabling the HP-stage through the CPU the microphone detection interrupt will follow.

When using the MICS terminal as ADC-10 input to monitor external voltages the 20kOhm pull-up has to be disabled by disabling the interrupt for microphone detection.

8.2.4 Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this, 1mA as microphone bias is still available.

8.2.5 Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

8.2.6 Parameter

AVDD17=1.7V, AVDD27=2.7V, T_A= 25°C unless otherwise mentioned

Table 8. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MICPRE} = 30dB; AMIC = 0dB		20		mV_P
$V_{MICIN}1$		A_{MICPRE} = 36dB; AMIC = 0dB		10		mV_P
$V_{MICIN}2$		A_{MICPRE} = 42dB; AMIC = 0dB		5		mV_P
R_{MICIN}	Input Impedance	MICP to AGND		7.5		kΩ
Δ_{MICIN}	Input Impedance Tolerance			-7 +33		%
C_{MICIN}	Input Capacitance			5		pF
A_{MICPRE}	Microphone Preamplifier Gain	Preamplifier has 3 selectable (fixed) gain settings		30 36 42		dB
A_{MIC}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Precision			±0.25		dB
V_{ATTACK}	Limiter Activation Level			0.57		V_{PEAK}
V_{DECAY}	Limiter Release Level			0.47		V_{PEAK}
$A_{MICLIMIT}$	Limiter Gain Overdrive	128 @ 0.375dB		30 36 42		dB
t_{ATTACK}	Limiter Attack Time			50		µs/6dB
t_{DECAY}	Limiter Decay Time			120		ms/ 6dB
$A_{MICMUTE}$	Mute Attenuation			100		dB
V_{MICSUP}	Microphone Supply Voltage	depending on V_MICS setting		2 1.55 1.26 1.06		V
I_{MICMAX}	Max. Microphone Supply Current	microphones nominally need a bias current of 0.5mA-1mA		6.5		mA
V_{NOISE}	Microphone Supply Voltage Noise			5		µV
I_{MICDET}	Microphone Detection Current			50		µA
I_{REMDET}	Max. Remote Detection Current			500		µA

8.2.7 Register Description

Table 9. Microphone Input Related Register

Name	Base	Offset	Description
MIC_R	2-wire serial	06h	Right Microphone Input volume settings, AGC control
MIC_L	2-wire serial	07h	Left Microphone Input volume settings, MIC supply control
AudioSet1	2-wire serial	14h	Enable/disable driver stage
AudioSet3	2-wire serial	16h	Enable/disable mixer input
IRQENRD_1	2-wire serial	24h	Interrupt settings for microphone voice activation
IRQENRD_3	2-wire serial	26h	Interrupt settings for microphone detection
IRQENRD_4	2-wire serial	27h	Interrupt settings for remote button press detection

8.3 Line Output

8.3.1 General

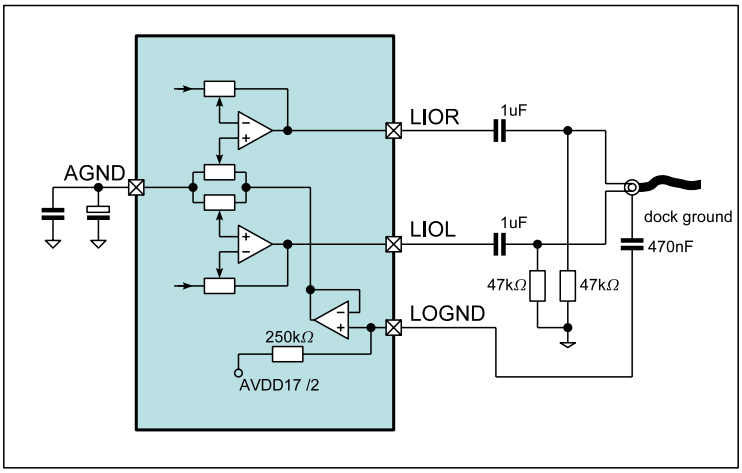
The line output is designed to provide the audio signal with a typical V_{PEAK} level at a load of minimum 10kΩ, which is a minimum value for line inputs. If the limiters (N20/N21) are deactivated the peak output voltage is AVDD17/2 Vp.

This AFE has a combined output stage for headphone and line output with an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB.

If the line output is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the output.

Line Output and Line Input are sharing the same pins.

Figure 5. Line Output



8.3.2 Auto Fading

By setting a new output volume level, the stage does a automatic fading from the current gain setting to the new target. Changing the input multiplexer from one source to another will be done by fadeing out to mute, source changing and fading in of the new source to the target volume. Change from HPH-out to LINE-out is done by fading out of HPH-out to mute and fading in of the LINE-out to the target volume.

The fading speed can be programmed to 3 different speed levels. The immediate response can be selected as 4th state.

8.3.3 Ground Noise Cancelation

A separate ground input allows to connect a ground sense line direct from the dock connector ground or line out jack shield to make the audio output independent from PCB ground noise.

8.3.4 Parameter

AVDD17=1.7, AVDD27=2.7, T_A= 25°C, unless otherwise mentioned

Table 10. Line Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_LO}	Load Impedance (Stereo Mode)	line inputs nominally have 10kΩ	5			kΩ
C_{L_LO}	Load Capacitance (Stereo Mode)				100	pF
A_{LO}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
A_{LOMUTE}	Mute Attenuation			100		dB

8.3.5 Register Description

Table 11. Line Output Related Register

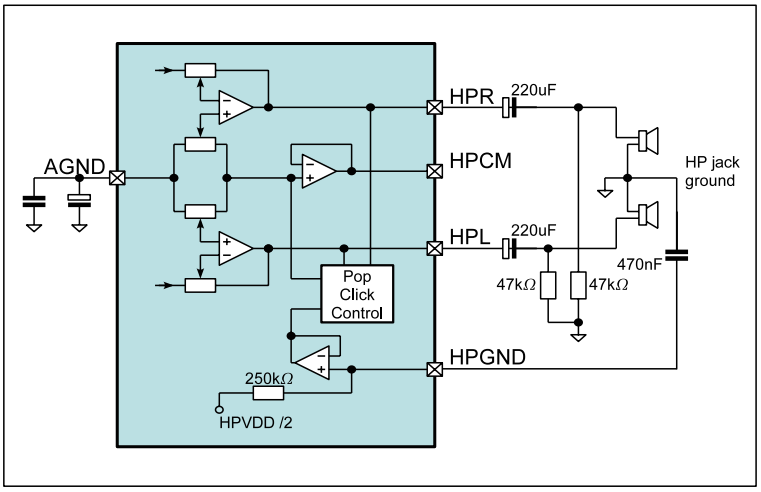
Name	Base	Offset	Description
OUT_R	2-wire serial	00h	Right Line Output volume settings, MUX control
OUT_L	2-wire serial	01h	Left Line Output volume settings
AudioSet2	2-wire serial	15h	Auto fading timing settings
AudioSet3	2-wire serial	16h	Enable/disable mixer input

8.4 Headphone Output

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones.

This AFE has a combined output stage for headphone and line output with an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB.

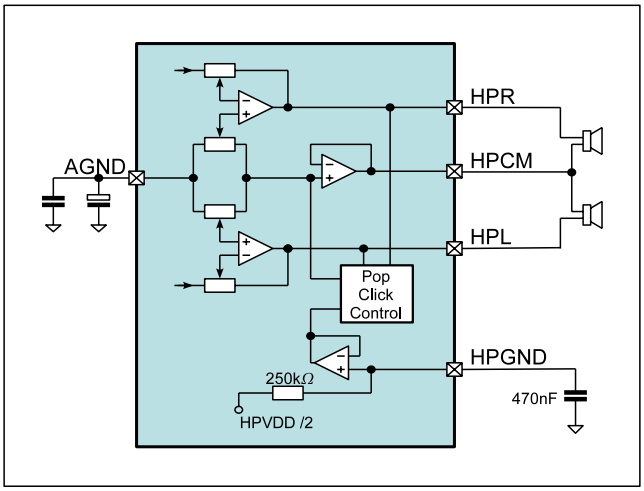
Figure 6. Headphone Output



8.4.1 Phantom Ground

There are 2 ways to connect a headphone to the AFE. In order to spare the bulky ac/dc de-coupling capacitors at pins HPR/HPL a buffered ground (Phantom Ground) is provided. This Common Mode Buffer needs to be switched on if utilized. If form factor considerations are less stringent, the headphones can be conventionally connected via 2x200µF capacitors.

Figure 7. Headphone Output using Common Mode Buffer



8.4.2 No-Pop Function

The output is automatically set to mute when the output stage is disabled.

To avoid Pop-Click noise during power-up and shut-down of the headphone amplifier, a charge/discharge control of HPGND (0V-HPVDD/2-0V) at pins HPR/HPL is incorporated into the AFE. The 470nF capacitor at pin HPGND is used to form the charge/discharge slope. Pls observe that pin HPGND is a high impedance node which must not be connected to any other external device than the 470nF buffer capacitor. To avoid Pop-Click noise one has to wait for 750ms in between a power-down (switch-off) and a power-up (switch-on) of the headphone amplifier.

8.4.3 Auto Fading

By setting a new output volume level, the stage does a automatic fading from the current gain setting to the new target. Changing the input multiplexer from one source to another will be done by fading out to mute, source changing and fading in of the new source to the target volume. Change from HPH-out to LINE-out is done by fading out of HPH-out to mute and fading in of the LINE-out to the target volume.

The fading speed can be programmed to 3 different speed levels. The immediate response can be selected as 4th state.

Figure 8. Headphone Startup with MaxGain Settings

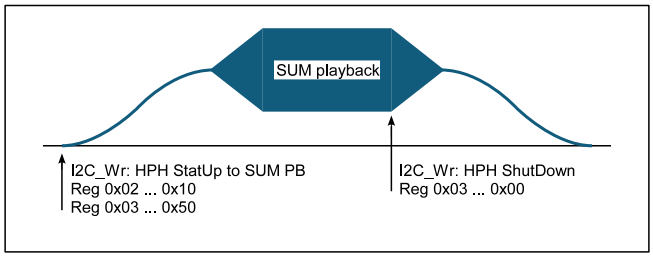
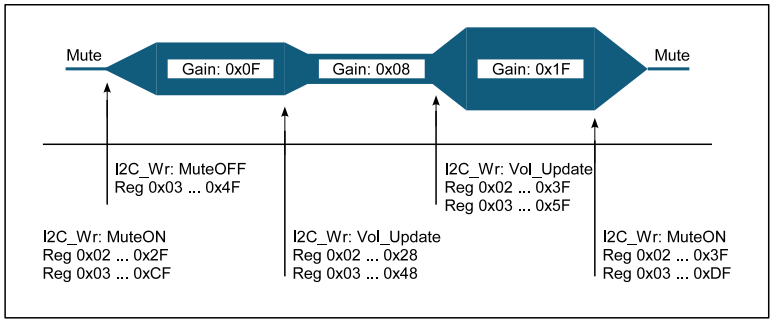


Figure 9. Headphone Change Gain Settings



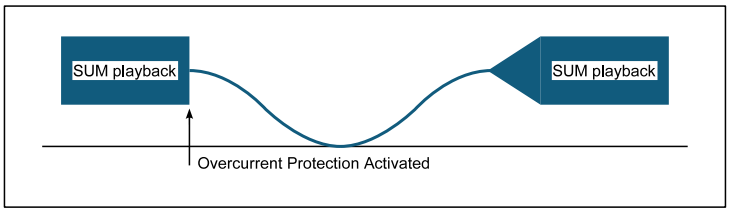
8.4.4 Headphone Detection

When the headphone amplifier is powered down, one can detect the connection of a headset. It only work if the headset is connected between pins HPR/HPL and HPCM. As long as the headphone amplifier is powered down, HPCM is biased to 150mV and acting as the sense pin. There is a corresponding interrupt available to be enabled.

8.4.5 Over-current Protection

The headphone amplifier has an over-current protection (e.g. HPR/HPL is shorted). This over-current protection will power down the headphone amplifier for a programmable time-out period (512ms, 0ms). There is a corresponding interrupt available to be enabled.

Figure 10. Headphone Overcurrent OFF-ON Sequence



8.4.6 Ground Noise Cancelation

As separate ground input allows to connect a ground sense line direct from the dock connector ground or headphone jack shield to make the audio output independent from PCB ground noise.

8.4.7 Power Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current is selected. For 16Ohm loads the bias current can be increased.

8.4.8 Parameter

AVDD17=1.7, AVDD27=2.7, HPVDD = 2.7V, T_A= 25°C, unless otherwise mentioned

Table 12. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	stereo mode	16			Ω
C_{L_HP}	Load Capacitance	stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=16Ω, limiter enabled RL=32Ω, limiter enabled		40 20		mW
A_{HP}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB

Table 12. Headphone Output Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Gain Step Accuracy			±0.25		dB
	Over current limit	HPR/HPL pins HPCM pin, @1.8V		70mA 140mA		mA mA
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB
A_{HPMUTE}	Mute Attenuation			100		dB

8.4.9 Register Description

Table 13. Headphone Related Register

Name	Base	Offset	Description
OUT_R	2-wire serial	02h	Right HP Output volume and over-current settings
OUT_L	2-wire serial	03h	Left HP Output volume settings, enable and detection control
AudioSet2	2-wire serial	15h	Auto fading timing settings
AudioSet3	2-wire serial	16h	Power options, common mode buffer enable
IRQENRD_3	2-wire serial	26h	Interrupt settings for over current and HP detection

8.5 DAC, ADC and I2S Digital Audio Interface

8.5.1 Input

The AFE receives serialized audio data for the DAC via pin SDI. The output of the DAC is fed through a volume control to the mixer stage and to the multiplexers of line output and headphone amplifiers or direct to these output stages.

This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is input to the DAC digital filters. LRCK (Left Right Clock) indicates whether the serial bit-stream received via pin SDI, represents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDI and LRCK are synchronous with SCLK. SDI, LRCK and SCLK are inputs; SDO is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

8.5.2 Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the audio ADC. The digital output is done via an I2S interface.

The AFE sends serialized audio data from the ADC via pin SDO. This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is signalled to the connected devices (e.g. CPU). LRCLK (Left Right Clock) indicates whether the serial bit-stream sent via pin SDI, presents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDO and LRCK are synchronous with SCLK. SDO is an output; LRCK and SCK are inputs; SDI is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate. The exact ratio can be set in register 11h.

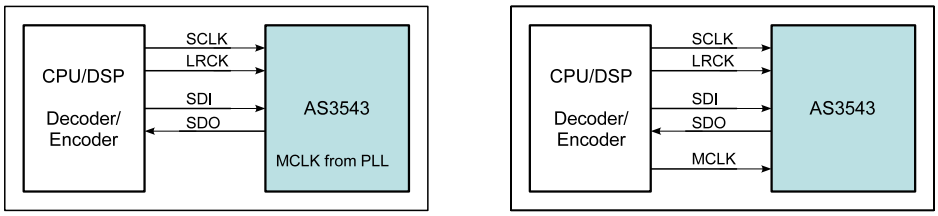
The SDO output can be configured to operate in push/pull (3 different driver strengths) or to be tri-state. For a more detailed description of the GPIO functionality of this pin please refer to chapter GPIO Pins on page 48.

8.5.3 I2S Modes

The AFE can be operated either in Slave Mode or in Slave Mode with the master clock directly signalled via pin MCLK. The master clock (MCLK) is the necessary internal over-sampling clock for the DAC and ADC (e.g. 128*fs, fs=audio sampling frequency)

In Slave Mode the PLL generates the master clock based on LRCK. Thus the PLL needs to be preset to the expected sampling frequency. The ranges are 8kS-23kS (8kHz-23kHz) and 24kS-48kS (24kHz-48kHz). Please refer to register 1A-7h.

Figure 11. I2S Modes



8.5.4 Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

8.5.5 Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

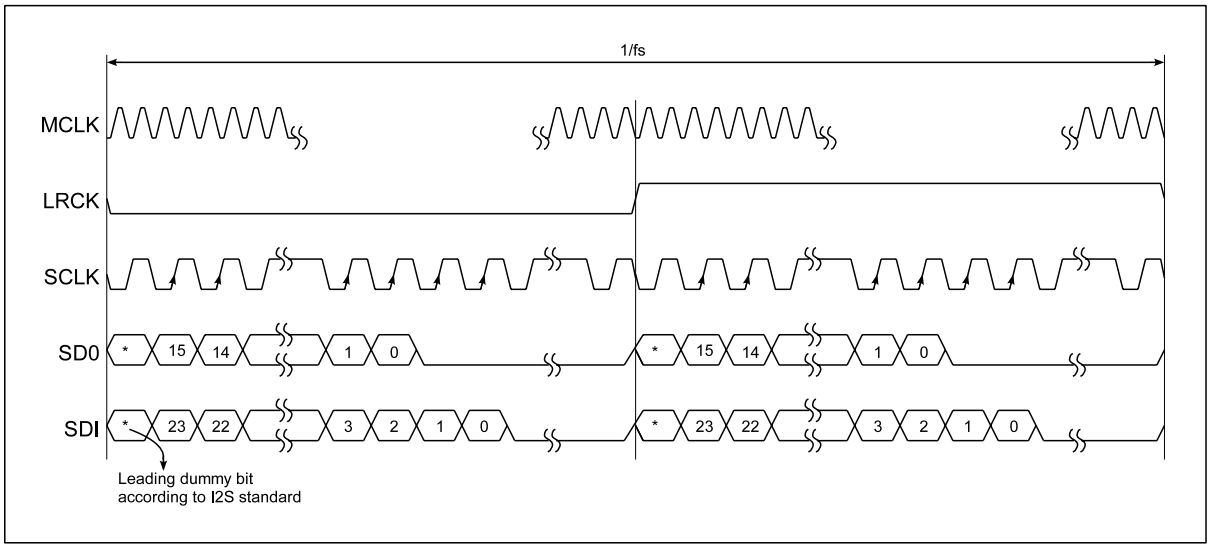
The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with “0”s. In I2S direct mode the data length has to be minimum 18 bits.

The ADC output is always 14 bit. If more SCLK pulses are provided, only the first 14 will be significant.

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

Please observe that LRCK has to be activated before enabling the ADC.

Figure 12. I2S left justified mode



8.5.6 Parameter

DVDD=2.9V, TA=25°C, Slave Mode, fS=48kHz, MCLK = 128*fS, unless otherwise specified

Table 14. I2S Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK}	SCLK Cycle Time		160			ns
t_{SCLKH}	SCLK Pulse Width High		80			ns
t_{SCLKL}	SCLK Pulse Width Low		80			ns
T_{LRSU}	LRCK Setup Time before SCLK rising edge		80			ns
T_{LRHD}	LRCK Hold Time after SCLK rising edge		80			ns
t_{SDSU}	SDI setup time before SCLK rising edge		25			ns
t_{SDHD}	SDI hold time after SCLK rising edge		25			ns
t_{SDOD}	SDO Delay from SCLK falling edge				25	ns
t_{JITTER}	Jitter of LRCK	internal PLL generates MCLK from LRCK	-20		20	ns
I2S direct mode						
T_{SCD}	SCLK delay after MCLK rising edge		0.5		1.5	ns
T_{LRD}	LRLCK delay after SCLK rising edge		0.5		1.5	ns
t_{SDSU}	SDI setup time before SCLK rising edge		5			ns
t_{SDHD}	SDI hold time after SCLK rising edge		5			ns
t_{SDOD}	SDO Delay from SCLK falling edge				15	ns

8.5.7 Register Description

Table 15. Audio Converter Related Register

Name	Base	Offset	Description
DAC_R	2-wire serial	0Eh	DAC input volume settings
DAC_L	2-wire serial	0Fh	DAC input volume settings
ADC_R	2-wire serial	10h	ADC output volume settings, source multiplexer settings
ADC_L	2-wire serial	11h	ADC output volume settings, sampling rate settings
DAC_IF	2-wire serial	11h	DAC input digital volume settings
AudioSet1	2-wire serial	14h	Enable/disable DAC, DAC gain stage & ADC
AudioSet3	2-wire serial	16h	Enable/disable mixer input
Out_Cntr3	2-wire serial	1A-3h	Control of SDO signal and drive
PLL	2-wire serial	1A-7h	PLL sample rate settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 1Ah-3 and 1Ah-7
IRQENRD_1	2-wire serial	25h	Interrupt settings for LRCK changes

DAC and ADC have to be enabled in register 14h first before other settings in register 0Eh to 11h can be programmed.

8.6 Audio Output Mixer

8.6.1 General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1
- Line Input 1/2
- DAC Output
- ADC Input

The mixing ratios have to be set within the volume registers of the corresponding input stages. Please be sure that the peak voltage of input signals for the mixer stage is less than AVDD17/3. If summing up several signals, each individual signal has of course to be accordingly lower. This shall insure that the output signal is also not higher than AVDD17/3 peak to get a proper signal for the output amplifier.

This stage features an automatic gain control (AGC), which automatically avoids clipping.

8.6.2 Register Description

Table 16. Audio Mixer Related Register

Name	Base	Offset	Description
AudioSet2	2-wire serial	15h	Enable/disable mixer stage and AGC
AudioSet3	2-wire serial	16h	Enable/disable DAC, MIC or Line Inputs to mixer stage

8.7 2-Wire-Serial Control Interface

8.7.1 General

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Ch_write
- 8Dh_read

8.7.2 Protocol

Table 17. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1100b (8Ch)
DR	Device address for read	R	1000 1101b 8Dh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
	AS3542 (=slave) receives data		
	AS3542 (=slave) transmits data		

Figure 13. Byte Write

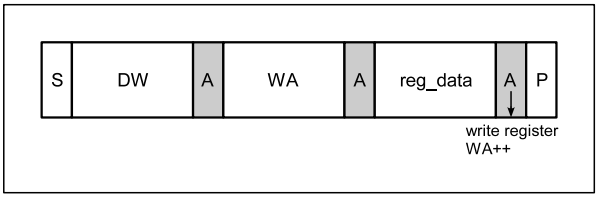
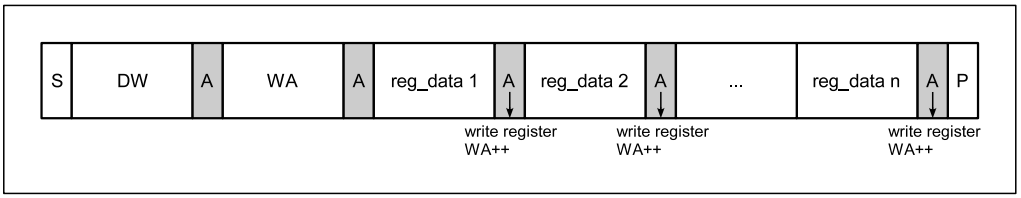


Figure 14. Page Write

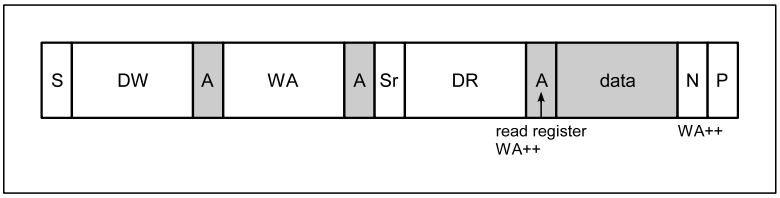


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 15. Random Read

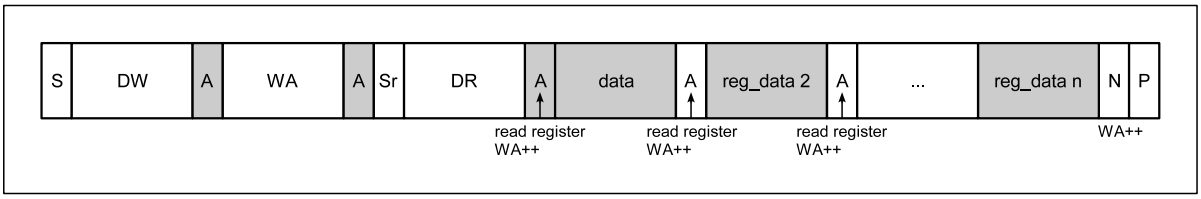


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

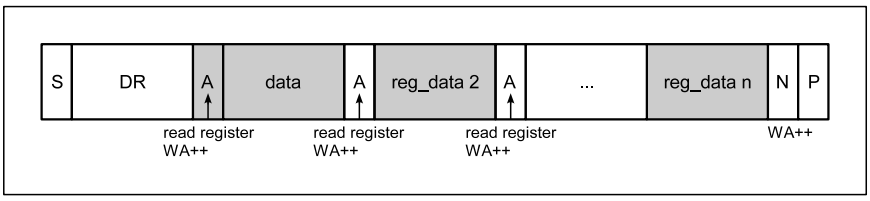
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 16. Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

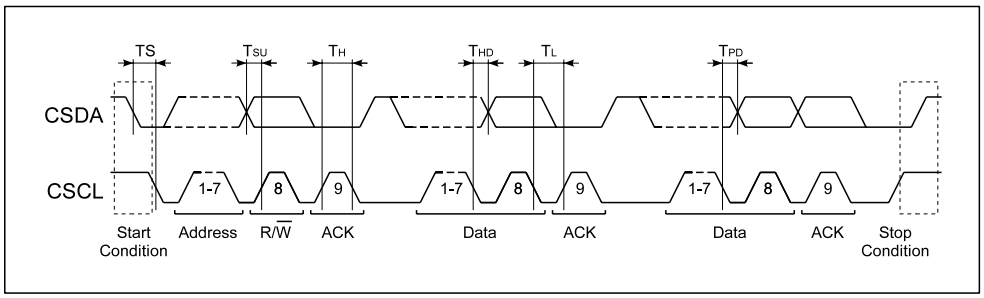
Figure 17. Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

8.7.3 Parameter

Figure 18. 2-Wire Serial Timing



DVDD =2.9V, T_{amb}=25ºC; unless otherwise specified

Table 18. 2-Wire Serial Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30%DVDD)	0	-	0.87	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70%DVDD)	2.03	-	5.5	V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change Tsetup before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_start	200	-	-	ns
T_{PD}		CSDA prop delay relative to lowgoing edge of CSCL		50		ns

9 Detailed Description - Power Management Functions

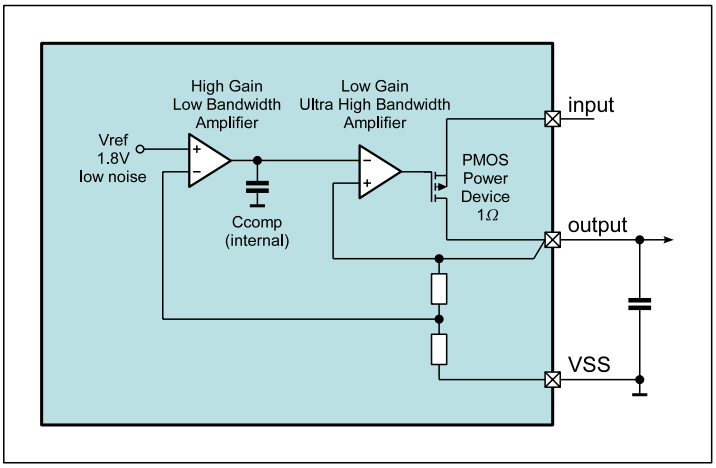
9.1 Low Drop Out Regulators

9.1.1 General

These LDOs are designed to supply sensitive analogue circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF +/-20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 19. LDO Block Diagram



9.1.2 LDO1

This LDO generates the audio supply voltage used for the AFE itself.

- Input voltage is VDD17IN
- Output voltage is VDD17 (typ. 1.7V)
- Driver strength: 50mA

It is set to a default output voltage of 1.7V, $50mA_{max}$. It supplies the analog audio blocks of the AFE. Additional external loads are possible but most not exceed the supply ratings in total together with the operating internal blocks. Further the external load must not induce noise to the sensitive AVDD17 supply pin.

9.1.3 LDO2

This LDO generates the digital and audio supply voltage used for the AFE itself.

- Input Voltage is BVDD
- Output Voltage is VDD27 (typ. 2.7V)
- Driver strength: 100mA

It is set to a default output voltage of 2.7V, $100mA_{max}$. It supplies the digital part of the AFE as well as all audio switches and multiplexers. Additional external loads are possible but most not exceed the supply ratings in total together with the operating internal blocks. Further the external load must not induce noise to the AVDD27 supply pin but is not as critical as AVDD17.

9.1.4 LDO3 & LDO4

These LDOs can used to generate the periphery voltage for the digital processor or other external components (e.g. ext. DAC, USB-PHY, SD-Cards, NAND-Flashes, FM-Tuner …)

LDO3 has a separate input pin (BVDDP1) which can be connected to either the battery or a DCDC converter output.

- Input Voltage BVDDP1 or BVDD
- Output Voltage is PVDD1 & PVDD2 (1.2 to 3.5V)
- Default value at start-up is defined by VPRG2 pin
- Driver strength: 100mA

9.1.5 Parameter

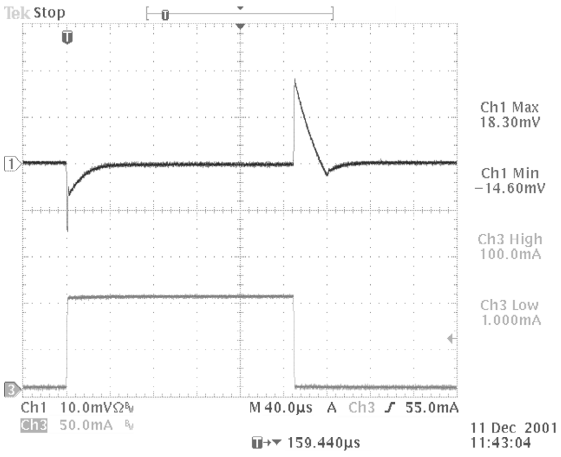
BVDD=3.6V, T_A= 25°C, unless otherwise mentioned

Table 19. LDO Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{ON}	On resistance				1	Ω
PSRR	Power supply rejection ratio	f=1kHz		70		dB
		f=100kHz		40		
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	without load		50		µA
Noise	Output noise	10Hz < f < 100kHz		50		μV_{rms}
t_{start}	Startup time			200		µs
V_{out_tol}	Output voltage tolerance	minimum +/- 50mV	-2.5%		2.5%	mV
$V_{LineReg}$	Line regulation	LDO2, Static		<1		mV
		LDO2, Transient; Slope: t_r=10µs		<10		
$V_{LoadReg}$	Load regulation	LDO2, Static		<1		mV
		LDO2, Transient; Slope: t_r=10µs		<10		
I_{LIMIT}	Current limitation	LDO1		100		mA
		LDO2, LDO3, LDO4		200		

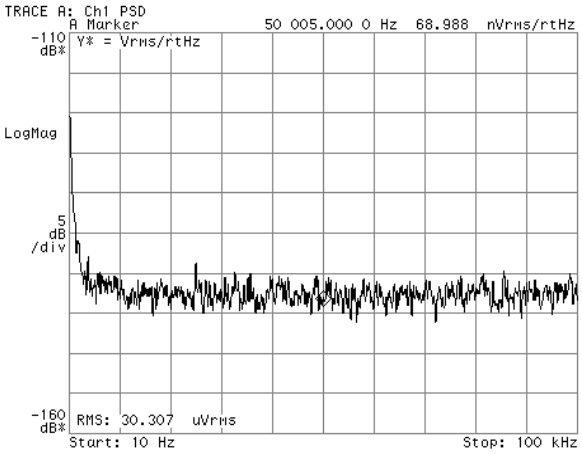
Figure 20. LDO Block Diagram

Load regulation



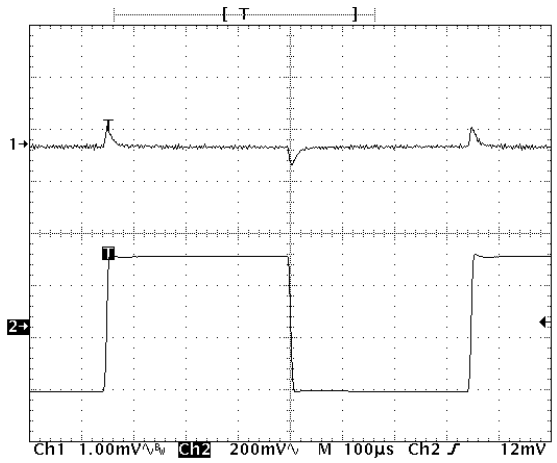
transient load: 1mA – 100mAslope: 1µs

Output noise



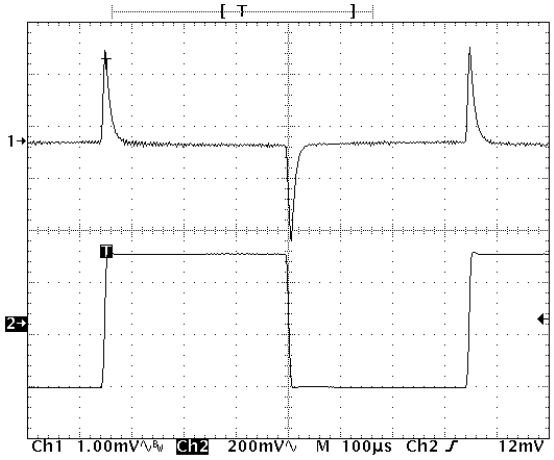
Output load: 150mA

Load Regulation



output load: 10mA
transient input voltage ripple: 500mV

Load Regulation



output load: 150mA
transient input voltage ripple: 500mV

9.1.6 Register Description

Table 20. LDO Related Register

Name	Base	Offset	Description
PVDD1	2-wire serial	18h-1	PVDD1 (LDO3) control and voltage settings
PVDD2	2-wire serial	18h-2	PVDD2 (LDO4) control and voltage settings
AVDD27	2-wire serial	18h-6	AVDD27 (LDO2) control and voltage settings
AVDD17	2-wire serial	18h-7	AVDD17 (LDO1) control and voltage settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 18h-1 to 18h-7

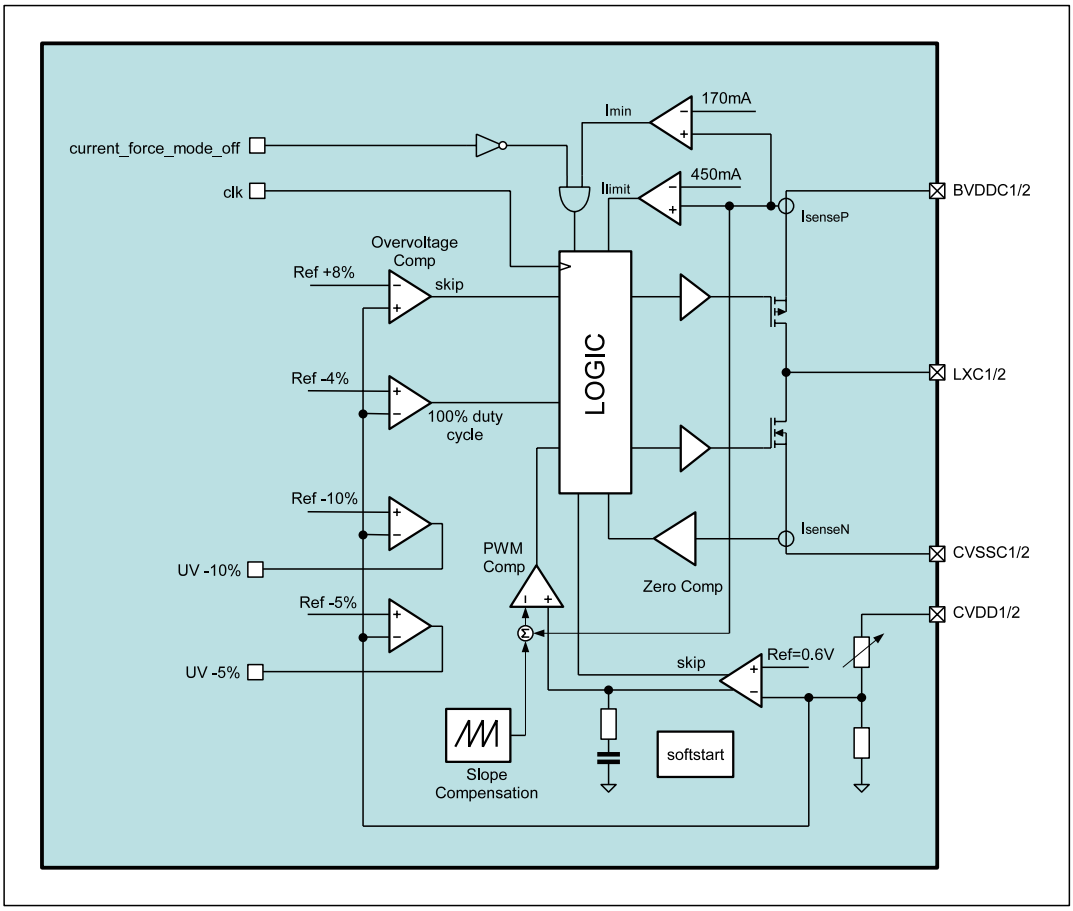
9.2 DCDC Step-Down Converter (2x)

9.2.1 General

These converters are meant to convert the battery voltage down to voltages which fit to the core and peripheral supply voltage requirements for microprocessors.

- input Voltage BVDDC1/2 (usually connected to the battery)
- output Voltage CVDD1 & CVDD2
- output voltage levels can be programmed independently form 0.61V to 3.35V
- the default value at start-up is defined by VPRG1 and VPRG2 pin
- DVM for both outputs with selectable timings
- driver strength 250mA
- under- and over-voltage detection

Figure 21. DCDC Step-Down Block Diagram



9.2.2 Functional Description

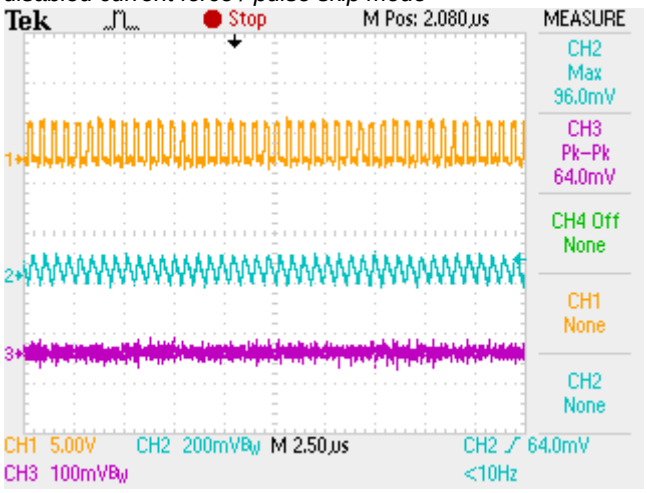
The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 97% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 250mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

To achieve optimized performance in different applications, adjustable settings allow to compromise between high efficiency and low input, output ripple:

Low ripple, low noise operation:

In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. In the case of an inverted coil current the regulator will not operate in pulse skip mode.

Figure 22. DCDC buck with disabled current force / pulse skip mode

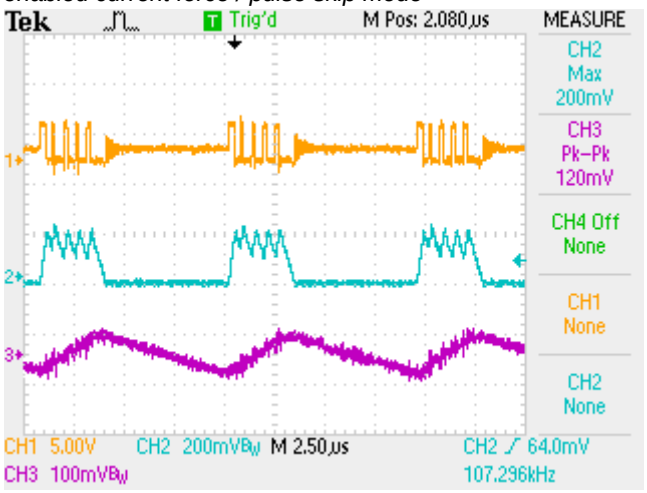


1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

High efficiency operation:

In this mode there is a minimum coil current necessary before switching off the PMOS. As result, fewer pulses at low output loads are necessary, and therefore the efficiency at low output load is increased. On the other hand the output voltage ripple increases, and the noisy pulse skip operation is on up to a higher output current.

Figure 23. DCDC buck with enabled current force / pulse skip mode



1: LXC1 voltage, 2:coil current (1mV=1mA) 3: output voltage

It's also possible to switch between these two modes dynamically during operation:

100% PMOS ON mode for low dropout regulation:

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is than in LDO mode. This feature is enabled if the output voltage drops by more than 4%.

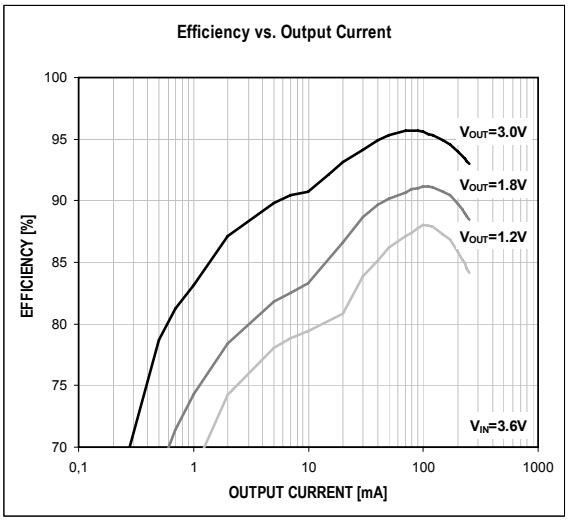
9.2.3 Parameter

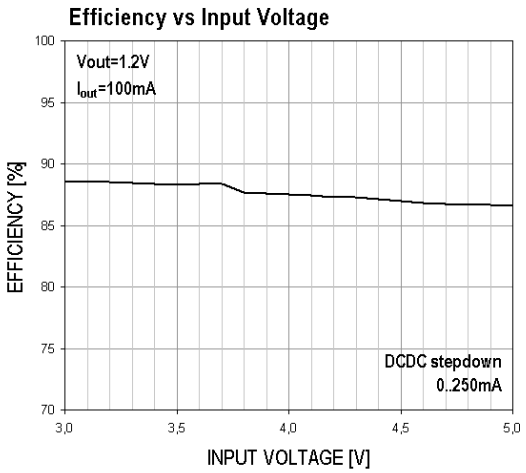
BVDD=3.6, T_A= 25°C, unless otherwise mentioned

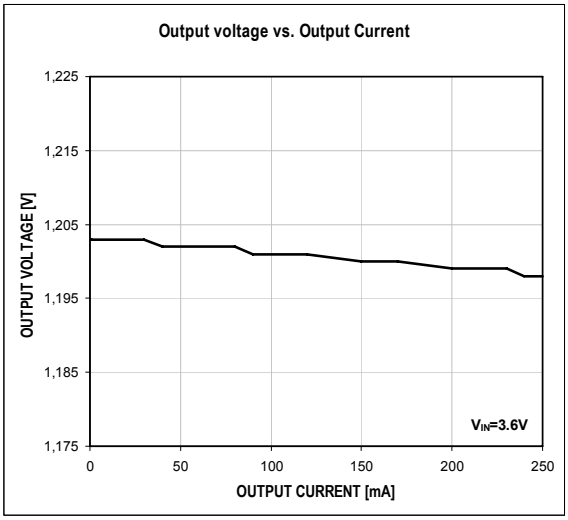
Table 21. DCDC Parameter

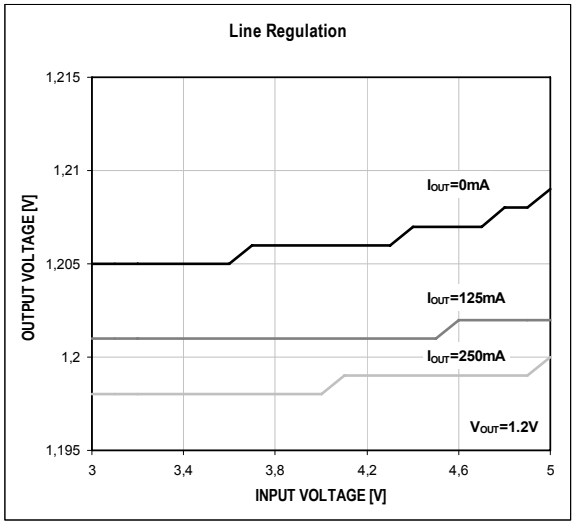
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	BVDD	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.65		3.4	V
V_{OUT_tol}	Output voltage tolerance	minimum +/- 50mV	-3%		3%	mV
I_{load}	Maximum Load current			250		mA
I_{LIMIT}	Current limit			450		mA
R_{PSW}	P-Switch ON resistance	BVDD=3.0V		0.5	0.7	Ω
R_{NSW}	N-Switch ON resistance	BVDD=3.0V		0.5	0.7	Ω
f_{SW}	Switching frequency	depending on DCDC_Cntr settings		1/2		MHz
f_{SWsc}	Switching frequency	in shortcut case		0.6		MHz
C_{out}	Output capacitor	Ceramic, +/- 10% tolerance		10		µF
Lx	Inductor	+/- 10% tolerance	2.2		4.7	µH
η_{eff}	Efficiency	Iout=100mA, Vout=3.0V		97		%
I_{VDD}	Current consumption	Operating current without load Low power mode current Shutdown current		220 100 0.1		µA
t_{MIN_ON}	Minimum on time			80		ns
t_{MIN_OFF}	Minimum off time			40		ns
$V_{LineReg}$	Line regulation	Static		2		mV
		Transient; Slope: t_r=10µs, 100mV step, 200mA load		10		
$V_{LoadReg}$	Load regulation	Static		5		mV
		Transient; Slope: t_r=10µs, 100mA step		50		

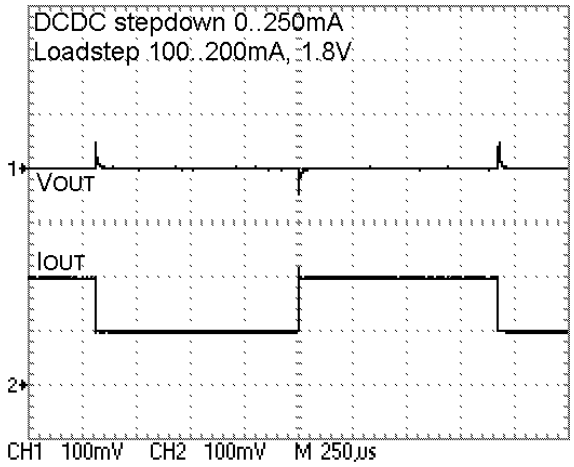
Figure 24. DCDC Step-down Performance Characteristics

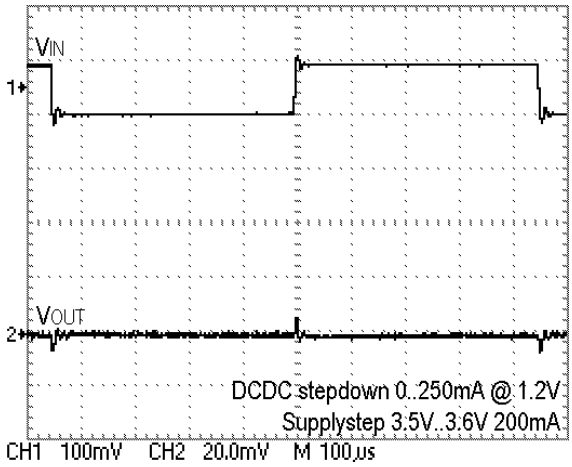












9.2.4 Register Description

Table 22. DCDC Buck Related Register

Name	Base	Offset	Description
CVDD1	2-wire serial	17h-1	CVDD1 (DCDC1) voltage settings
CVDD2	2-wire serial	17h-2	CVDD2 (DCDC2) voltage settings
Hibernation	2-wire serial	17h-6	Hibernation control
DCDC_Cntr	2-wire serial	17h-7	DCDC frequency and DVM settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 17h-1 to 17h-7

9.3 15V Step-Up DCDC Converter

9.3.1 General

The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 15V. A constant switching-frequency results in a low noise on supply and output voltages.

It has a programable high voltage current sinks (1.2 to 37.2mA) for driving e.g. white LEDs as back-light. A voltage feedback mode allows generating constant supply voltages for e.g. OLEDs by using an external Zener diode. To bias the diode ISINK is sinking about 50uA in this voltage feedback mode.

An internal protection circuit will shut down the regulator if the voltage on SW15 exceeds 15V. No more external protection has to be used to avoid an exceeding of the operation conditions in a no load situation.

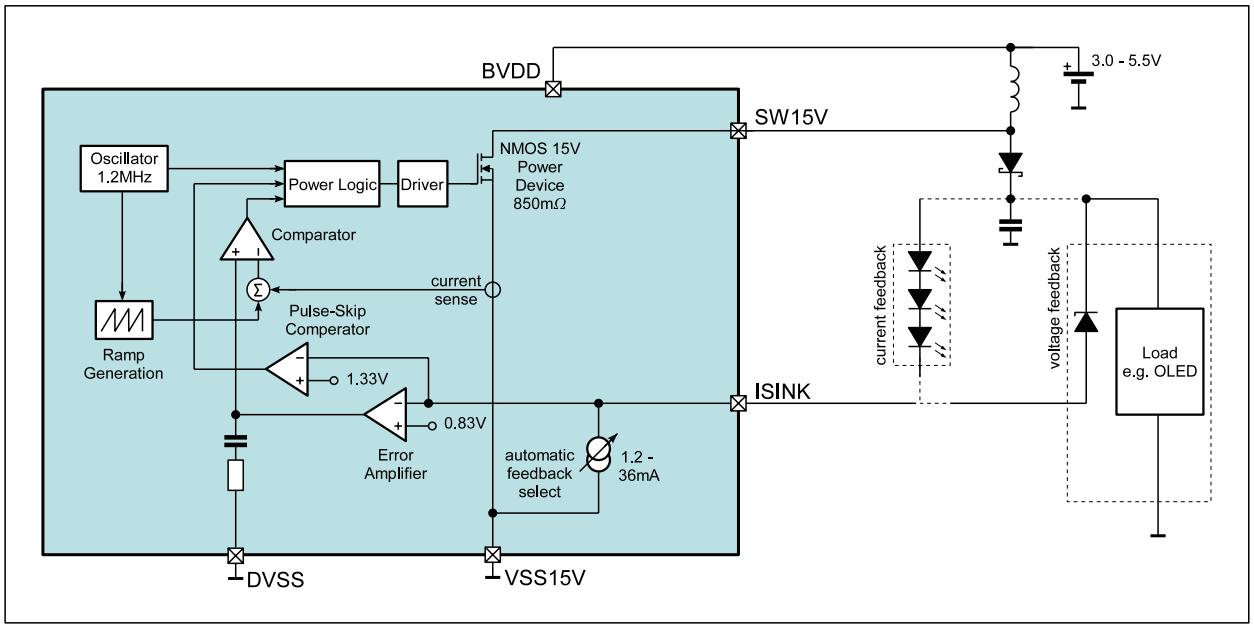
9.3.2 Dimming

The DCDC boster together with the current sinks has an adjustable automatic logarithmic dimming for a smooth ON/OFF transition. It is also possible to control the dimming with an external signal via a GPIO pin. PWGD, Q24M or Q32K pin can be selected as input for the external dimming signal.

9.3.3 Current Sink Only Mode

The current sinks are normally only working when the DCDC booster is swichted on, but can also be activated separtely. To do so reg. 1Bh-1 has to be set to 08h (select external dimming), and reg. 1Ah-4 has to be set to xxxx xx00b (no ext. dimming source selected).

Figure 25. DCDC15 Block Diagram



9.3.4 Parameter

BVDD=3.6V, T_A= 25°C, unless otherwise mentioned

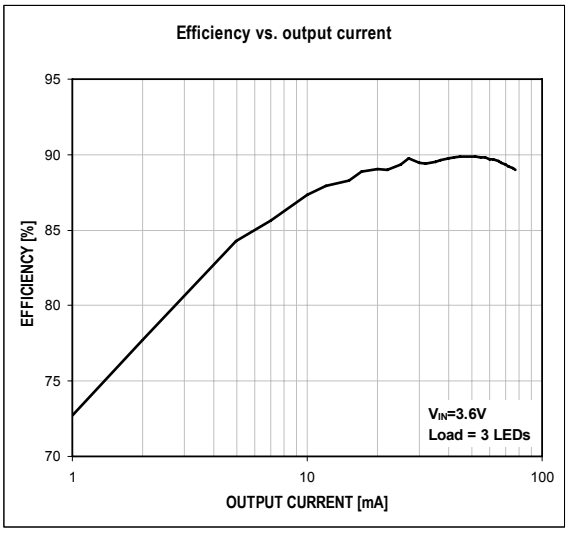
Table 23. DCDC Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SW}	High Voltage Pin	Pin SW15	0		15	V
I_{VDD}	Quiescent Current	Pulse Skipping mode		140		µA
V_{FB}	Feedback Voltage, Transient	Pin ISINK	0		5.5	V
V_{FB}	Feedback Voltage, during Regulation	Pin ISINK		0.63		V

Table 23. DCDC Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{SW_MAX}	Current Limit	V15_ON = 1	350	510	750	mA
R_{SW}	Switch Resistance	V15_ON = 0		0.85	1.54	Ω
I_{LOAD}	Load Current	@ 15V output voltage	0		45	mA
I_{FB}	Current into ISINK1 during voltage feedback mode			50		uA
$V_{PULSESKIP}$	Pulse-skip Threshold	Voltage at pin ISINK, pulse skips are introduces when load current becomes too low		0.96		V
F_{IN}	Fixed Switching Frequency		0.45	0.66	0.85	MHz
C_{OUT}	Output Capacitor	Ceramic		1		µF
L (Inductor)	I_{LOAD} > 20mA	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficiency	17	22	27	µH
	I_{LOAD} < 20mA		8	10	27	
t_{MIN_ON}	Minimum On-Time	Guaranteed per design	90		200	ns
MDC	Maximum Duty Cycle	Guaranteed per design	84	91	98	%

Figure 26. 15V Step-Up Performance Characteristics



9.3.5 Register Description

Table 24. DCDC15 Related Register

Name	Base	Offset	Description
In_Cntr	2-wire serial	1Ah-4	Selection of external dimming input
DCDC15	2-wire serial	1Bh-1	DCDC15 on/off and dimming control
ISINK1	2-wire serial	1Bh-2	ISINK1 current settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 1Ah1, 1Bh-1 to 1Bh-3

9.4 Charger

9.4.1 General

This block can be used to charge a 4V Li-Ion accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (55 to 460mA) and maximum charging voltage (3.9 to 4.25V).

An internal protection circuit will limit the charging current when a CHGIN voltage drop is detected.

For the end of charge current four levels can be selected while the battery temperature shutdown has two temperature levels to choose from.

The current battery voltage as well as the actual charging current can be measured with the general purpose ADC.

Figure 27. Charger Block Diagram

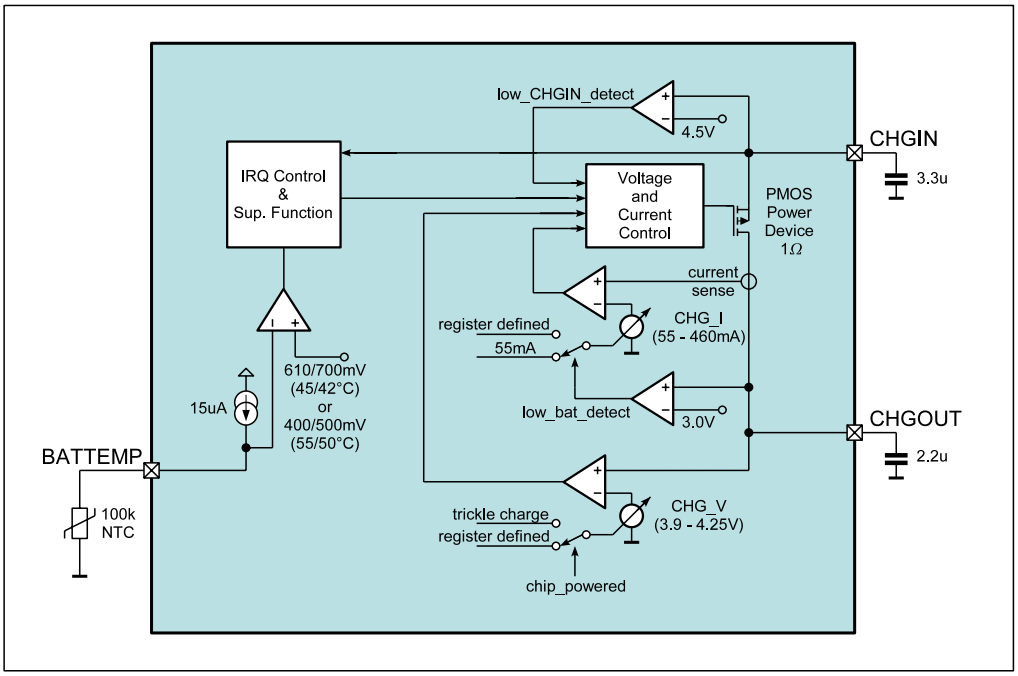
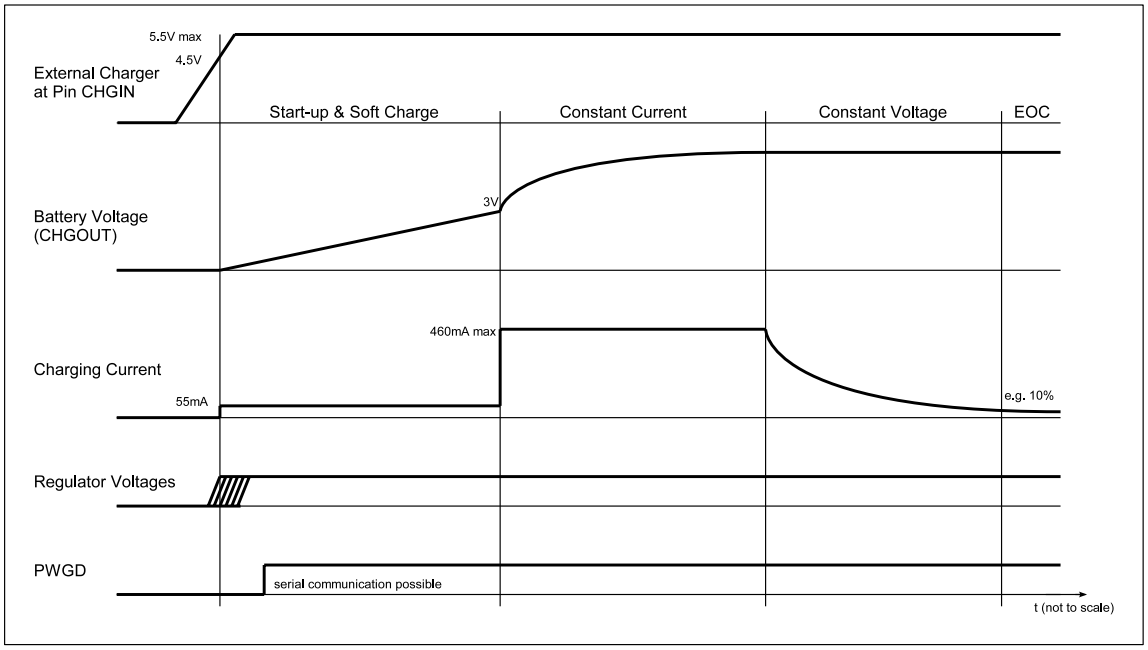


Figure 28. Charger States



9.4.2 Soft Charge

If the battery and therefore CHGOUT is below 3V the charger is working in a fixed soft charge mode with the smallest possible charging current of 55mA and 3.9V charger end voltage. After reaching the 3V level the charger switches to the register defined mode and sets the programmed charging current and voltage.

9.4.3 End of Charge Detection

For the EOC level 4 presets can be selected. This makes it possible to monitor the charging progress also during constant voltage mode. If the EOC level is reached an interrupt can be generated, but it is also possible to poll the charger status bits at any time.

9.4.4 Temperature Supervision

This charger block also features a 15uA supply for an external 100k NTC resistor to measure the battery temperature while charging. If the temperature is too high, an interrupt can be generated. If the battery temperature drops the charger will start charging again. The levels for switching off/on the charger (45/42°C or 55/50°C) can be selected via register settings.

If the NTC resistor does not have 100kΩ its value can be corrected with a resistor in series or in parallel.

9.4.5 Parameter

AVDD27=2.7, T_A= 25°C, unless otherwise mentioned

Table 25. Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CHG} (0-7)	Charging Current	BVDD > 2.7V, I_{CHG} > 70mA	I_{NOM} -8%	I_{NOM}	I_{NOM} +8%	mA
V_{CHG} (0-7)	Charging Voltage	BVDD > 2.7V, end of charge is true	V_{NOM} -50mV	V_{NOM}	V_{NOM} +30mV	V
V_{ON_ABS}	Charger On Voltage IRQ	CHGOUT>3V		3.1	4.0	V
V_{ON_REL}	Charger On Voltage IRQ	CHGIN-CHGOUT		170	240	mV
V_{OFF_REL}	Charger Off Voltage IRQ	CHGIN-CHGOUT	40	77		mV

Table 25. Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BATEMP_ON}	Battery Temp. high level (45 or 55°C)	BVDD >3V		610 or 400		mV
V_{BATEMP_OFF}	Battery Temp. low level (42 or 50°C)	BVDD >3V		700 or 500		mV
I_{CHG_OFF}	End Of Charge current level	BVDD >3V	5% I_{NOM}	10% 30% 50% 70% I_{NOM}	15% I_{NOM}	mA
I_{REV_OFF}	Reverse current shut down	BVDD = 5V, CHGIN open		<1		uA

9.4.6 Register Description

Table 26. Charger Related Register

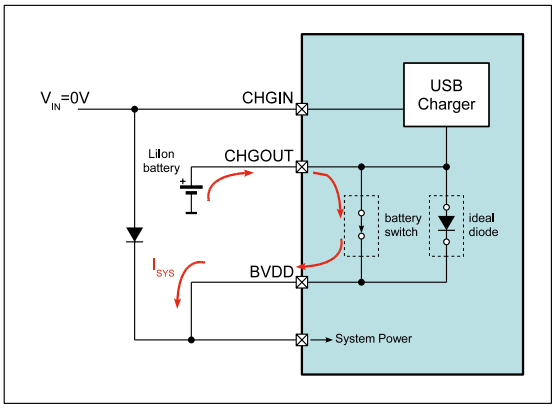
Name	Base	Offset	Description
CHGVBUS1	2-wire serial	19h-1h	Charger voltage, current and temp. supervision control
CHGVBUS2	2-wire serial	19h-2h	Charger temperature and EOC level settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 19h-1 to 19h-2
IRQENRD_2	2-wire serial	25h	Enable/disable EOC and battery over-temperature interrupt Read out charger status
IRQENRD_4	2-wire serial	27h	Set CHGIN debounce time
ADC10_0	2-wire serial	2Eh	ADC source selection, ADC result<9:8>
ADC10_1	2-wire serial	2Fh	ADC result <7:0>

9.5 Battery Switch

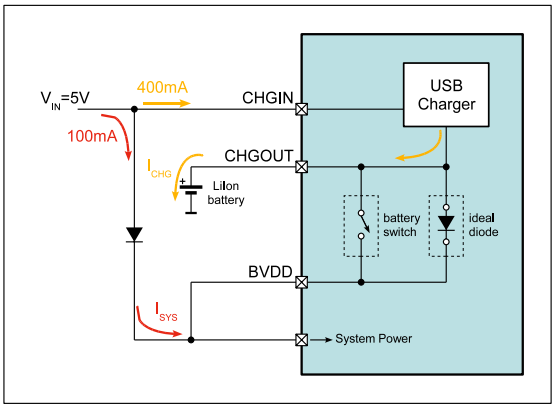
9.5.1 General

An integrated battery switch provides a battery separation during charging. In normal battery operation the switch is closed. With an ideal diode function a smooth transition between the different modes are guaranteed.

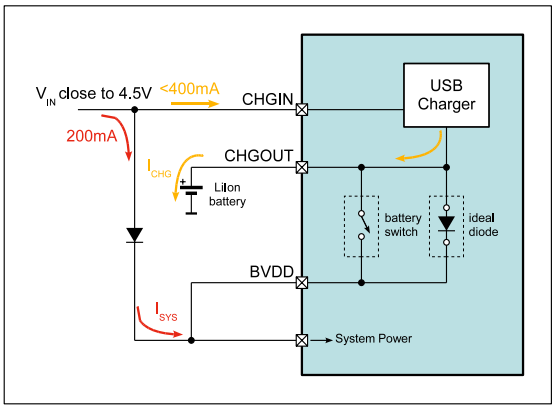
Figure 29. Battery Switch Modes



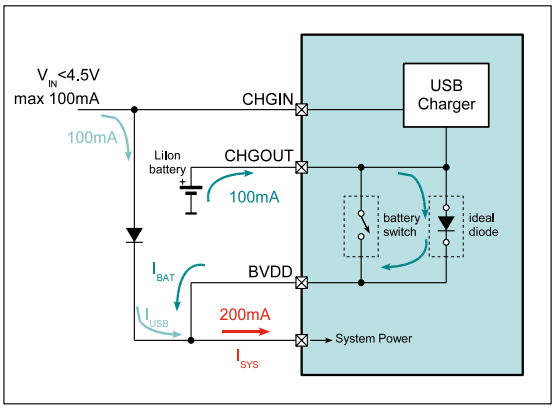
In normal operation, when the charger is not connected, all the system current comes out of the battery



During charging the battery switch opens and the system is supplied direct from the charger input.



If the system current (red) plus the charger current (yellow) is higher than the maximum available current from USB or wall adapter, V_{IN} will drop.
If it comes close to 4.5V the charger will automatically reduce the charging current, which will bring up V_{IN} to its nominal voltage again.



If the system current (red) is higher than the max. available current from e.g. USB, than the additional needed current will be provided from the battery .
To ensure a smooth transition an ideal diode will provide the current till the battery switch closes.
This ideal diode function will also ensure a smooth switchback to battery operation, when the USB or wall adapter connector is plugged out.

10 Detailed Description - SYSTEM Functions

10.1 SYSTEM

10.1.1 General

The system block handles the power up, power down and regulator voltage settings of the AFE.

The PWGD and XRES outputs can be configured to operate in push/pull (2 different driver strengths) open-drain mode or to be tri-state. For a more detailed description of the GPIO functionality of these pins please refer to chapter GPIO Pins on page 48.

10.1.2 Power Up/Down Conditions

The chip powers up when one of the following condition is true:

Table 27. Power UP Conditions

#	Source	Description
1	PWRUP PwUp	ON_KEY High Level at PRWUP pin of >= 1/3 BVDD
2	CHGIN PwUp	Charger Plug-In … High level at CHGIN pin of >= 4.0V
3	VBUS PwUp	USB Plug-In …. High level at VBUS pin of >= 4.5V
4	WAKEUP PwUp	Wake-Up Timer power-up on RTC clock
4	MCLK PwUp	ON_KEY High Level at MCLK pin of >= 1/3 BVDD

The chip automatically shuts off if one of the following conditions arises:

Table 28. Power DOWN Conditions

#	Source	Description
1	SERIF MAJOR PwDn	**Power-Down** by SERIF writing 0h to register 20h This Power-Down clears wake-up as well.
2	Emergency PwDn	**Power-Down** if PWRUP pin is HIGH for 10sec. This time can be reduced to 5sec with bit 7 in register 21h.
3	Wake-Up PwDn	write 4h to reg. 1Ch and 0h to reg. 1Ah … disable heartbeat source Write 3 times to reg.22h to define wake-up time; **Power-Down** by heartbeat without source by writing 9h to reg. 20h
4	Heartbeat PwDn	write 4h to reg. 1Ch and 4h/8h or Ch to reg. 1Ah … select HBT source write 9h to reg. 20h … enable heartbeat with source **Power-Down** if no edge on the selected HBT source is seen for 500ms.
5	SERIF Watch-Dog PwDn	write 3h to reg. 20h … enable SERIF watch-dog **Power-Down** if no SERIF read is seen for 500ms.
6	Junction-Temp PwDn	**Power-Down** if junction temperature rises up to 140degC. This threshold can be lowered with bits <4:0> in reg 21h. This supervisor can be disabled with bit 2 in reg. 20h.
7	BVDD LOW PwDn	**Power-Down** if AVDD27 LDO has 10% under-voltage for more than 680us. This supervisor can get disabled with bit 6 in reg. 21h.
8	PVDD1 LOW PwDn	**Power-Down** if enabled with bit 1 in reg. 23h and PVDD1 LDO has 10% under-voltage for more than 680us.
9	PVDD2 LOW PwDn	**Power-Down** if enabled with bit 3 in reg. 23h and PVDD2 LDO has 10% under-voltage for more than 680us.
10	CVDD1 LOW PwDn	**Power-Down** if enabled with bit 7 in reg. 23h and CVDD1 DCDC has 10% under-voltage for more than 680us.
11	CVDD2 LOW PwDn	**Power-Down** if enabled with bit 1 in reg. 24h and CVDD2 DCDC has 10% under-voltage for more than 680us.

10.1.3 Start-up Sequence

The AFE offers different power-up sequences. While VPRG1 and VPRG2 pins are defining the regulator voltages VPRG3 is setting the sequence of powering on the regulators during the start-up. These pins detect 5 logical input states which shall come from an external resistor divider network.

At first, LDO2 (AVDD27) and LDO1 (AVDD17) are powered up. This cannot be influenced with the selection of specific sequences below. LDO2 is necessary for the internal supply of the AFE, LDO1 could be turned off later if no audio functionality is needed.

After power-up sequence all voltage settings and power on/off conditions of the described regulators can be programmed via the serial interface

Table 29. Start-Up Sequence

	CVDD1	CVDD2	PVDD1	PVDD2
VPRG1 (core)				
open	1.2V			
VPRG2 (peri)				
vdd		2.5V	3.3V	3.3V
150k PU		2.8V	1.8V	3.3V
open		1.8V	3.3V	3.3V
150k PD				
vss		3.3V	3.3V	3.3V
VPRG3 (sequence)				
vdd	1st	2nd	3rd	off
150k PU	1st	2nd	3rd	3rd
open	3rd	2nd	1st	1st
150k PD				
vss	3rd	2nd	1st	off

10.1.4 XRES delay with PWGD pin

With using an exteral capacitor on PWGD, the XRES signal can be delayed. This delay can be calculated with the 10uA pull-up current and a comparator threshold of ~1V. Using a 100nF capacitance will give a delay of 10ms.

10.1.5 Register Description

Table 30. System Related Register

Name	Base	Offset	Description
Out_Cntr1	2-wire serial	1A-1h	Control of PWGD and XRES signal and drive
In_Cntr	2-wire serial	1A-4h	Selection of HBT input pin
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 1Ah-1 and 1Ah-5
SYSTEM	2-wire serial	20h	Watchdog and Over-temperature control, Power down enable
SUPERVISOR	2-wire serial	21h	Set emergency shutdown time
IRQENRD_0	2-wire serial	23h	Enable/disable PMU interrupts
IRQENRD_1	2-wire serial	24h	Enable/disable wake-up, voice and PMU interrupts
IRQENRD_2	2-wire serial	25h	Enable/disable charger, USB and supervisor interrupts
IRQENRD_3	2-wire serial	26h	Enable/disable junction temperature interrupt

10.2 Hibernation

10.2.1 General

Hibernation allows shutting down a part or the complete system. Hibernation can be terminated by every possible interrupt of the AFE. E.g. one can use the RTC for a time triggered wake-up. The interrupt has to be enabled before going to hibernation.:

Table 31. Hibernation

State	Description
Enter	To enter hibernation mode the following settings have to be done: - Enable just these IRQ sources which should lead to leave hibernation mode. - Make sure that IRQ is inactive (IRQ flags get cleared by Reg0x23-27 readings. - Define which regulators should be kept powered and enter hibernation by writing to Reg 1Ch_0x06 + Reg 17h_0xXX Note that hibernation will shutdown regulators which are not in the keep list of the mentioned Reg 17h writing and which are powered by the selected power-up sequence. (e.g. PVDD2 will not go hibernation with VPRG3 is vss or vdd)
Hibernation	VDD27 chip supply is kept ON All other regulators are switched OFF dependent on the KEEP-Bits XRES goes active and PWGD goes inactive.
Leave	The chip will come out of Hibernation with IRQ activation. Start-Up sequence is provided defined by the VPRG state latched on the previous Start-Up. (VPRG state does not get latched again by leaving hibernation)

10.2.2 Register Description

Table 32. Hibernation Related Register

Name	Base	Offset	Description
Hibernation	2-wire serial	17h-6	Hibernation control
PMU_Enable	2-wire serial	1Ch	Enables writings to extended register 17h-6

10.3 Supervisor

10.3.1 General

This supervisor function can be used for automatic detection of BVDD brown out or junction over-temperature condition.

10.3.2 BVDD Supervision

The BVDD supervision interrupt level is set to 175mV above regulator output AVDD27. When BVDD reaches this level an interrupt can be generated.

If AVDD27 reaches the “programmed level of AVDD27” -10% for more than 680us, the AFE shuts down automatically, if the shutdown is not disabled.

10.3.3 Junction Temperature Supervision

The temperature supervision level can also be set by 5 bits (120 to –15ºC). If the temperature reaches this level, an interrupt can be generated. The over-temperature shutdown level is always 20ºC higher.

10.3.4 Power Rail Monitoring

The 4 main regulators as well as the DCDC15 booster and the system supply AVDD27 have an extra monitor which observes the output voltage of the regulators. This power rail monitors are independent from the 10bit ADC. To activate these please see related registers. For a shut down the voltage of the regulator has to be 10% or more below the programmed value for more than 680us.

10.3.5 Register Description

Table 33. Supervisor Related Register

Name	Base	Offset	Description
SUPERVISOR	2-wire serial	21h	Low battery shutdown disable and junction temperature supervision threshold levels
IRQENRD_0	2-wire serial	23h	Enable/disable PVDD/CVDD monitoring interrupt and shutdown
IRQENRD_1	2-wire serial	24h	Enable/disable PVDD/CVDD monitoring interrupt and shutdown
IRQENRD_2	2-wire serial	25h	Enable/disable battery brown out interrupt
IRQENRD_3	2-wire serial	26h	Enable/disable junction temperature interrupt
IRQENRD_4	2-wire serial	27h	Enable/disable AVDD27 and DCDC15 monitoring interrupt

10.4 Interrupt Generation

10.4.1 General

All interrupt sources can get enabled or disabled by corresponding bits in the 5 IRQ-bytes. By default no interrupt source is enabled.

The XIRQ output can be configured to operate in push/pull (2 different driver strengths), open-drain mode or to be tri-state. The signal polarity can be defined as active-low or active-high. Default state is open-drain active-low. For a more detailed description of the GPIO functionality of this pin please refer to chapter GPIO Pins on page 48.

10.4.2 IRQ Source Interpretation

There are 3 different modules to process interrupt sources:

LEVEL

The IRQ output is kept active as long as the interrupt source is present and this IRQ-Bit is enabled

EDGE

The IRQ gets active with a high going edge of this source. The IRQ stays active until the corresponding IRQ-Register gets read.

STATUS CHANGE

The IRQ gets active when the source-state changes. The change bit and the status can be read to notice which interrupt was the source. The IRQ stays active until the corresponding interrupt register gets read.

10.4.3 De-bouncer

There is a de-bounce function implemented for USB and CHARGER. Since these 2 signals can be unstable for the phase of plug-in or unplug, a de-bounce time of 512ms/256ms/128ms/8ms can be selected by 2 bits in the IRQ_ENRD_4 register (27h).

10.4.4 Interrupt Sources

25 IRQ events will activate the XIRQ pin:

- Headphone connected
- Headphone over-current
- Microphone connected
- Microphone remote control
- Voice activation threshold reached
- ■ 10bit ADC end of conversion
- I²S changed (active/inactive)
- USB changed (connect/disconnect)
- Charger changed (end of charge or connect/disconnect)
- Battery temperature high (at 45ºC or 55ºC with 100kΩ NTC)
- Junction temperature high
- RTC watchdog (e.g. after battery was changed)
- Battery low (Brown-out voltage reached)
- Wake-up from hibernation
- Power-up key (pin PWRUP) pressed
- Power rail monitor: over-voltage PVDD1, PVDD2, CVDD1, CVDD2, DCDC15
- Power rail monitor: under-voltage PVDD1, PVDD2, CVDD1, CVDD2, AVDD27

10.4.5 Register Description

Table 34. Interrupt Related Register

Name	Base	Offset	Description
Out_Cntr3	2-wire serial	1A-3h	Control of XIRQ signal, polarity and drive
PMU_Enable	2-wire serial	1Ch	Enables writings to extended register 1Ah-3 and 1Ah-5
IRQENRD_0	2-wire serial	23h	Enable/disable PMU interrupts
IRQENRD_1	2-wire serial	24h	Enable/disable wake-up, voice and PMU interrupts
IRQENRD_2	2-wire serial	25h	Enable/disable charger, USB and supervisor interrupts
IRQENRD_3	2-wire serial	26h	Enable/disable junction temperature, headphone, microphone and I2S interrupt
IRQENRD_4	2-wire serial	27h	Enable/disable PMU, RTC, ADC10 and microphone interrupt, set VBUS and CHGIN debounce time

10.5 Real Time Clock

10.5.1 General

The real time clock is not available in this package, please make sure that the RTC is disabled.

10.5.2 Register Description

Table 35. RTC Related Register

Name	Base	Offset	Description
RTC_Cntr	2-wire serial	28h	RTC oscillator enable, free usable bits

10.6 10-Bit ADC

10.6.1 General

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc.

10.6.2 Input Sources

Table 36. ADC10 Input Sources

#	Source	Range	LSB	Description
0	BVDD	5.120V	5mV	check main system input voltage
1				reserved
2	CHGIN	5.120V	5mV	check charger input voltage
3	CHGOUT	5.120V	5mV	check battery voltage of 4V Li-Ion accumulator
4	VBUS	5.120V	5mV	check USB input voltage
5		5.120V	5mV	Source defined by DC_TEST in register 18h
6	BatTemp	2.048V	2mV	check battery charging temperature
7				reserved
8	MICS	2.048V	2mV	check voltage on MICS for remote control or external voltage measurement
9				reserved
A	I_MICS	1.024mA typ.	2uA	check current of MICS for remote control detection
B				reserved
C	VBE_1uA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = (674 - ADC10<9:0>) / 2
D	VBE_2uA	1.024	1mV	measuring basis-emitter voltage of temperature sense transistor; Tj = (694 - ADC10<9:0>) / 2
E	I_CHGact	1.024V	1mV	check active charger current
F	I_CHGref	1.024V	1mV	check reference charger current

10.6.3 Parameter

AVDD27=2.7, T_A= 25°C, unless otherwise mentioned

Table 37. ADC10 Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ADC_{FS}	ADC Full Scale Range		-	2.16	-	V
T_{CON}	Conversion Time		-	34	50	µs
I_MIC_{FS}	I_MICS Full Scale Range		0.7	1.0	1.4	mA

10.6.4 Register Description

Table 38. ADC10 Related Register

Name	Base	Offset	Description
PMU_Enable	2-wire serial	1Ch	Extended ADC source selection
IRQENRD_4	2-wire serial	27h	Interrupt settings for end of conversion interrupt
ADC10_0	2-wire serial	2Eh	ADC source selection, ADC result<9:8>
ADC10_1	2 wire serial	2Fh	ADC result <7:0>

10.7 GPIO Pins

10.7.1 General

PWGD, XRES, SDO, XIRQ are so called GPIO (general purpose inputs/outputs) as they can feature auxiliary functionality.

If the main pin function is not needed all pins can provide internal clocks or can drive a static HIGH or LOW. Four different clock lines (CLKINT1, CLKINT2, CLK24M, CLK32K) can be selected. Each of these clock lines can drive different frequencies which can be set by register options. In addition some pins can provide a PWM signal. The duty cycle of the PWM output can also be set in the registers.

PWGD, XRES and XIRQ can be configured also as open drain outputs. For all pins the driver strength of the push/pull output mode can be selected.

PWGD, Q24M, Q32K can also be used as inputs for a heartbeat signal or an external dimming signal for the DCDC15 booster.

10.7.2 Internal Source Signals

CLKINT1 Signal

This is an internal signal line which can drive pre defined frequencies of 125Hz, 1kHz, 667kHz or 2MHz. This signal line can be selected as source for the XRES, XIRQ and SDO GPIO output pins.

CLKINT2 Signal

This is an internal signal line which can drive the PLL clock, the clock for the logarithmic dimming of DCDC15 or can be set to static HIGH/LOW. This signal line can be selected as source for the PWGD and XIRQ output pins.

PWM Signal

The duty cycle of the PWM signal can be set in 128 steps plus an option to invert the signal. It ca be used as source for all GPIO outputs other than XIRQ.

10.7.3 Pin Functions

PWGD Pin

Can drive CLKINT2 or the PWM signal as auxiliary function. The output can be configured to operate in push/pull (2 different driver strength) open-drain mode or to be trie-state. It can be used as an input for a heartbeat, external dimming signal or as additional source for the 10-bit general purpose ADC.

Using a capacitor on this pin will delay the XRES signal. Please refer to chapter XRES delay with PWGD pin on page 43. When usig the pin as an ADC input the voltage to be measurted has to be higher than 1V, the XRES delay functionality is than no longer avilable.

XRES Pin

Can drive CLKINT1 or the PWM signal as auxiliary function. The output can be configured to operate in push/pull (2 different driver strengths) open-drain mode or to be trie-state.

The XRES signal can be delayed by using a capacitor on PWGD pin. Please refer to chapter XRES delay with PWGD pin on page 43.

XIRQ Pin

Can drive CLKINT1, CLKINT2 signal as auxiliary function. The output can be configured to operate in push/pull (2 different driver strengths) open-drain mode or to be trie-state. The interrupt signal polarity can be defined as active-low or active-high.

SDO Pin

Can drive CLKINT1 or the PWM signal as auxiliary function. The output can be configured to operate in push/pull (3 different driver strengths) or to be trie-state.

10.7.4 Register Description

Table 39. GPIO Related Register

Name	Base	Offset	Description
Out_Cntr1	2-wire serial	1A-1h	Control of PWGD and XRES signal and drive
reserved	2-wire serial	1A-2h	Control of Q32K signal and drive
Out_Cntr3	2-wire serial	1A-3h	Control of XIRQ signal, polarity and drive
In_Cntr	2-wire serial	1A-4h	Selection of HBT and DCDC 15 dimming input pin
Clk_Cntr	2-wire serial	1A-5h	Selection of clock source or drive level for GPIO pins
PWM_Cntr	2-wire serial	1A-6h	PWM duty cycle and polarity settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 1Ah-1 to 1Ah-6

10.8 12-24MHz Oscillator

10.8.1 General

This oscillator is not available in this package. As the oscillator is default ON, it has to be disabled.

10.8.2 Register Description

Table 40. 12-24MHz Oscillator Related Register

Name	Base	Offset	Description
Clk_Cntr	2-wire serial	1A-5h	Enable/disable oscillator and clock divider settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers A1Ah-5

10.9 Unique ID Code (64 bit OTP ROM)

10.9.1 General

This fuse array is used to store a unique identification number, which can be used for DRM issues. The number is generated and programmed during the production process.

10.9.2 Register Description

Table 41. UID Related Register

Name	Base	Offset	Description
UID_0 to UID_7	2-wire serial	38h to 3Fh	Unique ID register 0 to 7

11 Register Definition

Table 42. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
Audio Registers									
00h	reserved								
01h	reserved								
02h	OUT_R	LOUT 0: HP; 1: LOUT	MUX_C<1:0> 0: SUM; 1: DAC; 2: LIN; 3: MIC		OUTR_VOL<4:0> Gain from MUX_C to HPR/LOUTR= -40.5dB...+6dB				
03h	OUT_L	MUTE_K_ON	STAGE_ON	HPDET_ON	OUTL_VOL<4:0> Gain from MUX_C to HPL/LOUTL= -40.5dB…+6dB				
04h	reserved								
05h	reserved								
06h	MIC_R	MIC_MODE 0: MonoDiff 1: SingleEnd	PRE_GAIN<1:0> 0: 30dB; 1: 36dB; 2: 42dB; 3: reserved		MICR_VOL<4:0> Gain from MicAmp (N4) to Mixer (N12) = -40.5dB...+6dB				
07h	MIC_L	MSUP_OFF	MUTE_D_ON	-	MICL_VOL<4:0> Gain from MicAmp (N4) to Mixer (N13) = -40.5dB...+6dB				
08h	reserved								
09h	reserved								
0Ah	LINE_IN_R	-	-	MUTE_B_OFF	LIR_VOL<4:0> Gain from MUX_E (N27) to Mixer (N10) = -40.5dB...+6dB				
0Bh	LINE_IN_L	LO_DISCHG_OFF	LI_MODE 0: stereo 1: mono	MUTE_G_OFF	LIL_VOL<4:0> Gain from MUX_E (N28) to Mixer (N17) = -40.5dB...+6dB				
0Ch	reserved								
0Dh	reserved								
0Eh	DAC_R	-	-	-	DAR_VOL<4:0> Gain from DAC (N19) to Mixer (N23) = -40.5dB…+6dB				
0Fh	DAC_L	-	-	MUTE_H_OFF	DAL_VOL<4:0> Gain from DAC (N22) to Mixer (N26) = -40.5dB…+6dB				
10h	ADC_R	MUX_A<1:0> 0: MIC; 1: LIN; 2: -; 3: SUM		-	ADR_VOL<4:0> Gain from MUX_A to ADC/Mixer (N9) = -34.5dB...+12dB				
11h	ADC_L	ADC_MODE<1:0> 0: Fdac/2; 1: Fdac/4; 2,3: Fdac/1		MUTE_A_OFF	ADL_VOL<4:0> Gain from MUX_A to ADC/Mixer (N18) = -34.5dB...+12dB				

Table 42. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
12h	DAC_IF	I2S_DIRECT	I2S_LOOP	I2S_ATTEN 0: NoAtten 1: AttenON	SDI_ATTEN<4:0> Attenuation of I2S input data = -48dB...-1.5dB				
13h	reserved								
14h	AudioSet1	ADC_ON	DAC_ON	DAC_GST_ON	SDI_MUTE	-	LIN_ON	-	MIC_ON
15h	AudioSet2	BIAS_OFF	SUM_OFF	SUM_AGC_OFF	-	GAIN_STEP<1:0> 0: 2ms; 1: 4ms; 2: 8ms; 3: no control		VMICS<1:0> 0: VDD17*20/17, 1: VDD17*20/22 2: VDD17*20/27, 3: VDD17*20/32	
16h	AudioSet3	-	MICMIX_OFF	-	ADCMIX_ON	LINMIX_OFF	HP_FASTSTART	-	HPCM_ON
PMU Register									
17h-1	CVDD1	PROG_CVDD1	VSEL_CVDD1>6:0> 0 … OFF 0x01 – 0x40: 0.6V + VSEL * 12.5mV -> (0.6125V – 1.400V) 0x41 – 0x70: 1.4V + (VSEL-0x40) * 25mV ->(1.425V – 2.600V) 0x71 – 0x7F: 2.6V + (VSEL-0x70) * 50mV -> (2.650V – 3.350V)						
17h-2	CVDD2	PROG_CVDD2	VSEL_CVDD2<6:0> 0 … OFF 0x01 – 0x40: 0.6V + VSEL * 12.5mV -> (0.6125V – 1.400V) 0x41 – 0x70: 1.4V + (VSEL-0x40) * 25mV ->(1.425V – 2.600V) 0x71 – 0x7F: 2.6V + (VSEL-0x70) * 50mV -> (2.650V – 3.350V)						
17h-3	reserved								
17h-4	reserved								
17h-5	reserved								
17h-6	Hibernation	-	-	KEEP_PVDD2	KEEP_PVDD1	-	-	KEEP_CVDD2	KEEP_CVDD1
17h-7	DCDC_Cntr	CVDD2_fast 0: Cext=10uF 1: Cext=22uF	CVDD1_fast 0: Cext=10uF 1: Cext=22uF	CVDD2_freq 0: 2MHz 1: 1MHz	CVDD1_freq 0: 2MHz 1: 1MHz	DVM_CVDD2<1:0> 0: immediate; 1: 42us/step; 2: 166us/step; 3: 666us/step		DVM_CVDD1<1:0> 0: immediate; 1: 42us/step; 2: 166us/step; 3: 666us/step	
18h-1	PVDD1	PVDD1_OFF	-	PRG_PVDD1	VSEL_PVDD1<4:0> 0x00 – 0x0F: 1.2V + VSEL * 50mV -> (1.2V – 1.95V) 0x10 – 0x1F: 2.0V + (VSEL-0x10) * 100mV ->(2.0V – 3.5V)				
18h-2	PVDD2	PVDD2_OFF	-	PRG_PVDD2	VSEL_PVDD2<4:0> 0x00 – 0x0F: 1.2V + VSEL * 50mV -> (1.2V – 1.95V) 0x10 – 0x1F: 2.0V + (VSEL-0x10) * 100mV ->(2.0V – 3.5V)				
18h-3	reserved								
18h-4	reserved								
18h-5	reserved								

Table 42. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
18h-6	AVDD27	-	-	PRG_AVDD27	-	VSEL_AVDD27<3:0> 0x0 – 0x2: 2.3V 0x3 – 0xF: 2.0V + VSEL* 100mV ->(2.3V – 3.5V)			
18h-7	AVDD17	AVDD17_OFF	-	PRG_AVDD17	VSEL_AVDD17<4:0> 0x00 – 0x1F: 1.65V + VSEL * 50mV -> (1.65V – 3.2V)				
19h-1	CHGVBUS1	BAT_TEMP_OFF	CHG_I<2:0> 0..3: 55, 70, 140, 210mA 4..7: 280, 350, 420, 460mA			CHG_V<2:0> 3.9V + CHG_V * 50mV -> (3.9V – 4.25V)			CHG_OFF
19h-2	CHGVBUS2	VBUS_COMP_TH <1:0> 0: 4.5V; 1: 3.18V; 2: 1.5V; 3: 0.6V		-	-	-	BAT_TEMP 0: 0.4/0.5V; 1: 0.6/0.7V	CHG_EOC_TH<1:0> 0: 10% CC; 1: 30% CC; 2: 50% CC; 3: 70% CC	
1Ah-1	Out_Cntr1	DRIVE_PWGD<1:0> 0: 6mA OD; 1: 6mA PP; 2: 1mA PP; 3: HiZ		MUX_PWGD<1:0> 0: PWGD; 1: -; 2: CLKINT2; 3: PWM		DRIVE_XRES<1:0> 0: 6mA OD; 1: 6mA PP; 2: 1mA PP; 3: HiZ		MUX_XRES<1:0> 0: XRES; 1: -; 2: CLKINT1; 3: PWM	
1Ah-2	reserved	-		-		-		-	
1Ah-3	Out_Cntr3	DRIVE_SDO<1:0> 0: 6mA PP; 1: HiZ; 2: 2mA PP; 3: 1mA PP		MUX_SDO<1:0> 0: SDO; 1: -; 2: CLKINT1; 3: PWM		DRIVE_XIRQ<1:0> 0: 6mA OD; 1: 6mA PP; 2: 1mA PP; 3: HiZ		MUX_XIRQ<1:0> 0: XIRQ; 1: CLKINT1; 2: CLKINT2; 3: IRQ	
1Ah-4	In_Cntr	-	-	-	-	MUX_HBT<1:0> 0: OFF; 1: PWGD; 2: -; 3: -		MUX_ExtDim<1:0> 0: OFF; 1: PWGD; 2: -; -	
1Ah-5	Clk_Cntr	CLKINT2<1:0> 0: CLKPLL; 1: CLKlogdim; 2: LOW; 3: HIGH		CLKINT1<1:0> 0: 2MHz; 1: 667kHz; 2: 1kHz; 3: 125Hz		CLK24M<1:0> 0: -; 1: -; 2: -; 3: OSC24M_PD		-	
1Ah-6	PWM_Cntr	PWM_INVERT	PWM_CYCLE<6:0> 0: no pulses; 1-127: duty cycle = PWM_CYCLE * 0.39%						
1Ah-7	PLL	OSR<3:0> 0x0: 128; 0x1-0xF: n/a				VCO_MODE<1:0> 0: 24-48kHz; 1: 8-23kHz ; 2: n/a; 3: n/a		PLL_MODE<1:0> 0: automatic; 1: ON; 2: OFF; 3: auto_inv	
1Bh-1	DCDC15	DIM_UP_XDOWN	DIM_RATE<1:0> 0: 0ms; 1: 300ms; 2: 600ms; 3: 1200ms	VFB_ON	ExtDim_ON	-	-	-	
1Bh-2	ISINK1	I_SINK1<4:0> 0: OFF; 1-31: 1.2mA *I;_ISINK1 -> (1.2mA...37.2mA)							
1Bh-3	reserved	-							

Table 42. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
1Ch	PMU_Enable	DC_TEST_MUX <3:0> 0: open; 1: VDD27; 2: VDD17; 3: PVDD1; 4: PVDD2; 5: CVDD1; 6: CVDD2; 7: RVDD; 8: FVDD; 9: PWGD; A-F: not defined				PMU_GATE	PMU_WR_ENABLE <2:0> SubRegister addresses for registers: 0x17: DCDC regulators 0x18: LDOs regulators 0x19: Charger 0x1A: IO_clock_control 0x1B: BackLight_DCDC		
System Register									
20h	SYSTEM	Design_Version<3:0>				HB_WD_ON	JTEMP_OFF	I2C_WD_ON	PWR_HOLD
21h	SUPERVISOR	SD_TIME 0: 10s; 1: 5s	BVDDlow_SD_OFF VDD27-10%	-	JTEMP_SUP<4:0> Temp_ShutDown = 140°C - JTEMP_SUP*5°C -> (140°C...-15°C) TEmp_IRQ = 120°C - JTEMP_SUP*5°C -> (120°C...-35°C)				
23h	IRQENRD_0	CVDD1_SD	CVDD1_IRQ	-	-	PVDD2_SD	PVDD2_IRQ	PVDD1_SD	PVDD1_IRQ
		CVDD1_under	CVDD1_over	-	-	PVDD2_under	PVDD2_over	PVDD1_under	PVDD1_over
24h	IRQENRD_1	PWRUP_IRQ	WAKEUP_IRQ	MCLK_IRQ	-	-	-	CVDD2_SD	CVDD2_IRQ
								CVDD2_under	CVDD2_over
25h	IRQENRD_2	BATTEMP_IRQ	-	-	CHG_IRQ	-	USB_IRQ	RTC_WD	BVDD_LOW
			CHG_EOC	CHG_CON	CHG_changed	USB_CON	USB_changed		
26h	IRQENRD_3	JTEMP_HIGH	-	HP_OVC	-	I2S_IRQ	VOXM_IRQ	MIC_CON	HPH_CON
					I2S_status	I2S_changed			
27h	IRQENRD_4	T_DEB<1:0> 0: 512ms; 1: 256ms; 2: 128ms; 3: 8ms		AVDD27_IRQ	DCDC15_IRQ	-	REM_DET	-	ADC_EOC
				AVDD27_under	DCDC15_over				
28h	RTC_Cntr	Free_Bits<3:0> to be used for application purpose				-		-	OSC_ON
29h	reserved								
2Ah	RTC_0	QRTC<7:0>							
2Bh	RTC_1	QRTC<15:8>							
2Ch	RTC_2	QRTC<23:16>							
2Dh	RTC_3	QRTC<31:24>							
2Eh	ADC10_0	ADC10_MUX<3:0> 0: BVDD; 1: BVDDR; 2: CHGIN; 3: CHGOUT; 4: VBUS 5: DC_TEST; 6: BATTEMP; 7: MCLK; 8: MICS; A: I_MICS; C: VBE_1uA; D: VBE_2uA; E: I_CHGact; F: I_CHGref				-	-	ADC10<9:8>	
2Fh	ADC10_1	ADC10<7:0>							

Table 42. I2C Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
UID Register									
38h	UID_0	ID<7:0>							
39h	UID_1	ID<15:8>							
3Ah	UID_2	ID<23:16>							
3Bh	UID_3	ID<31:24>							
3Ch	UID_4	ID<39:32>							
3Dh	UID_5	ID<47:40>							
3Eh	UID_6	ID<55:48>							
3Fh	UID_7	ID<63:56>							

Table 43. OUT_R Register

Name		Base	Default
OUT_R		**2-wire serial**	**00h**
Offset: 02h		**Right HP/Line Output Register**	
		Configures MUX_C and the audio gain from MUX_C output to HPR/LOUTR output and switches between the headphone and line output. This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LOUT	0	R/W	Switches between headphone and line output **00: headphone enabled** 01: line out enabled
6:5	MUX_C<1:0>	00	R/W	Multiplexes the analog audio inputs to MUX_C output for HPR/L and LOUTR/L **00: Mixer: ΣR to HPR/LOUTR and ΣL to HPL/LOUTL** 01: DAC direct : (N19/ N22), DAC gain stage and mixer are bypassed 10: LineIn direct (N10/N17) 11: Mic direct (N12/N13)
4:0	OUTR_VOL<4:0>	00000	R/W	volume settings for right headphone/line output, adjustable in 32 steps @ 1.5dB; gain from MUX_C to HPR/LOUTR 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 44. OUT_L Register

Name		Base	Default
OUT_L		**2-wire serial**	**00h**
Offset: 03h		**Left HP/Line Output Register**	
		Configures the audio gain from MUX_C output to HPL/LOUTL output and controls MUTE switch K as well as on/off of the stage. This register is reset when the stage is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled	
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MUTE_K_ON	0	R/W	Control of MUTE switch K **0: HP/line output set to mute** 1: normal operation
6	STAGE_ON	0	R/W	**0: HP/line stage not powered** 1: normal operation
5	HPDET_ON	0	R/W	Enables the detection when a headset gets connected. HPCM is used as a sense pin and is biased to 150mV **0: no headphone detection** 1: enable headphone detection
4:0	OUTL_VOL<4:0>	00000	R/W	volume settings for left headphone/line output, adjustable in 32 steps @ 1.5dB; gain from MUX_C to HPL/LOUTRL 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 45. MIC_R Register

Name		Base		Default
MIC_R		**2-wire serial**		**00h**
Offset: 06h		**Right Microphone Input Register**		
		Configures MUX_C and the audio gain from MUX_C output to HPR/LOUTR output and switches between the headphone and line output. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MIC_MODE	0	R/W	Selects the microphone input mode **0: mono differential mode** 1: single ended mode
6:5	PRE_GAIN<1:0>	00	R/W	Sets the gain of the microphone preamplifier (gain from microphone inputs to N3) **00: gain set to 30 dB** 01: gain set to 36 dB 10: gain set to 42 dB 11: reserved, do not use.
4:0	MICR_VOL<4:0>	00000	R/W	volume settings for right microphone input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N4) to mixer input (N12) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 46. MIC_L Register

Name		Base		Default
MIC_L		**2-wire serial**		**00h**
Offset: 07h		**Left Microphone Input Register**		
		Configures the gain from microphone amplifier output up to mixer input (Σ) and controls MUTE switch D. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	MSUP_OFF	0	R/W	**0: microphone supply enabled** 1: microphone supply disabled
6	MUTE_D_ON	0	R/W	Control of MUTE switch D **0: normal operation** 1: microphone input set to mute
5	-	0	n/a	
4:0	MICL_VOL<4:0>	00000	R/W	volume settings for left microphone input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier (N4) to mixer input (N13) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 47. LINE_IN_R Register

Name		Base		Default
LINE_IN_R		**2-wire serial**		**00h**
Offset: 0Ah		**Right Line Input Register**		
		Configures the gain from right analog line input MUX E to mixer input (Σ) and controls MUTE switch B. This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	n/a	
6	-	0	n/a	
5	MUTE_B_OFF	0	R/W	Control of MUTE switch B **0: right line input is set to mute** 1: normal operation
4:0	LIR_VOL<4:0>	00000	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from MUX output (N27) to mixer input (N10) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 48. LINE_IN_L Register

Name		Base		Default
LINE_IN_L		**2-wire serial**		**00h**
Offset: 0Bh		**Left Line Input Register**		
		Configures the gain from analog left line input MUX E to mixer input (Σ) and controls MUTE switch G. This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LO_DISCHG_OFF	0	R/W	**0: normal operation** 1: disables discharge resitors. Need if the line ouptut is directly connected to the line input for useing the same connector.
6	LI_MODE	0	R/W	Selects the line input mode **0: stereo** 1: 2x mono single ended
5	MUTE_G_OFF	0	R/W	Control of MUTE switch G **0: left line input is set to mute** 1: normal operation
4:0	LIL_VOL<4:0>	00000	R/W	volume settings for left line input, adjustable in 32 steps @ 1.5dB; gain from MUX output (N28) to mixer input (N17) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 49. DAC_R Register

Name		Base		Default
DAC_R		**2-wire serial**		**00h**
Offset: 0Eh		**Right DAC Output Register**		
		Configures the gain from DAC output to mixer input (Σ). This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	-	000	n/a	
4:0	DAR_VOL<4:0>	00000	R/W	volume settings for right DAC output, adjustable in 32 steps @ 1.5dB; gain from DAC output (N19) to mixer input (N23) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 50. DAC_L Register

Name		Base		Default
DAC_L		**2-wire serial**		**00h**
Offset: 0Fh		**Left DAC Output Register**		
		Configures the gain from DAC output to mixer input (Σ) and controls MUTE switch H. This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	00	n/a	
5	MUTE_H_OFF	0	R/W	Control of MUTE switch H **0: DAC output is set to mute** 1: normal operation
4:0	DAL_VOL<4:0>	00000	R/W	volume settings for left DAC output, adjustable in 32 steps @ 1.5dB; gain from DAC output (N22) to mixer input (N26) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 51. ADC_R Register

Name		Base		Default
ADC_R		**2-wire serial**		**00h**
Offset: 10h		**Right ADC Input Register**		
		Configures MUX_A and the gain from MUX_A output to the ADC/mixer input (Σ). This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	MUX_A<1:0>	00	R/W	Connect MUX A output to following inputs **00: Microphone (N4/N4)** 01: Line_In1 (N1/N8) 10: - 11: Mixer output (N24/N25)
5	-	0	n/a	
4:0	ADR_VOL<4:0>	00000	R/W	volume settings for right ADC input, adjustable in 32 steps @ 1.5dB; gain from MUX A output to ADC/mixer input (Σ) (N9) 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

Table 52. ADC_L Register

Name		Base		Default
ADC_L		**2-wire serial**		**00h**
Offset: 0Fh		**Left ADC Input Register**		
		Configures the ADC mode, gain from MUX_A output to the ADC/mixer input (Σ) input and controls MUTE switch A. This register is reset when the block is disabled in AudioSet1 register (14h) or at a AVDD27-POR. The register cannot be written when the block is disabled.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	ADC_MODE<1:0>	00	R/W	Devider setting for ADC sampling frequency **00: I2S LRCK / 2** 01: I2S LRCK / 4 10: I2S LRCK 11: I2S LRCK
5	MUTE_A_OFF	0	R/W	Control of MUTE switch A **0: ADC input is set to mute** 1: normal operation
4:0	ADL_VOL<4:0>	00000	R/W	volume settings for left ADC input, adjustable in 32 steps @ 1.5dB; gain from MUX A output to ADC/mixer input (Σ) (N18) 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

Table 53. DAC_IF Register

Name		Base		Default
DAC_IF		**2-wire serial**		**00h**
Offset: 12h		**DAC Interface Register**		
		Configures the DAC interface and digital gain on the I2S input stream. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	I2S_DIRECT	0	R/W	**0: I2S master clock is generated by the internal PLL** 1: signal on MCLK is used as I2S master clock
6	I2S_LOOP	0	R/W	**0: normal operation** 1: ADC output is connected to DAC input
5	I2S_ATTEN	0	R/W	**0: normal operation** 1: digital attenuation on I2S input data (SDI) enabled
4:0	SDI_ATTEN<4:0>	00000	R/W	digital volume settings I2S input data (SDI), adjustable in 32 steps @ 1.5dB; gain from SDI pin to DAC input 11111: -1.5 dB gain 11110: -3 dB gain .. 00001: -46.5 dB gain **00000: -48.0 dB gain**

Table 54. AudioSet1 Register

Name		Base		Default
AudioSet1		**2-wire serial**		**00h**
Offset: 14h		**First Audio Set Register**		
		Powers the various audio inputs and outputs UP or DOWN. **Caution:** This control register resets and holds LineIn, DAC, and ADC related registers in reset. After activation the required register settings need to be re-programmed. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ADC_ON	0	R/W	**0: ADC powered down** 1: ADC enabled for recording
6	DAC_ON	0	R/W	**0: DAC powered down** 1: DAC enabled for playback
5	DAC_GST_ON	0	R/W	**0: DAC gainstage powered down** 1: DAC gainstage enabled (needed for playback via mixer)
4	SDI_MUTE	0	R/W	**0: SDI nromal operation** 1: SDI data muted (set to zero)
3	-	0	n/a	
2	LIN_ON	0	R/W	**0: Line Input powered down** 1: Line Input enabled
1	-	0	n/a	
0	MIC_ON	0	R/W	**0: Microphone Input powered down** 1: Microphone Input enabled

Table 55. AudioSet2 Register

Name		Base		Default
AudioSet2		**2-wire serial**		**00h**
Offset: 15h		**Second Audio Set Register**		
		Control of various audio blocks. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BIAS_OFF	0	R/W	Power-down of the AGND bias if only digital data transfer and PMU functions are used. **0: bias enabled** 1: bias disabled, for power saving in non audio mode
6	SUM_OFF	0	R/W	**0: Mixer stage enabled** 1: Mixer stage powered down
5	SUM_AGC_OFF	0	R/W	Switches the signal limiter OFF (N20/N21) **0: automatic gain control for summing stage enabled** 1: automatic gain control for summing stage disabled
4	-	0	n/a	
3:2	GAIN_STEP<1:0>	00	R/W	Sets the transition time of the auto fading for the output stage **00: 2ms/step** 01: 4ms/step 10: 8ms/step 11: auto fading off
1:0	VMICS<1:0>	00	R/W	Sets the microphone supply output voltage **00: AVDD17*20/17** 01: AVDD17*20/22 10: AVDD17*20/27 11: AVDD17*20/32

Table 56. AudioSet3 Register

Name		Base		Default
AudioSet3		**2-wire serial**		**00h**
Offset: 16h		**Third Audio Set Register**		
		Control of mixer stage inputs and headphone. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	n/a	
6	MICMIX_OFF	0	R/W	**0: microphone input to ΣR and ΣL (N12/N13) on** 1: microphone input to mixer disabled
5	-	0	n/a	
4	ADCMIX_ON	0	R/W	**0: ADC input to mixer disabled** 1: ADC input to ΣR and ΣL (N12/N13) on
3	LINMIX_OFF	0	R/W	**0: line input to ΣR and ΣL (N12/N13) on** 1: line input to mixer disabled
2	HP_FASTSTART	0	R/W	**0: normal operation** 1: shortens delay for start-up when using 220nF on HPGND
1	-	0	n/a	
0	HPCM_ON	0	R/W	**0: headphone common mode buffer is switched off** 1: headphone common mode buffer is powerd up

Table 57. CVDD1 Register

Name		Base		Default
CVDD1		**2-wire serial**		**00h**
Offset: 17h-1		**CVDD1 DC/DC Buck Regulator Control Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PROG_CVDD1	0	R/W	Selects the control mode for CVDD1 **0: CVDD1 is in default mode controlled by pin VPRG1** 1: CVDD1 is register controlled (Reg. 17-1h)
6:0	VSEL_CVDD1>6:0>	000000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h: DC/DC powered down** 01h-40h: CVDD1=0.6V+VSEL_CVDD1*12.5mV 41h-70h: CVDD1=1.4V+VSEL_CVDD1*25mV 71h-7Fh: CVDD1=2.6V+VSEL_CVDD1*50mV

Table 58. CVDD2 Register

Name		Base		Default
CVDD2		**2-wire serial**		**00h**
Offset: 17h-2		**CVDD2 DC/DC Buck Regulator Control Register**		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PROG_CVDD2	0	R/W	Selects the control mode for CVDD2 **0: CVDD2 is in default mode controlled by pin VPRG2** 1: CVDD2 is register controlled (Reg. 17-1h)
6:0	VSEL_CVDD2<6:0>	000000	R/W	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h: DC/DC powered down** 01h-40h: CVDD1=0.6V+VSEL_CVDD1*12.5mV 41h-70h: CVDD1=1.4V+VSEL_CVDD1*25mV 71h-7Fh: CVDD1=2.6V+VSEL_CVDD1*50mV

Table 59. Hibernation Register

Name		Base		Default
Hinbernation		**2-wire serial**		**00h**
Offset: 17h-6		**PMU Hibernation Control Register**		
		Hibernation starts when writing this register. This is an extended register and needs to be enabled by writing 110b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	00	n/a	
5	KEEP_PVDD2	0	R/W	Keeps the programmed PVDD2 level during hibernation. **0: power down PVDD2** 1: keep PVDD2
4	KEEP_PVDD1	0	R/W	Keeps the programmed PVDD1 level during hibernation. **0: power down PVDD1** 1: keep PVDD1
3:2	-	00	n/a	
1	KEEP_CVDD2	0	R/W	Keeps the programmed CVDD2 level during hibernation. **0: power down CVDD2** 1: keep CVDD2
0	KEEP_CVDD1	0	R/W	Keeps the programmed PVDD1 level during hibernation. **0: power down CVDD1** 1: keep CVDD1

Table 60. DCDC_Cntr Register

Name		Base		Default
DCDC_Cntr		**2-wire serial**		**00h**
Offset: 17h-7		**DC/DC Step Down Control Register**		
		This is an extended register and needs to be enabled by writing 111b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD2_fast	0	R/W	Selects a faster regulation mode for CVDD2 suitable for larger load changes. **0: normal mode, Cext=10uF** 1: fast mode, Cext=22uF required
6	CVDD1_fast	0	R/W	Selects a faster regulation mode for CVDD1 suitable for larger load changes. **0: normal mode, Cext=10uF** 1: fast mode, Cext=22uF required
5	CVDD2_freq	0	R/W	Selects the switching frequency for DCDC2 **0: 2MHz** 1: 1MHz
4	CVDD1_freq	0	R/W	Selects the switching frequency for DCDC2 **0: 2MHz** 1: 1MHz

Table 60. DCDC_Cntr Register

Name		Base		Default
DCDC_Cntr		**2-wire serial**		**00h**
Offset: 17h-7		**DC/DC Step Down Control Register**		
		This is an extended register and needs to be enabled by writing 111b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:2	DVM_CVDD2<1:0>	00	R/W	Configures the dynamic voltage management (output voltage slope) for CVDD2 **00: immediate change of the output voltage** 01: 42us/step 02:166us/step 03: 666us/step
1:0	DVM_CVDD1<1:0>	00	R/W	Configures the dynamic voltage management (output voltage slope) for CVDD1 **00: immediate change of the output voltage** 01: 42us/step 02:166us/step 03: 666us/step

Table 61. PVDD1 Register

Name		Base		Default
PVDD1		**2-wire serial**		**00h**
Offset: 18h-1		**PVDD1 Control Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVDD1_OFF	0	R/W	Switches off PVDD1 regulator **0: normal mode** 1: PVDD1 switched off
6	-	0	n/a	
5	PRG_PVDD1	0	R/W	Selects the output voltage control mode for PVDD1 **0: PVDD1 is in default mode controlled by pin VPRG2** 1: PVDD1 is register controlled (Reg. 18-1h)
4:0	VSEL_PVDD1<4:0>	00000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is selcted by pin VPROG2) 0x00-0x0F: 1.2V+VSEL*50mV ->(1.2V - 1.95V) 0x10-0x1F: 2.0V + (VSEL-0x10)*100mV -> (2.0V-3.5V)

Table 62. PVDD2 Register

Name		Base		Default
PVDD2		**2-wire serial**		**00h**
Offset: 18h-2		**PVDD2 Control Register**		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVDD2_OFF	0	R/W	Switches off PVDD2 regulator **0: normal mode** 1: PVDD1 switched off
6	-	0	n/a	
5	PRG_PVDD2	0	R/W	Selects the output voltage control mode for PVDD2 **0: PVDD2 is in default mode controlled by pin VPRG2** 1: PVDD2 is register controlled (Reg. 18-2h)
4:0	VSEL_PVDD2<4:0>	00000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is selcted by pin VPRG2) 0x00-0x0F: 1.2V+VSEL*50mV ->(1.2V - 1.95V) 0x10-0x1F: 2.0V + (VSEL-0x10)*100mV -> (2.0V-3.5V)

Table 63. AVDD27 Register

Name		Base		Default
AVDD27		**2-wire serial**		**00h**
Offset: 18h-6		**AVDD27 Control Register**		
		This is an extended register and needs to be enabled by writing 110b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	n/a	
6	-	0	n/a	
5	PRG_AVDD27	0	R/W	Selects the output voltage control mode for AVDD27 **0: AVDD27 is in default mode (2.7V)** 1: AVDD27 is register controlled (Reg. 18-6h)
5	-	0	n/a	
3:0	VSEL_AVDD27<3:0>	0000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is 2.7V) 0x0-0x2: 2.3V 0x3-0xF: 2.0V + VSEL*100mV -> (2.3V-3.5V)

Table 64. AVDD17 Register

Name		Base		Default
AVDD17		**2-wire serial**		**00h**
Offset: 18h-7		**AVDD17 Control Register**		
		This is an extended register and needs to be enabled by writing 111b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	AVDD17_OFF	0	R/W	Switches off AVDD17 regulator **0: normal mode** 1: AVDD17 switched off, no audio functions possible
6	-	0	n/a	
5	PRG_AVDD17	0	R/W	Selects the output voltage control mode for AVDD17 **0: AVDD17 is in default mode (1.7V)** 1: AVDD17 is register controlled (Reg. 18-7h)
4:0	VSEL_AVDD17<4:0>	0000	R/W	Sets the LDO output voltage in register control mode (default voltage of the regulator is 1.7V) 0x00-0x1F: 1.65V + VSEL*100mV -> (1.65V-3.2V)

Table 65. CHGVBUS1 Register

Name		Base		Default
CHGVBUS1		**2-wire serial**		**00h**
Offset: 19h-1		**Charger / VBUS 1 Control Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BAT_TEMP_OFF	0	R/W	**0: enables 15uA supply for external 100k NTC resistor** 1: disables supply
6:4	CHG_I<2:0>	000	R/W	set maximum charging current during constant current charging 111: 460 mA 110: 420 mA 101: 350 mA 100: 280 mA 011: 210 mA 010: 140 mA 001: 70 mA **000: 55 mA**
3:1	CHG_V<2:0>	000	R/W	set maximum charger voltage in 50mV steps for the constant voltage charging 111: 4.25 V 110: 4.2 V .. 001: 3.95 V **000: 3.9 V**
0	CHG_OFF	0	R/W	**0: enables Charger** 1: disables Charger

Table 66. CHGVBUS2 Register

Name		Base		Default
CHGVBUS2		**2-wire serial**		**00h**
Offset: 19h-2		**Charger / VBUS 2 Control Register**		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	VBUS_COMP_TH <1:0>	00	R/W	Sets the threshold for the VBUS comparator. The output can be read in register 25h. **00: 4.5V** 01: 3.18V 10: 1.5V 11: 0.6V
5:3	-	000	n/a	-
2	BAT_TEMP	0	R/W	Selects the battery temperature supervision level **0: 0.4/0.5V equal to 55/50°C with 100k NTC** 1: 0.6/0.7V equal to 45/42°C with 100k NTC
1:0	CHG_EOC_TH<1:0>	00	R/W	Setes the threshold for the charger EOC (end of charge) interrupt as a ratio of the constant current (CC) setting. **00: 10% CC** 01: 30% CC 10: 50% CC 11: 70% CC

Table 67. Out_Cntr1 Register

Name		Base		Default
Out_Cntr1		**2-wire serial**		**00h**
Offset: 1Ah-1		**PWGD and XRES Output Control Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	DRIVE_PWGD<1:0>	00	R/W	Sets the PWGD output pin to open-drain, push-pull or tri-state and sets various driving strengths **00: 6mA open-drain output** 01: 6mA push-pull output 10: 1mA push-pull output 11: HiZ, stri-state
5:4	MUX_PWGD<1:0>	00	R/W	Multiplexes various digital signals to the PWGD output pin **00: PWGD, PowerGood control signal** 01: - 10: CLKINT2, internal clock signal, see Clk_Cntr regsiter 11: PWM, PMW_Cntr register

Table 67. Out_Cntr1 Register

Name		Base		Default
Out_Cntr1		**2-wire serial**		**00h**
Offset: 1Ah-1		**PWGD and XRES Output Control Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:2	DRIVE_XRES<1:0>	00	R/W	Sets the XRES output pin to open-drain, push-pull or tri-state and sets various driving strengths **00: 6mA open-drain output** 01: 6mA push-pull output 10: 1mA push-pull output 11: HiZ, stri-state
1:0	MUX_XRES<1:0>	00	R/W	Multiplexes various digital signals to the XRES output pin **00: XRES, active low reset signal** 01: - 10: CLKINT1, internal clock signal, see Clk_Cntr regsiter 11: PWM, PMW_Cntr register

Table 68. Out_Cntr3 Register

Name		Base		Default
Out_Cntr3		**2-wire serial**		**00h**
Offset: 1Ah-3		**SDO and XIRQ Output Control Register**		
		This is an extended register and needs to be enabled by writing 011b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	DRIVE_SDO<1:0>	00	R/W	Sets the SDO output pin to push-pull or tri-state and sets various driving strengths **00: 6mA push-pull output** 01: HiZ, stri-state 10: 2mA push-pull output 11: 1mA push-pull output
5:4	MUX_SDO<1:0>	00	R/W	Multiplexes various digital signals to theSDO output pin **00: SDO, serial data output of the audio ADC** 01: - 10: CLKINT1, internal clock signal, see Clk_Cntr regsiter 11: PWM, PMW_Cntr register
3:2	DRIVE_XIRQ<1:0>	00	R/W	Sets the XIRQ output pin to open-drain, push-pull or tri-state and sets various driving strengths **00: 6mA open-drain output** 01: 6mA push-pull output 10: 1mA push-pull output 11: HiZ, stri-state
1:0	MUX_XIRQ<1:0>	00	R/W	Multiplexes various digital signals to the XRES output pin **00: XIRQ, active low interrupt request signal** 01: CLKINT1, internal clock signal, see Clk_Cntr regsiter 10: CLKINT2, internal clock signal, see Clk_Cntr regsiter 11: IRQ, active low reset signal

Table 69. In_Cntr Register

Name		Base		Default
In_Cntr		**2-wire serial**		**00h**
Offset: 1Ah-4		**HBT and Dimming Input Control Register**		
		This is an extended register and needs to be enabled by writing 100b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	0000	n/a	
3:2	MUX_HBT<1:0>	00	R/W	Selects the HBT (heartbeat) input pin **00: OFF, heartbeat input deactivated** 01: PWGD pin 10: - 11: -
1:0	MUX_ExtDim<1:0>	00	R/W	Selects the input pin for external dimming of the DCDC15 **00: OFF, no pin selected** In this mode the current sinks can be used without enabling the DCDC15. ExtDim_ON bit has to be set in DCDC15 register. 01: PWGD pin 10: - 11: -

Table 70. Clk_Cntr Register

Name		Base		Default
Clk_Cntr		**2-wire serial**		**00h**
Offset: 1Ah-5		**Clock Control Register**		
		This is an extended register and needs to be enabled by writing 101b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	CLKINT2<1:0>	00	R/W	Selects the CLKINT2 input source. Note, this is an internal clock, which can be multiplexed to one of the GPIO ouptus. **00: CLKPLL, internal PLL clock** 01: CLKlogdim, clock used for dimming the DCDC15 10: LOW, drives the signal to logic “0” 11: HIGH, drives the signal to logic “1”
5:4	CLKINT1<1:0>	00	R/W	Selects the CLKINT1 frequency. Note, this is an internal clock, which can be multiplexed to one of the GPIO ouptus. **00: 2MHz** 01: 887kHz 10: 1kHz 11: 125Hz
3:2	CLK24M<1:0>	00	R/W	Disables the 24MHz oszillator, please set to 11b. **00: OSC24MHz enabled** 01: - 10: - 11: OSC24MHz_PD, OSC24M is set to power down
1:0	-	00	n/a	

Table 71. PWM_Cntr Register

Name		Base		Default
PWM_Cntr		**2-wire serial**		**00h**
Offset: 1Ah-6		**PWM Control Register**		
		This is an extended register and needs to be enabled by writing 110b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWM_INVERT	0	R/W	PWM output polarity **0: not inverted** 1: inverted
6:0	PWM_CYCLE<6:0>	0000000	R/W	Sets the PWM duty cycle **0: no pulses** 1-127: duty cycle = PWM_CYCLE * 0,39%

Table 72. PLL Register

Name		Base		Default
PLL		**2-wire serial**		**00h**
Offset: 1Ah-7		**PLL Register**		
		This is an extended register and needs to be enabled by writing 111b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	OSR<3:0>	0000	R/W	Sets the oversampling rate when using the internal PLL **0x0: 128** 0x1-0xF: n/a
3:2	VCO_MODE<1:0>	00	R/W	Selects the speed of the PLL VCO according to the audio sampling frequency. **00: normal: 24-48kHz** 01: low: 8-23kHz 10: n/a 11: n/a
1:0	PLL_MODE<1:0>	00	R/W	Selects the PLL mode and master clock frequency source **00: automatic** turns PLL on, PLL clock is used as master clock if freq(LRCK) >8kHz and freq(MCLK)<32*freq(LRCK) 01: ON; turns PLL on, PLL clock is used asmaster clock 10: OFF; turns the PLL off, MCLK is used as master clock 11: auto_inv; like outomatic but with inverted clock

Table 73. DCDC15 Register

Name		Base		Default
DCDC15		**2-wire serial**		**00h**
Offset: 1Bh-1		**DCDC15 Register**		
		This is an extended register and needs to be enabled by writing 001b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	DIM_UP_XDOWN	0	R/W	**0: disables the step-up converter and dims it down** 1: enables the step-up converter and dims it up
6:5	DIM_RATE<1:0>	00	R/W	Selects the dimming speed when enabling or disablilng the DCDC15 **00: 0ms** 01: 300ms 10: 600ms 11: 1200ms
4	VFB_ON	0	R/W	**0: current feedback selected via ISINK1 and ISINK2** 1: voltage feedback selected, ISINK1 is sinking 50uA to define the voltage via an external zener diode
3	ExtDim_ON	0	R/W	**0: selects internal clock for dimming** 1: selects external clock for dimming
2:0	-	000	n/a	

Table 74. ISINK1 Register

Name		Base		Default
ISINK1		**2-wire serial**		**00h**
Offset: 1Bh-2		**ISINK1 Register**		
		This is an extended register and needs to be enabled by writing 010b to Reg. 1Ch first. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	I_SINK1<4:0>	00000	R/W	sets the current into current sink 1in 1.2mA steps **0: OFF, current sink 1 disabled** 1-31 1.2mA * I_SINK1 -> (1.2mA...37.2mA)
2:0	-	000	n/a	

Table 75. PMU_Enable Register

Name		Base		Default
PMU_Enable		**2-wire serial**		**00h**
Offset: 1Ch-2		**PMU_Enable Register**		
		Selects the extended register on address 17h to 1Bh and enables writng to these PMU register. It also sets the ADC10 multiplexer to measure various regulator voltages This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	DC_TEST_MUX <3:0>	0000	R/W	Allows multiplexing internal and external supply voltages to one DC test node which can be further multiplexed to the ADC10. The accuracy is 5mV/LSB (see reg. 2Eh) **0x0: open** 0x1: AVDD27 0x2: AVDD17 0x3: PVDD1 0x4: PVDD2 0x5: CVDD1 0x6: CVDD2 0x7: RVDD 0x8: FVDD 0x9: PWGD 0xA-0xF: n/a
3	PMU_GATE	000	R/W	Enables all settings made in registers 17h to 1Bh at once. If this bit is set, changes are activated as soon as they are written to the related register. **0: no change** 1: change at once
2:0	PMU_WR_ENABLE <2:0>	000	R/W	Selects extended registers 17h to 1Bh for the next write **0: no register selected** 1: 17h-1 to 1Bh-1 selected 2: 17h-2 to 1Bh-2 selected ... 7: 17h-7 to 1Bh-7 selected

Table 76. SYSTEM Register

Name		Base		Default
SYSTEM		**2-wire serial**		**41h**
Offset: 20h		**SYSTEM Register**		
		This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Design_Version<3:0>	0100	R	AFE number to identify the design version 0100: for chip version 3v0
3	HB_WD_ON	0	R/W	Heartbeat (HBT) Watchdog The watchdog counter will be reset by a rising edge at the HBT input pin which has to occur at least every 500ms. If the watchdog counter is not reset, the AFE will be powered down. **0: HBT watchdog is disabled** 1: HBT watchdog is enabled
2	JTEMP_OFF	0	R/W	Junction temperature supervision (level can be set in register 21h) **0: temperature supervision enabled** 1: temperature supervision disabled
1	I2C_WD_ON	0	R/W	2-wire serial interface watchdog To reset the watchdog counter a 2-wire serial read operation has to be performed at least every 500ms. If the watchdog counter is not reset, the AFE will be powered down. **0: watchdog is disabled** 1: watchdog is enabled
0	PWR_HOLD	0	R/W	**0: power up hold is cleared and AFE will power down** 1: is automatically set to on after power on

Table 77. SUPERVISOR Register

Name		Base		Default
SUPERVISOR		**2-wire serial**		**00h**
Offset: 21h		**SUPERVISOR Register**		
		This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	SD_TIME	0100	R/W	Sets the emergency shut-down time invoked by PWRUP. **0: 5.4sec** 1: 10.9sec
6	BVDDlow_SD_OFF	0	R/W	**0: BVDDlow shut down enalbed** 1: BVDDlow shut down disabled
5	-	0	n/a	
4:0	JTEMP_SUP<4:0>	0	R/W	Sets the threshold for junction temperature emergency shutdown and junction temperature interrupt Invoke shutdown at: JTemp_SD=140-JTEMP_Sup*5°C Invoke interrupt at: JTemp_IRQ=120-JTEMP_Sup*5°C

JT_Sup	IRQ	Shutdown
00000	**120°C**	**140°C**
00001	115°C	135°C
.	.	.
.	.	.
11110	-30°C	-10°C
11111	-35°C	-15°C

Table 78. First Interrupt Register

Name		Base		Default
IRQENRD_0		**2-wire serial**		**00h**
Offset: 23h		**First Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	CVDD1_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD1 occurs **0: disable** 1: enable
	CVDD1_under	x	R	This bit is set when a –5% under-voltage at CVDD1 occurs
6	CVDD1_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD1 **0: disable** 1: enable
	CVDD1_over	x	R	This bit is set when a +8% over-voltage at CVDD1 occurs
5:4	-	00	n/a	
3	PVDD2_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at PVDD2 occurs **0: disable** 1: enable
	PVDD2_under	x	R	This bit is set when a –5% under-voltage at PVDD2 occurs
2	PVDD2_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of PVDD2 **0: disable** 1: enable
	PVDD2_over	x	R	This bit is set when a +5% over-voltage at PVDD2 occurs
1	PVDD1_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at PVDD1 occurs **0: disable** 1: enable
	PVDD1_under	x	R	This bit is set when a –5% under-voltage at PVDD1 occurs
0	PVDD1_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of PVDD1 **0: disable** 1: enable
	PVDD1_over	x	R	This bit is set when a +5% over-voltage at PVDD1 occurs

Table 79. Second Interrupt Register

Name		Base		Default
IRQENRD_1		**2-wire serial**		**00h**
Offset: 24h		**Second Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWRUP_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the PWRUP input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. BVDD/3 at the PWRUP input pin occurs (PWRUP pin is commonly connected to the power-up button)
6	WAKEUP_IRQ	0	W	Enables interrupt which is invoked whenever a wake-up from RTC wake-up counter occurs **0: disable** 1: enable
		x	R	This bit is set when a wake-up has been invoked by the RTC wake-up counter.
5	MCLK_IRQ	0	W	Enables interrupt which is invoked whenever a high signal at the MCLK input pin occurs **0: disable** 1: enable
		x	R	This bit is set whenever a high level of min. BVDD/3 at the MCLK input pin occurs (MCLK pin can be used as alternative power-up button)
4:2	-	0	n/a	
1	CVDD2_SD	0	W	Invokes shut-down of AFE when a –10% under-voltage spike at CVDD2 occurs **0: disable** 1: enable
	CVDD2_under	x	R	This bit is set when a –5% under-voltage at CVDD2 occurs
0	CVDD2_IRQ	0	W	Enables interrupt for over-voltage/under-voltage supervision of CVDD2 **0: disable** 1: enable
	CVDD2_over	x	R	This bit is set when a +8% over-voltage at CVDD2 occurs

Table 80. Thrid Interrupt Register

Name		Base		Default
IRQENRD_2		**2-wire serial**		**00h**
Offset: 25h		**Third Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BATTEMP_IRQ	0	W	Battery over-temperature interrupt setting. **0: disable** 1: enable interrupt if battery temperature exceeds 45/55°C The interrupt must not be enabled if the charger block and battery temperature supervision is disabled
		x	R	Battery over-temperature interrupt reading **0: battery temperature below 45/55°C** 1: battery temperature was too high and the charger was turned off. The charger will be turned on again, when the temperature gets below 42/50°C
6	CHG_EOC	x	R	Battery end of charge interrupt reading **0: battery charging in progress** 1: charging is complete, charging current is below 10% of nominal current, turn off charger
5	CHG_CON	x	R	0: no charger input source connected 1: charger input source connected, also valid if charger is connected during wakeup
4	CHG_IRQ	0	W	Charger status change interrupt setting **0: disable** 1: enables an interrupt on a low to high or high to low change of CHGIN pin or on an EOC condition
	CHG_changed (status change)	x	R	Charger input status change interrupt reading 0: charger status not changed 1: charger status changed, check CHG_CON, CHG_EOC
3	USB_CON	0	n/a	0: no USB input connected 1: USB input connected, also valid if USB is connected during wakeup. The threshold can be set in the USB_UTIL register (1Ah)
2	USB_IRQ	0	W	USB input status change interrupt setting **0: disable** 1: enables an interrupt on a low to high or high to low change of VBUS pin. The threshold can be set in the USB_UTIL register (1Ah)
	USB_changed (status change)	x	R	USB input status change interrupt reading 0: USB input status not changed 1: USB input status changed, check USB_CON

Table 80. Thrid Interrupt Register

Name		Base		Default
IRQENRD_2		**2-wire serial**		**00h**
Offset: 25h		**Third Interrupt Register**		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while with reading you get the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	RTC_WD (level)	0	W	Real time clock watchdog interrupt setting **0: disable** 1: enable
		x	R	Real time clock watchdog interrupt reading **0: RTC o.k.** 1: RTC oszillator was stopped, RTC not longer valid The interrupt gets set in hibernation or during power-up even if the interrupt is not enabled thus allowing to recognise a change of the battery connected to BVDDR during hibernation or shutdown. For a valid reading, the interrupt has to be enabled first.
0	BVDD_LOW (level)	0	W	BVDD under-voltage supervisor interrupt setting **0: disable** 1: enable
		x	R	BVDD supervisor interrupt setting **0: BVDD is above brown out level** 1: BVDD has reached brown out level The threshold can be set in the SUPERVISOR register (21h)

Table 81. Fourth Interrupt Register

Name		Base		Default
IRQENRD_3		**2-wire serial**		**00h**
Offset: 26h		**Fourth Interrupt Register**		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	JTEMP_HIGH (level)	0	W	Supervisor junction over-temperature interrupt setting **0: disable** 1: enable
		x	R	Supervisor junction over-temperature interrupt reading 0: chip temperature below threshold 1: chip temperature has reached the threshold The threshold can be set in the SUPERVISOR register (21h)
6	-	0	n/a	

Table 81. Fourth Interrupt Register

Name		Base		Default
IRQENRD_3		**2-wire serial**		**00h**
Offset: 26h		**Fourth Interrupt Register**		
		Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	HP_OVC (level)	0	W	Headphone over-current interrupt setting **0: disable** 1: enable The interrupt must not be enabled if the headphone block is disabled
		x	R	Headphone over-current interrupt reading 0: no over-current detected 1: headphone over-current detected, headphone amplifier was shut down. The current thresholds are 150mA at HPR / HPL pin or 300mA at HPCM pin.
4	I2S_status	x	R	0: no LRCK on I2S interface detected 1: LRCK on I2S interface present
3	I2S_IRQ	0	W	I2S input status change interrupt setting **0: disable** 1: enable
	I2S_changed (status change)	x	R	I2S input status change interrupt reading 0: I2S input status not changed 1: I2S input status changed, check I2S_status
2	VOXM_IRQ	0	W	Enables interrupt which is invoked by reaching a voltage threshold at the MIC input (voice activation) **0: disable** 1: enable
		x	R	This bit is set when a voltage threshold of 5mV$_{RMS}$ (unfiltered) at the MIC has been reached (voice activation)
1	MIC_CON (level)	0	W	Microphone connect detection interrupt setting **0: disable** 1: enable
		x	R	Microphone connect detection interrupt reading 0: no microphone connected to MIC input 1: microphone connected at MIC input. This interrupt is only invoked when the microphone stage is powered down. The IRQ will be released after enabling the microphone stage. Detecting a microphone during operation has to be done by measuring the supply current
0	HPH_CON (level)	0	W	Headphone connect detection interrupt setting **0: disable** 1: enable
		x	R	Headphone connect detection interrupt reading 0: no headphone connected 1: headphone connected This interrupt is only invoked when the headphone stage is powered down. The IRQ will be released after enabling the headphone stage. Detecting a headphone during operation is not possible.

Table 82. Fifth Interrupt Register

Name		Base		Default
IRQENRD_4		**2-wire serial**		**00h**
Offset: 27h		**Fifth Interrupt Register** Please be aware that writing to this register will enable/disable the corresponding interrupts, while reading gets the actual interrupt status and will clear the register at the same time. It is not possible to read back the interrupt enable/disable settings. This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	T_DEB<1:0>	00	R/W	Sets the USB and Charger connect de-bounce time: **00: 512ms** 01: 256ms 10: 128ms 11: 0ms
5	AVDD27_IRQ	0	W	Enables interrupt for under-voltage supervision of AVDD27 **0: disable** 1: enable
	AVDD27_under	x	R	This bit is set when a -5% under-voltage at AVDD27 occurs
4	DCDC15_IRQ	0	W	Enables interrupt for over-voltage supervision of SW15 **0: disable** 1: enable
	DCDC15_over	x	R	This bit is set when SW15 exceeds 15V.
3	-	0	n/a	
2	REM_DET (edge)	0	W	Microphone remote key press detection interrupt setting **0: disable** 1: enable
		x	R	Microphone remote key press detection interrupt reading 0: no key press detected 1: Microphone supply current got increased, remote key press detected -> measure MICS supply current
1	-	0	n/a	
0	ADC_EOC (edge)	0	W	ADC end of conversion interrupt setting **0: disable** 1: enable
		x	R	ADC end of conversion interrupt reading 0: ADC conversion not finished 1: ADC conversion finished. Read out ADC_0 and ADC_1 register to get the result (2Eh & 2Fh)

Table 83. RTC_Cntr Register

Name		Base		Default
RTC_Cntr		**2-wire serial**		**03h**
Offset: 28h		**RTC Control Register**		
		This register is reset at a RVDD-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Free_Bits<3:0>	0000	R/W	Free Bits to be used for application purpose
3:1	-	000	n/a	
0	OSC_ON	1	RW	RTC oscillator control, should be disabled. 0: Disable RTC oscillator **1: Enable RTC oscillator**

Table 84. ADC10_0 Register

Name		Base		Default
ADC10_0		**2-wire serial**		**0000 00xxb**
Offset: 2Eh		**First 10-bit ADC Register**		
		Writing to this register will start the measurement of the selected source. This register is reset at a AVDD27-POR, exception are bit 0 and 1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ADC10_MUX<3:0>	0000	R/W	Selects ADC input source **0000: BVDD** 0001: BVDDR 0010: CHGIN 0011: CHGOUT 0100: VBUS 0101: defined by DC_TEST in register 0x1C 0110: BATTEMP 0111: reserved 1000: MICS 1001: reserved 1010: I_MICS 1011: reserved 1100: VBE_1uA 1101: VBE_2uA 1110: I_CHGact 1101: I_CHGref
3:2	-	00	n/a	
1:0	ADC10<9:8>	xx	R	ADC result bit 9 to 8

Table 85. ADC10_1 Register

Name		Base		Default
ADC10_1		**2-wire serial**		**xxh**
Offset: 2Fh		**Second 10-bit ADC Register**		
		This register is reset at a AVDD27-POR.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ADC10<7:0>	00h	R	ADC results bits 7 to 0

Table 86. UID_0 to UID_7 Register

Name		Base		Default
UID_0 to UID7		**2-wire serial**		**n/a**
Offset: 38h to 3Fh		**UNIQUE ID Register**		
		This is a read only register and gets not reset.		
Adr.	**Byte Name**	**Default**	**Access**	**Bit Description**
38h	UID_0	n/a	R	Unique ID byte 0
39h	UID_1	n/a	R	Unique ID byte 1
3Ah	UID_2	n/a	R	Unique ID byte 2
3Bh	UID_3	n/a	R	Unique ID byte 3
3Ch	UID_4	n/a	R	Unique ID byte 4
3Dh	UID_5	n/a	R	Unique ID byte 5
3Eh	UID_6	n/a	R	Unique ID byte 6
3Fh	UID_7	n/a	R	Unique ID byte 7

12 Application Information

Figure 30. Typical Application Schematic

13 Package Drawings and Markings

Figure 31. MLF56 Marking

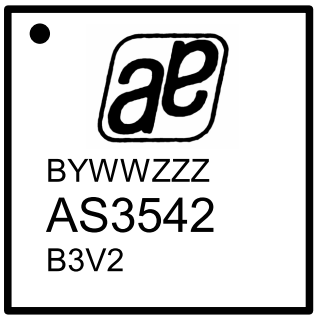
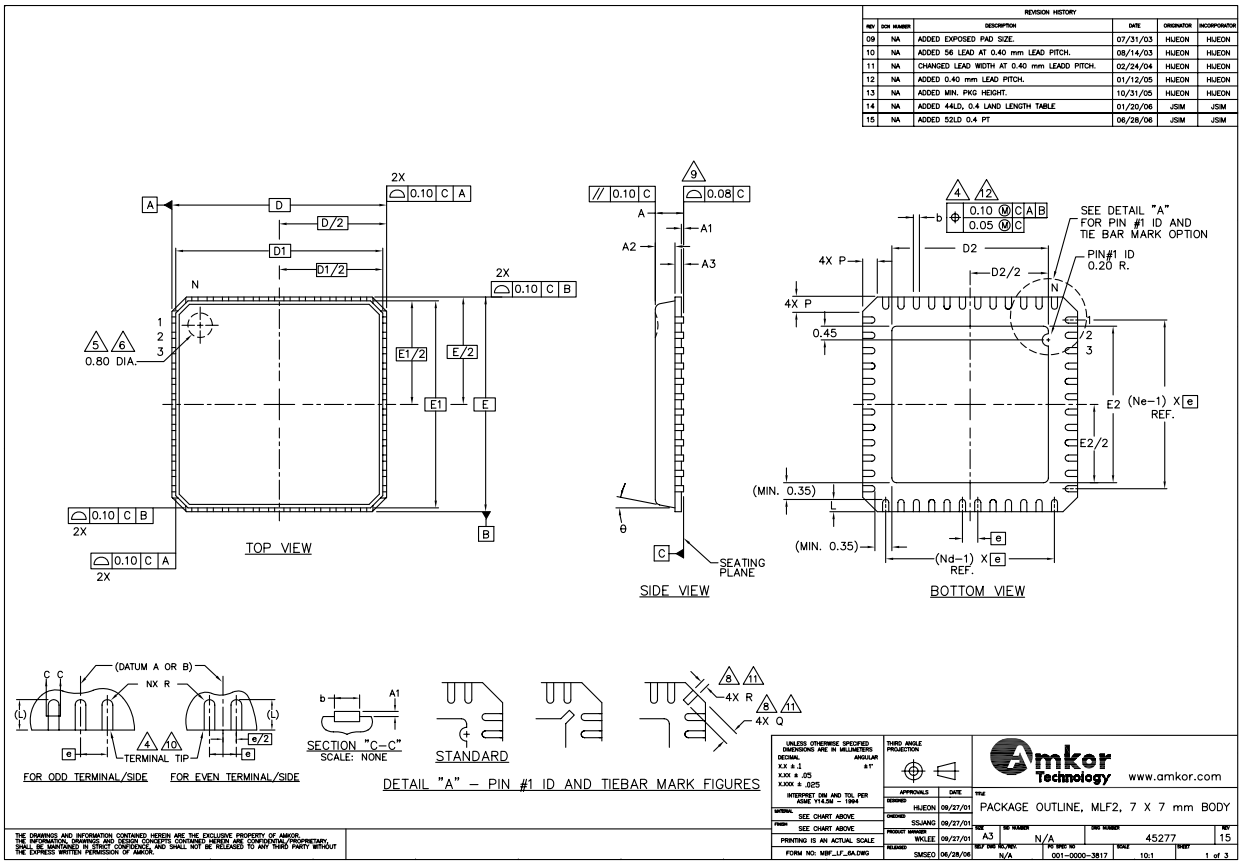


Table 87. Package Code AYWWZZZ

A	Y	WW	ZZZ
B ... for Green	year	working week assembly / packaging	free choice

Figure 32. MLF56 0.4mm pitch



SYMBOL	PITCH VARIATION E			NOTE
	MIN.	NOM.	MAX.	
e		0.40 BSC		
N		56		3
Nd		14		3
Ne		14		3
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	4,12
D2	4.80	4.90	5.00	
E2	4.80	4.90	5.00	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		7.00 BSC		
D1		6.75 BSC		
E		7.00 BSC		
E1		6.75 BSC		
θ	0	–	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.

14 Ordering Information

Table 88. Ordering Information

Model	Description	Delivery Form	Package
AS3542-EMFP	Ultra Low Power Stereo Audio Codec with System PMU	Tape & Reel dry pack	MLF2 56 [7.0x7.0x0.85mm] 0.4mm pitch

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