General Description

AS2702 (SAP4.1) is a new generation AS-Interface slave device, which supports AS-Interface bus systems with up to 62 slave modules.

Each slave module is equipped with an AS2702 device, which interfaces the module to the unshielded 2-wire AS-Interface bus for serial bidirectional data communication and power extraction.

Data communication over the AS-Interface takes place in master slave fashion, which foresees that all slave devices AS2702 connected to the bus are sequentially and cyclicly addressed by a single, central master unit. Data on the AS-Interface bus are Manchester encoded and can be found as sin2-pulses with a Vpp of between 3V and 8V on top of the bus' dc voltage of nominally 30V.

AS2702 regulates the nominal dc bus voltage of 30V internally down to 5V to supply it's internal circuitry including a 16 x 8 bits EEPROM, as well as down to a nominal supply level 24V with a max. loading of 35mA for the actuators and sensors connected to it at the field side.

Each slave device AS2702 may interface to up to 4 sensors or 3 actuators. An AS-Interface bus system based on AS2702 may hence link as many as 248 sensors and 186 actuators to a single master unit.

Slave device AS2702 (SAP4.1) is system compatible with predecessor device AS2701A (ISA3+):
slave modules equipped with AS2702 (SAP4.1) will run in existing AS-Interface bus systems based on AS2701A (ISA3+).

The AS-Interface concept is well established as a standardized digital bus system for industrial automation.

Key Features

- Interface device to connect actuators and sensors to an AS-Interface bus
- Flexible system solution offering 2 package options:
  SOIC 20 for full functionality;
  SOIC 16 for applications not requiring the parameter port
- DC power extraction from the AS-Interface bus
- Serial bidir. data communication with the bus
- Data communication watchdog
- 4-bit bidir. data port plus strobe to poll the sensors and control the actuators connected
- 4-bit parameter port plus strobe to provide settings to the sensors and actuators
- 24V power supply for the sensors and actuators
- Periphery fault input to signal hardware failure of the sensors and actuators
- Integrated 16 x 8 bit EEPROM to store (5 + 1)-bit slave address and settings
- 2 LED outputs to optically flag slave unit operation status
- Operating temperature Ta:
  - 25°C ... + 85°C
- Operating supply voltage/bus DC voltage:
  typ. 30V
- Operating current (Osc. on, outputs idle):
  ≤ 6mA
- Supply for sensors/actuators:
  typ. 24V, ≤ 35mA

Block Diagram

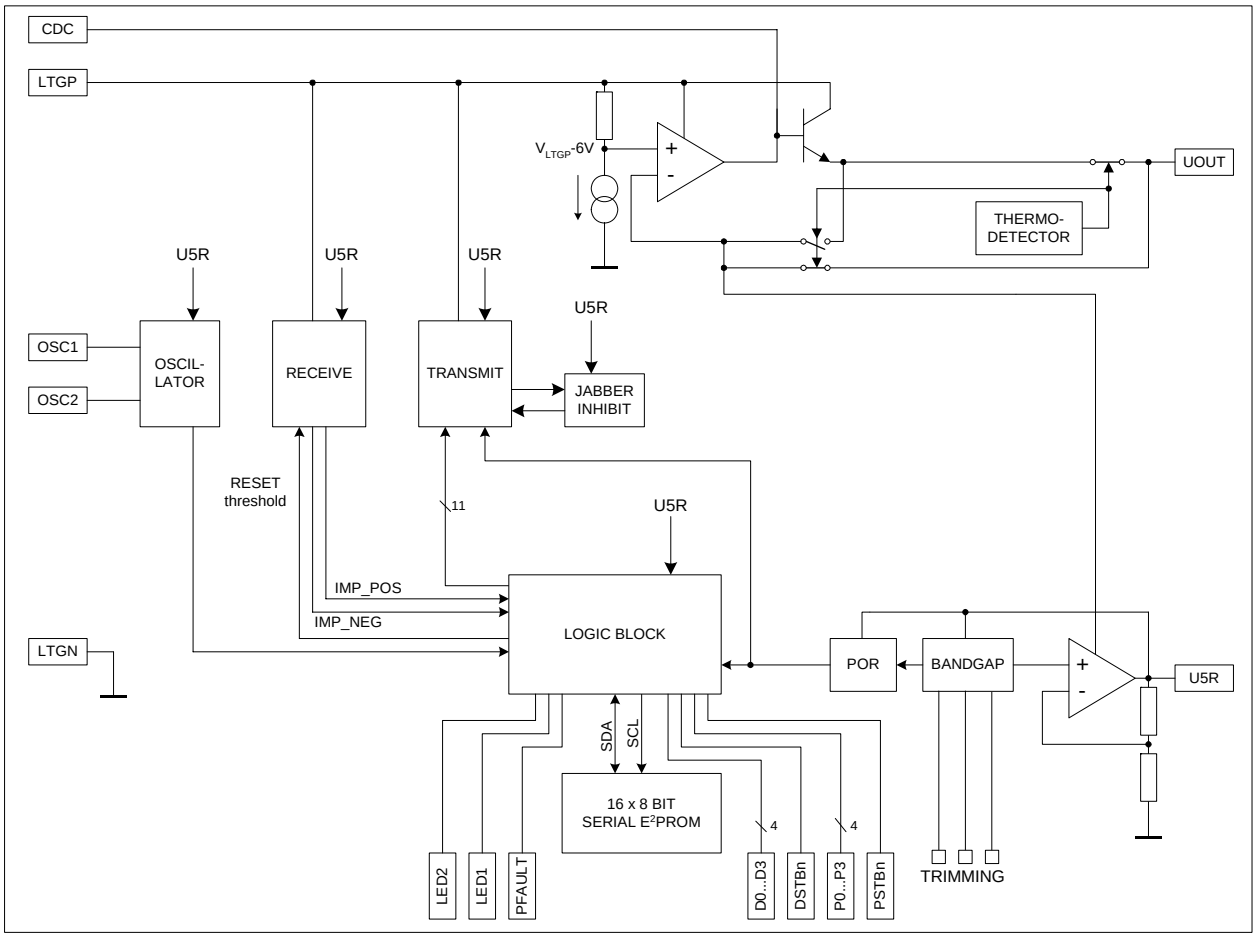

Figure 1 Block diagram

Pin Assignment and Description

SOIC 20 Pin No.	SOIC 16 Pin No.	Name	Type	Note	Description
1	-	P1	I/O, digital, pull-up	1, 2	Bidir. parameter port bit 1
2	-	P0	I/O, digital, pull-up	1, 2	Bidir. parameter port bit 0
3	1	D1	I/O, digital		Bidir. data port bit 1
4	2	D0	I/O, digital		Bidir. data port bit 0
5	3	DSTBn	I/O, digital, pull-up	1	Data port strobe output; reset-input
6	4	LED1	I/O, digital, pull-up	1	LED output 1 (IC test input)
7	5	OSC2	O, analog		Output to quartz crystal
8	6	OSC1	I, analog		Input from quartz crystal
9	7	U5R	O, power		Nom. 5V power supply output
10	8	LTGN	I, power		Neg. supply pin, connected to neg. AS-Interface bus line, ground reference
11	9	LTGP	I, power		Pos. supply pin, connected to pos. AS-Interface bus line
12	10	CDC	I/O, analog		Pin for ext. buffer capacitor
13	11	UOUT	O, power		Nom. 24V power supply output

SOIC 20	SOIC 16	Name	Type	Note	Description
14	12	PFAULT	I, digital, pull-up	1	Low-active input to flag failure of the sensors/actuators circuitry connected
15	13	LED2	I/O, digital, pull-up	1	LED output 2 (IC test input)
16	14	PSTBn	I/O, digital, pull-up	1	Parameter port strobe output (IC test input)
17	15	D3	I/O, digital		Bidir. data port bit 3
18	16	D2	I/O, digital		Bidir. data port bit 2
19	-	P3	I/O, digital, pull-up	1, 2	Bidir. parameter port bit 3
20	-	P2	I/O, digital, pull-up	1, 2	Bidir. parameter port bit 2

Notes:

1 The pull-up structure is a passive high-side current source with a nom. 10µA current.

2 The passive pull-up current source as per note 1 on these parameter port pins is off, if the slave device is programmed with I/O-configuration code 7 and a master data call is present.

Functional, Electrical and Timing Characteristics

All voltages are referenced to ground pin LTGN. Timing is valid for a quartz crystal frequency of 5.333MHz.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
VLTGP	Voltage at the positive supply pin	-0.3	40	V	1)
VCDC	Voltage at pin for ext. buffer capacitor	-0.3	VLTGP + 0.3V	V	
VU5R	Voltage at pins U5R, OSC1, OSC2	-0.3	7	V	
IIN	Input current at any pin, except for LTGP, CDC	-50	50	mA	2)
ESD1	Electrostatic discharge voltage	1500		V	3)
ESD2	Electrostatic discharge voltage	300		V	4)
Tstg	Storage temperature	-55	125	V	
Tbody	Soldering conditions		260	°C	5)
Ptot	Max. power dissipation		1	W	6)
RTHJA	Thermal resistance SOIC 16	61.2	74.8	°K/W	7)
RTHJA	Thermal resistance SOIC 20	58.5	71.5	°K/W	7)

Notes:

1) 50V during t > 50µs; repetition rate < 0.5Hz

2) Latch-up immunity test. Please observe max. power dissipation allowed

3) Human body model: R = 1.5kOhm; C = 100pF

4) Machine model; applies only for LTGP

5) The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C.

6) Free convection, see Figure 2

7) No forced cooling. PCB-surface: 21 cm^2; still air volume around the device. 10 cm^3

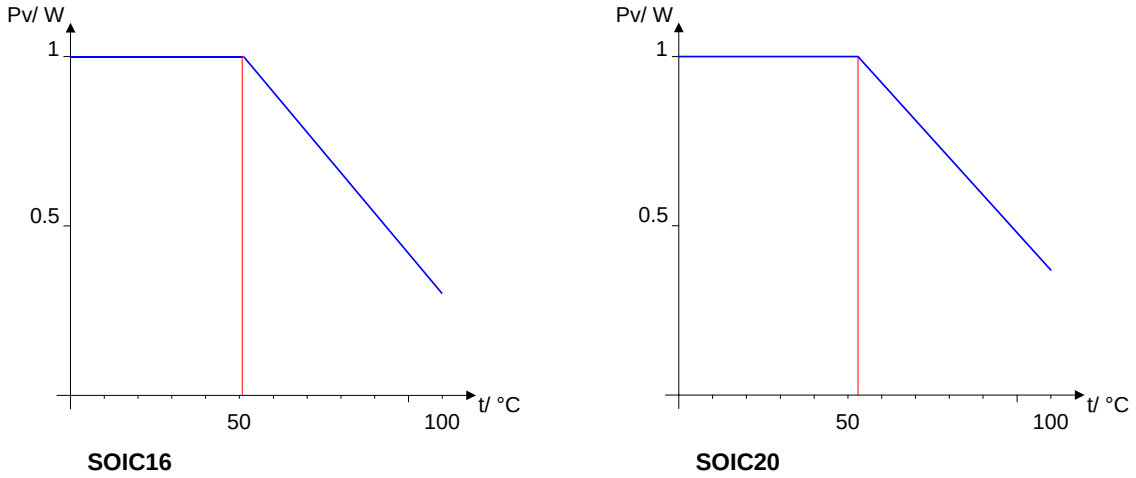

Figure 2 Max. acceptable power dissipation relative to ambient temperature

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit	Note
VLTGP	Positive supply voltage/dc portion	22.5		34	V	1
ILTG	Supply current consumption			6	mA	2
OA	Ambient temperature	- 25	25	85	°C	3
FC	Quartz frequency		5.333333		MHz	4
	Sensitivity against moisture					5

Notes:

1 False-poling protection diode to be inserted between pos. AS-Interface bus line and LTGP-pin. LTGP-pin to be protected furthermore with a voltage clamp between LTGP and LTGN.

2 Oscillator on; data transmission stage off; no loads connected

3 Power dissipation restrictions as per Figure 2 to be observed

4 AS-Interface Quartz

5 Level 5 acc. to JEDEC-standard JESD22-A112

Supply Pin LTGP

Positive supply pin connected to positive AS-Interface bus line and clamped relative to neg. supply pin/ground LTGN as described under Recommended Operating Conditions.

VLTGP and ILTG specified under Recommended Operating Conditions as well.

Symbol	Parameter	Min	Nom	Max	Unit	Note
VSIG	VPP of sin2-data-pulses on top of dc supply voltage	3		8	V	
Z	Input impedance between 50kHz and 300kHz			40	pF	CCDC = 100nF
		18			kOhm	
		50			mH	

Buffer Pin CDC

An external buffer capacitor with a recommended value of 100nF should be connected to this pin to ensure a sufficiently high input impedance Z at power supply pin LTGP.
Voltage at this pin can be as high as VLTGP.

Nom. 24V Power Supply Output UOUT

The supply output voltage at UOUT is directly derived from VLTGP and regulated to a level with an offset of about -6V relative to VLTGP.
UOUT provides bias to the sensors and actuators circuitry connected to the slave device as well as to the LEDs connected to outputs LED1 and LED2.

UOUT is equipped with a thermal overload protection, which foresees that VUOUT is switched off as soon as the slave device's substrate temperature TJ passes a threshold value in the range of (155 ±20)°C.
After TJ has come down and has passed a temperature threshold about (15 ±5)°C lower than (155 ±20)°C and after a consecutive minimum delay time of 1s has elapsed, VUOUT is switched on again.

Symbol	Parameter	Min	Max	Unit	Note
VUOUT	Power supply output voltage	VLTGP - 6.3V	VLTGP - 5.3V	V	
IUOUT	Load current		50	mA	1
VCOMOFF	UOUT voltage level	9.5	10.5	V	
	below which data transmission is inhibited				
CUOUT	Buffer capacitor	10		µF	2

Notes:
1 In case IUOUT >40mA and presence of sin2-data pulses on LTGP with VSIG >3V, VUOUT may drop as much as 1V below it's level in unloaded condition
2 Electrolytic and rf filter capacitor in parallel

Nom. 5V Power Supply Output U5R

The voltage at U5R is derived from the voltage present at UOUT, as long as UOUT is not switched off due to overload. In the latter case U5R is derived from an alternative voltage out of the UOUT voltage regulator, which is more or less similar to VUOUT in non switched off condition of UOUT. As a result VU5R is not affected by overload condition at UOUT and will remain.

Symbol	Parameter	Min	Max	Unit
VU5R	Power supply output voltage	4.85	5.15	V
IU5R	Load current		1	mA
CU5R	Buffer capacitor	470		nF

Oscillator Pins OSC1 and OSC2

The only component to be connected to these pins is a quartz crystal with a resonance frequency of 5.333333 MHz (AS-Interface quartz crystal).

Symbol	Parameter	Min	Max	Unit
CX2	Stray capacitance		10	pF

Data Port Pins D3, ..., D0 and Data Strobe Pin DSTBn

Basically data port D3, ..., D0 is designed for bidirectional data transfer out of and into the slave device. Each data port pin is equipped with both a low-side open-drain output stage as well as an input stage to this purpose.

Depending on the so-called IO-configuration code, written and stored in the slave device, each data port pin is individually set to behave as

- output, or
- output/input, or
- input.

The timing of the data transfer is presented in Figure 3.
Strobe signal DSTBn flags and governs the data transfer as follows:

a) data port pin is set 'output':
output data become valid upon the HL-edge of the strobe and will remain so until the next HL-edge, hence during the entire strobe cycle;

b) data port pin is set 'output/input':
output data become valid upon the HL-edge of the strobe and will remain so until it's LH-edge; input data to be valid within a specific time window relative to the HL-edge, after completion of the strobe's L-phase;

c) data port pin is set 'input':
input data to be valid within a specific time window relative to the HL-edge of the strobe, after completion of the strobe's L-phase.

If necessary, output data as per a) and b) can be easily latched with the LH-edge of strobe DSTBn as they will remain valid for about 0.4µs beyond as a minimum.
Care must be taken however, that signal delay added by external circuitry is lower for the strobe than for the data.

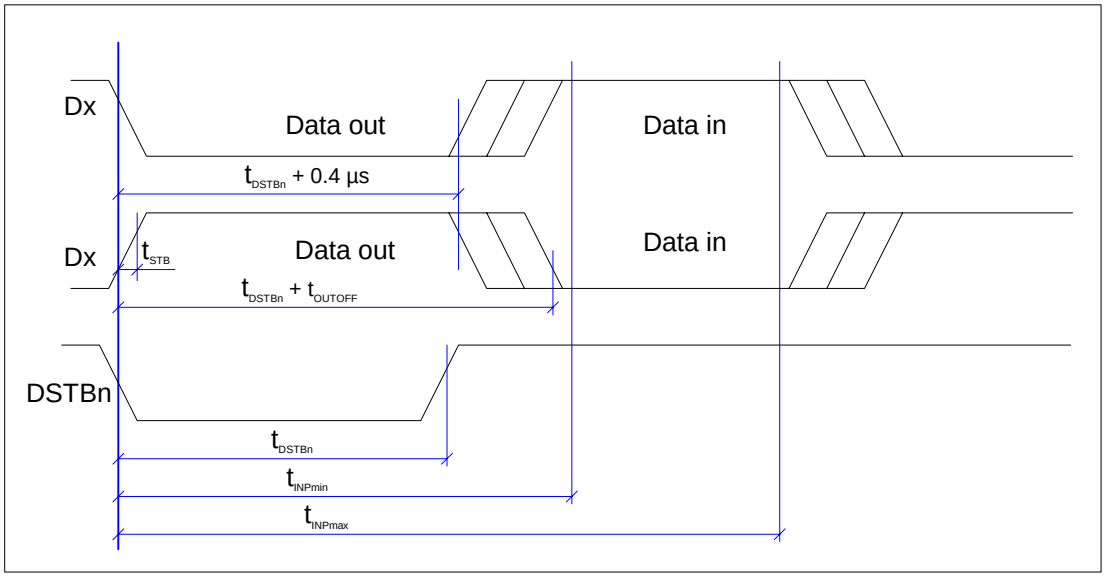

Figure 3 Timing of data transfer at data port D3, ..., D0 relative to strobe DSTBn

The following table specifies the timing parameters relating to Figure 3:

Symbol	Parameter	Min	Max	Unit	Note
tSTB	Delay DSTBn HL-edge to Dx output data valid		1.5	µs	
tDSTBn	DSTBn strobe width	6	6.8	µs	1
tOUTOFF	Delay DSTBn LH-edge to Dx output off	0.2	1	µs	2
tINP	Input data valid time window	10.5	12.5	µs	3

Notes:
1 Pulse width depends substantially on value of external pull-up resistor
2 Applies only to data port pins set to 'output/input' operation
3 Timing reference is DSTBn HL-edge.
Applies only to data port pins set to either 'output/input' or 'input' operation

The dc-parameters of the data port pins D3, ..., D0 are specified as follows:

Symbol	Parameter	Min	Max	Unit	Note
IOUTLO	Sink current @ output L	10		mA	VOUT = 1V
IOUTHI	Leakage current @ output off	-1	1	µA	1
VSCHLT	Input threshold voltage	2.5	3.5	V	2
VIN	Acceptable input voltage @ output off	-0.3	40	V	

Notes:
1 Output stage is low-side open-drain; ext. pull-up resistor required as no pull-up structure on chip
2 No hysteresis implemented

To govern the data transfer at data port D3, ...,D0 strobe pin DSTBn is equipped with a low-side open-drain output switch plus a passive high-side current source with a nom. 10µA pull-up current capability.
However a second function is assigned to the DSTBn pin which requires it to be input as well: if a low-pulse is imposed on DSTBn by external means with a pulse width of at least 50 to 100ms, the slave device will be put in RESET condition, as described in section “Reset”.

The dc-and timing parameters of strobe pin DSTBn are specified as follows:

Symbol	Parameter	Min	Max	Unit	Note
IOUTLO	Sink current @ output L	10		mA	VOUT = 1V
IOUTHI	Leakage current @ output off	-10	10	µA	VOUT = 5V
IINLO	Input current @ VIN = 1V	-5	-20	µA	1
VSCHLT	Input threshold voltage	1.5	3.5	V	2
VIN	Acceptable input voltage @ output off	-0.3	40	V	
tNORESET	DSTBn L-phase width, not triggering RESET		50	ms	
tRESET	DSTBn L-phase width, triggering RESET	100		ms	
CPINEXT	Max. stray capacity		20	pF	

Notes:
1 DSTBn is equipped with an on-chip pull-up current source, which ensures a sufficiently fast LH-edge upon output switch-off in open-pin condition, to prevent erroneous RESET triggering. If DSTBn has an external load connected to it, an additional external pull-up resistor may be needed to prevent erroneous RESET triggering upon output switch-off.
2 No hysteresis implemented

Parameter Port Pins P3, ..., P0 and Parameter Strobe Pin PSTBn

(Note that parameter port pins P3, ..., P0 are only available on AS2702 package option SOIC 20, not on the SOIC 16 option.)

The transfer of data at P3, ..., P0 and the supporting strobe action at pin PSTBn takes place similarly as at D3, ..., D0 resp. DSTBn.

Each parameter port pin P3, ..., P0 is equipped with both a low-side open-drain output switch plus a passive, but switchable high-side current source with a nom. 10 µA pull-up current capability, and with an input stage.

Though equipped for bidirectional data transfer as D3, ..., D0, the parameter port is nevertheless less flexible than the data port. Basically the parameter port is set to behave portwise as

- output, or
- input

depending on the IO-configuration code, written and stored in the slave device.

The timing of the data transfer is presented in Figure 4.
Strobe signal PSTBn flags and governs the data transfer as follows:

a) parameter port is set 'output':
output data become valid upon the HL-edge of the strobe and will remain so until the next HL-edge, hence during the entire strobe cycle;

b) parameter port is set 'input':
input data to be valid within a specific time window relative to the HL-edge of the strobe, after completion of the strobe's L-phase.

Output data as per a) could be easily latched with the LH-edge of strobe PSTBn, if at all necessary.

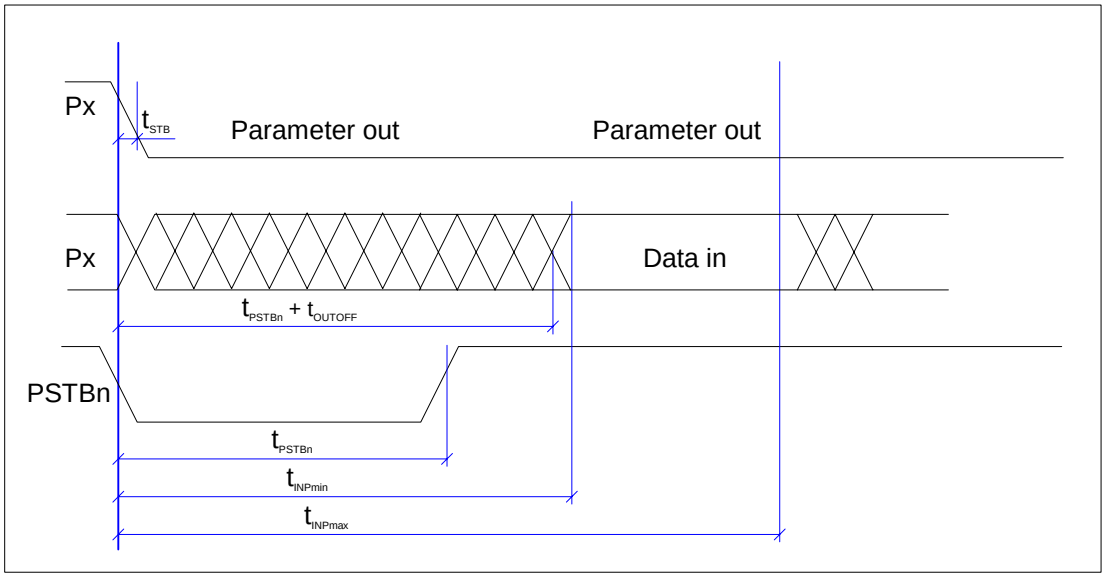

Figure 4 Timing of data transfer at parameter port P3, ..., P0 relative to strobe PSTBn

The following table specifies the timing parameters relating to Figure 4:

Symbol	Parameter	Min	Max	Unit	Note
tSTB	Delay PSTBn HL-edge to Px output data valid		1.5	µs	
tPSTBn	PSTBn strobe width	6	6.8	µs	1
tINP	Input data valid time window	10.5	12.5	µs	2

Notes:

1 Pulse width depends substantially on value of external pull-up resistor

2 Timing reference is PSTBn HL-edge.
Applies only to parameter port set to 'input' operation

The dc-parameters of the parameter port pins P3, ..., P0 are specified as follows:

Symbol	Parameter	Min	Max	Unit	Note
IOUTLO	Sink current @ output L	10		mA	VOUT = 1V
IOUTHI	Leakage current @ output off	-10	10	µA	VOUT = 5V
IOUTHI7	Leakage current @ output off; pull-up current source off	-1	1	µA	VOUT = 5V; IO-conf. = 7
IINLO	Input current @ VIN = 1V	-5	-20	µA	1

Symbol	Parameter	Min	Max	Unit	Note
VSCHLT	Input threshold voltage	2.5	3.5	V	2
VIN	Acceptable input voltage @ output off	-0.3	40	V	

Notes:
1 The passive high-side current-source provides an about constant input current @ 0V <= VIN <= 4V
2 No hysteresis implemented

Though equipped for bidirectional data transfer as D3, ..., D0, the parameter port is nevertheless less flexible than the data port. Note the following differences:
a) The parameter port is set portwise, the data port bitwise by the IO-configuration code;
b) The parameter port can only be set to either 'output' or 'input'. A bidirectional behaviour within a strobe cycle is not possible;
c) The parameter port is set to 'output' as a rule; the only exception occurs in case of IO-configuration 7 and a master data request, which set it to 'input'.

To govern the data transfer at the parameter port P3, ..., P0 strobe pin PSTBn is equipped with a low-side open-drain output switch plus a passive high-side current source with a nom. 10µA pull-up current capability. Typically the PSTBn-strobe width is about 6µs see Figure 4. (However to simplify and shorten the component test time of the slave device, the PSTBn pin is also used as an input. Input low pulses of more than 50µs each will step and cycle the device through 3 different test modes beyond the regular operation as described in this datasheet.)

The dc- and timing parameters of strobe pin PSTBn are specified as follows:

Symbol	Parameter	Min	Max	Unit	Note
IOUTLO	Sink current @ output L	10		mA	VOUT = 1V
IOUTHI	Leakage current @ output off	-10	10	µA	VOUT = 5V
IINLO	Input current @ VIN = 1V	-5	-20	µA	1
VSCHLT	Input threshold voltage	1.5	3.5	V	2
VIN	Acceptable input voltage @ output off	-0.3	40	V	
tNOTM	PSTBn L-phase width, not triggering test mode		35	µs	
tTM	PSTBn L-phase width, triggering test mode	50		µs	
CPINEXT	Stray capacitance		20	pF	

Notes:
1 PSTBn is equipped with an on-chip pull-up current source, which ensures a sufficiently fast LH-edge upon output switch-off in open-pin condition, to prevent erroneous test mode triggering.
If PSTBn has an external load connected to it, an additional external pull-up resistor may be needed to prevent erroneous test mode triggering upon output switch-off
2 No hysteresis implemented

Operation Status Pins LED1 and LED2

Pins LED1 and LED2 are both equipped with a low-side open-drain output switch plus a passive high-side current source with a nom. 10µA pull-up current capability. They will each have an LED load connected to UOUT, which will flag the operation status of the slave device, according to the following table:

Output LED1 (green LED connected)	Output LED2 (red LED connected)	Flagging Priority (1 = highest, ..., 4 = lowest)	Slave Device Operation Status	Reason
off	off		Supply voltage off	No supply voltage
on	off		Regular operation	
off	of	4	No data communication	Regular, non-zero slave address coded; data comm. watchdog triggered
blinks	on	3	No regular slave address coded	Slave address = default zero
blinks	blinks (alternating with LED1)	2	Hardware failure in sensor/actuator circuitry	Input PFAULT = L
off	blinks	1	External RESET or overload at UOUT pin	DSTBn = L to RESET, or UOUT switched-off due to overload

(LED1 and LED2 both also feature an input stage, to simplify component test and shorten test time of the slave device.)

The dc- and timing parameters of pins LED1 and LED2 are specified as follows:

Symbol	Parameter	Min	Max	Unit	Note
ILED	Sink current @ output L	10		mA	VOUT = 1V
IOUTHI	Leakage current @ output off	-10	10	µA	VOUT = 5V
VIN	Acceptable input voltage @ output off	-0.3	40	V	
fBLINK	Blinking frequency	2	3	Hz	

Data Communication Watchdog

AS2702 is equipped with a watchdog timer to supervise data communication by monitoring the strobe signals at pins DSTBn and PSTBn.
If a parameter or data strobe is not followed by a consecutive strobe within a time period of 50 ... 100ms, the watchdog is triggered and initiates a 'soft' reset, see section Reset.

Reset

There are 2 categories of reset-events, leading to 2 slightly different reset-conditions of the slave device:

1 A 'hard' reset taking place at power-up and power-down of supply-voltages U5R and UOUT.
At power-up the slave device leaves reset-condition as soon as U5R has passed 3.75V and UOUT has passed VCOMOFF = nom. 10V.
At power-down the slave device is forced into reset-condition as soon as U5R drops below 3.75V.
(Tolerance of the threshold voltages referred to is ±5 %)

2 A 'soft' reset, resulting from one of the following events:
- 2.1 Data strobe pin DSTBn is kept L for more than 100ms;
- 2.2 Master command 'RESET SLAVE' is received;
- 2.3 Master command 'RESET BROADCAST' is received;
- 2.4 The communication watchdog is triggered.

A ‘hard’ reset event conditions the slave device as follows:

- Internal states (counters, flags, ...) are reset
- The slave device’s receiver is desynchronized from the AS-Interface bus
- The low-side open-drain output stages at ports D3, ..., D0 and ports P3, ..., P0 are switched off
- Any test mode will be cancelled

A ‘soft’ reset has the following consequences:

- A regular, nominal 6µs L-phase strobe is generated on both the DSTBn and PSTBn pin
- The low-side open-drain output stages at ports D3, ..., D0 and ports P3, ..., P0 are switched off
- Internal states (counters, flags, ...) are rest, however the following states and operations are not affected:
  – the timer function which controls blinking of LED1 and LED2
  – the data communication
  – any test mode
  – any EEPROM write operation

Remark:
If UOUT drops below VCOMOFF = nom. 10V data communication with the AS-Interface bus is aborted by the receiver or transmitter of the slave device. As long as U5R does not drop below 3.75V in this situation, no ‘hard’ reset takes place; however the data communication watchdog will be triggered (unless disabled) and a ‘soft’ reset will result.

EEPROM

AS2702 has a 16 x 8 Bits serial interface EEPROM on board to store the slave unit’s address and set-up data in a non-volatile fashion.

The EEPROM stores the following data:

EEPROM-Address	Data	Relevant No. of Bits	Programmed by	Note
0, 1	Slave Address	5 + 1	Master (Initialization)	1
2	Settings (EID1)	4	Master (Initialization)	
3	Settings (IO-Conf.)	5	Slave unit manufacturer	
4	Settings (ID)	5	Slave unit manufacturer	
5	Settings (EID2)	5	Slave unit manufacturer	
6	Settings (Control-Code)	5	Slave unit manufacturer	

Note:
1 6 Bits (A4, ..., A0 + Sel-bit) in extended address mode: 62 slaves addressable;
5 Bits (A4, ..., A0) in non-extended address mode: 31 slaves addressable

Obviously the capacity of the EEPROM is only partially used.

Reading and writing of the EEPROM is performed bytewise and trough temporary, volatile registers.
Writing of data from the volatile register into the EEPROM takes about 10ms per byte, whereas reading takes less than 1ms per byte.

Upon RESET the EEPROM info is read into temporary register, including the slave’s address which has been written redundantly into EEPROM locations 0 and 1 before.
The temporary registers receiving the address are compared for similarity; in case of non-similarity – which e.g. may have been caused by a supply voltage dip during address writing – the slave will flag non-regular operation status/slave address zero.

AS-Interface Bus Communication

All slaves connected to an AS-Interface bus are sequentially and cyclicly called by the master in a string of individual transactions between the master and each slave unit.
A transaction consists of a 14 bits master request, typically containing the slave's address as well as data or parameter info, and an immediate acknowledging slave response of 7 bits.

The 14 bits master request – apart from Start Bit ST = 0 and End Bit EB = 1 – has the following contents:

- 1 Control Bit CB: CB = 0 stands for data transfer (typ. data or parameters)
  CB = 1 identifies command-type requests
- 5 Address Bits: A4, ..., A0
- 5 Information Bits: I4, ..., I0 (typ. data or parameters)
- 1 Parity Bit PB

AS2702 allows for up to 62 slaves on the same AS-Interface bus; this requires a slave address extended to 6 bits, hence an extra bit beyond A4, ..., A0.
Information bit I3 is used as the 6th address bit in this so-called extended address mode. It is called Sel-bit, as it is perceived as to select between A-slave (Sel = 0) and B-slave (Sel = 1) at address location A4, ..., A0.
In non-extended address mode AS2702 is addressed with A4, ..., A0 only – for a max. total of 31 slaves per AS-Interface bus system, and is system compatible with existing slave device AS2701A.

The 7 bits slave response – apart from Start Bit ST = 0 and End Bit EB = 1 – has the following contents:

- 4 Information Bits: I4, ..., I0 (typ. data or parameters)
- 1 Parity Bit PB

Application Support

For general information and documentation on the AS-Interface concept you may contact the AS-Interface Association:

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D-63571 Gelnhausen
Tel.: +49-6051-473212
Fax: +49-6051-473282
e-mail: info@as-interface.net
http://www.as-interface.net

Ordering Information

AS2702-20T	Package:	SOIC 20; delivery: tape & reel
AS2702-16T	Package:	SOIC 16W; delivery: tape & reel; no parameter port available
AS2702-20	Package:	SOIC 20; delivery: tubes
AS2702-16	Package:	SOIC 16W; delivery: tubes; no parameter port available

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