AS1801

Ultra-Low Power, I²C Serial Real-Time Clock with Trickle Charger

1 General Description

The AS1801 serial real-time clock is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I²C bus.

The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM / PM indicator.

The AS1801 provides a clean clock/calendar start function by clearing the 'wait_for_start' flag in the control register. The flag is set whenever a clock/calendar setting takes place and the counter operation is stopped until restarted by clearing the flag.

In addition to the basic timekeeping functions the device offers dual power pins for primary and backup power supplies as well as a trickle charger at pin VBAT for the backup battery.

The AS1801 provides two modes of frequency trimming for the external quartz crystal in steps of 3.81 ppm within an 8-second interval and in steps 5.8 ppm within a 2-day period. None, one or both methods can be used simultaneously.

A backup counter counts the seconds during read access to the clock/calendar registers and adds them after the end of the access hence, making sure that date and time stay correct even if the access takes longer than one second.

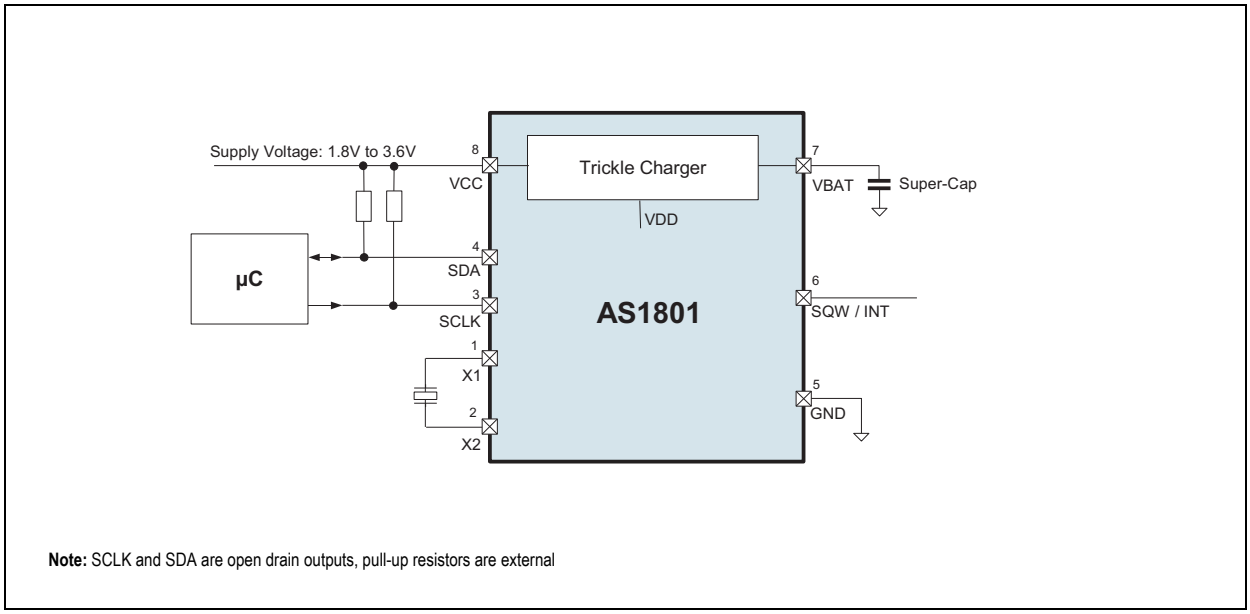
2 Key Features

- Real-Time Clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- 24-hour / 12-hour format with AM / PM indicator
- Trickle-Charger
- I²C Serial Interface
- Two Time-of-Day alarms
- Oscillator Frequency Trimming (every 8 seconds, every 2 days)
- Oscillator Stop Flag (deep power down detection)
- Wait-for-Start Flag for clean clock start
- Back-up counter allows long access times (>1s) of the serial interfaces
- Programmable Square-Wave Output - Defaults to 1Hz on Power-up
- Available in 8-pin TDFN (2x2mm)
- -40ºC to +85ºC Operating temperature range

3 Applications

The device is ideal for handhelds like GPS, POS Terminal, Consumer Electronics like Set-Top Box, VCR/Digital Recording; Office Equipment such as Fax/Printer, Copier; Medical implements such as Glucometer, Medicine Dispenser; Telecommunications like Router, Switch, Server; and many other applications like Utility Meters, Vending Machines, Thermostats and Modems.

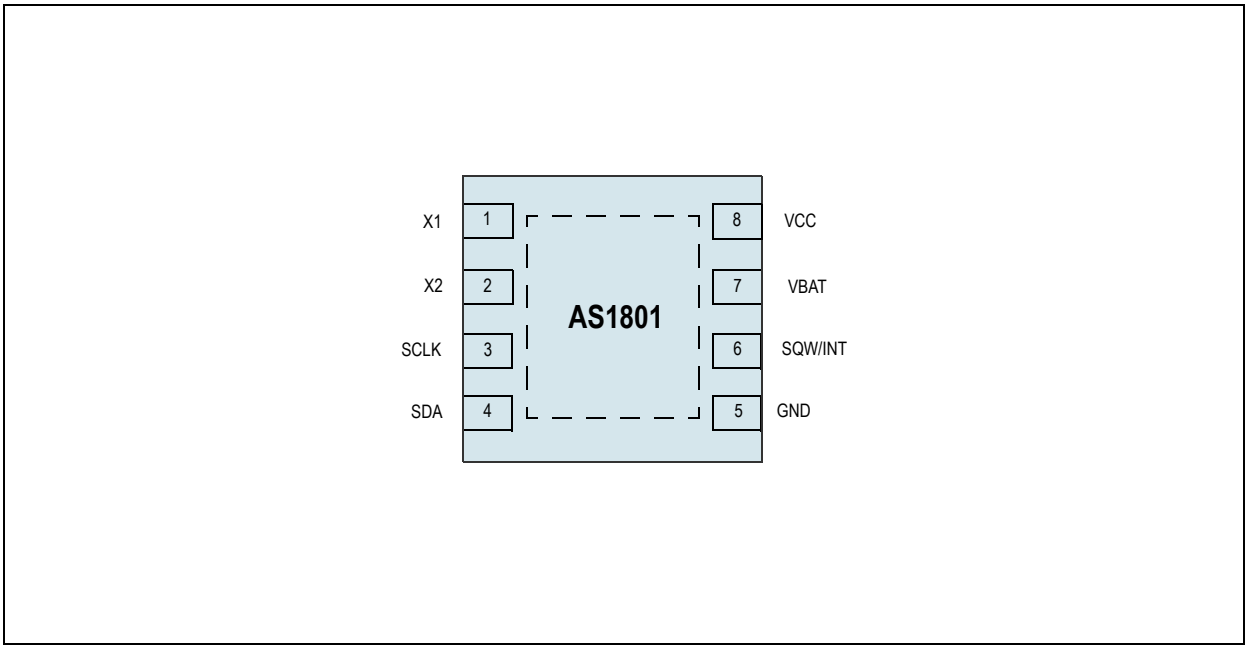
Figure 1. AS1801 - Typical Application Diagram



Note: SCLK and SDA are open drain outputs, pull-up resistors are external

4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Description

Table 1. Pin Description

Pin Name	Pin Number	Description
X1	1	**Connections for a Standard 32.768kHz Quartz Crystal.** The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6pF. An external 32.768kHz oscillator can also drive the AS1801. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
X2	2	
GND	5	**Ground.** DC power is provided to the device on this pin.
SCLK	3	**Serial Clock Input.** Open Drain Input. SCLK is used to synchronize data movement on the I²C interface.
SDA	4	**Serial Data Input/Output.** Open drain digital I/O I²C data pin.
SQW/INT	6	**Square-Wave/Interrupt Output.** Programmable Square-wave or Interrupt CMOS output signal. If the oscillator is running, SQW is running with 1Hz per default. bit INTCN=0: SQW output bit INTCN=1: INT output
VBAT	7	**Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup.** In systems using the trickle charger, the rechargeable energy source is connected to this pin.
VCC	8	**Supply Voltage.** DC power is provided to the device on this pin. If $V_{CC} > V_{BAT}$: VCC is used to power the device. If $V_{CC} < V_{BAT}$: VBAT is used to power the device.
	Exposed Pad	**Not Connected.** This pin is not connected may be left floating.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VCC, VBAT to GND	-0.3	5	V	
θJA Thermal Impedance		79	ºC/W	
Temperature Ranges and Storage Conditions				
Junction Temperature		+125	ºC	
Storage Temperature Range	-55	+125	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a maximum floor life time of unlimited

6 Electrical Characteristics

6.1 DC Electrical Characteristics

V_{CC} = 1.8V to 3.6V, typ. values @ V_{CC} = 1.8V, T_{AMB} = +25ºC (unless otherwise specified); All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{AMB}	Operating Temperature Range		-40		85	°C
T_J	Operating Junction Temperature		-40		+125	°C
I_{LI}	Input Leakage	SCLK only	-1		+1	µA
I_{LO}	I/O Leakage	SDA	-1		+1	µA
V_{OL}	Logic 0 Output (I_{OL} = 3mA)	SDA, SQW/INT			0.4	V
V_{OH}	Logic 1 Output (I_{OH} = -3mA)	SQW/INT only	V_{DD}-0.4V			V
I_{CCA}	Active Supply Current	I_{CCA} - SCLK clocking at maximum frequency = 400kHz, V_{IL} = 0.0V, V_{IH} = V_{CC}, t_R = t_f = 20ns		35		µA
I_{CCS}	Standby Current	Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, SQW is enabled		3		µA
V_{CC}	Supply Voltage	Full operation	1.8		3.6	V
V_{BAT}		Timekeeping	0.9		3.6	
V_{IH}	Logic 1	SCLK, SDA	0.7 x V_{CC}		V_{CC} + 0.3	V
V_{IL}	Logic 0	SCLK, SDA	-0.3		+0.3 x V_{CC}	V
I_{CCTOSC}	Timekeeping Current (Oscillator Enabled)[1]	V_{BAT} = 1.5V, T_{AMB} = 25°C		400	500	nA
Trickle-Charge						
R1	Trickle -Charge Resistors			2		kΩ
R2				3		
R3				4		
R4				8		
	Loading Current	V_{CC} = 3.6V, V_{BAT} =0V, @ R1 and Diode = 0			2	mA
V_{TD}	Trickle-Charge Diode Voltage Drop[2]			0.7		V

1. Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}. Specified with the SQW function disabled by setting INTCN = 1. Using recommended crystal on X1 and X2.
2. Through the Trickle-Charge Register no or up to 3 diodes can be placed in series (see Trickle-Charge Register on page 11).

6.2 AC Electrical Characteristics

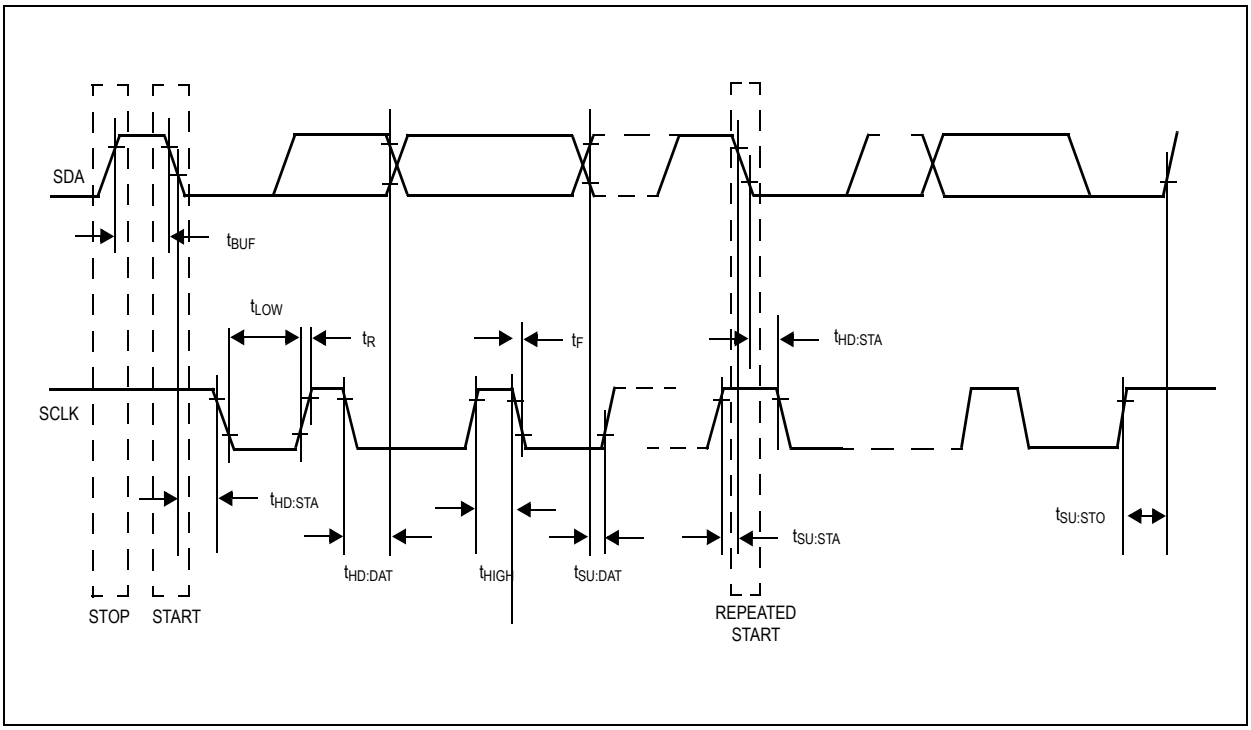
VCC = 1.8V to 3.6V, T_A = -40ºC to +85ºC, typical values @ TAMB = +25ºC (unless otherwise specified)

Table 4. AC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCLK}	SCLK Clock Frequency	Fast mode	100		400	kHz
		Standard mode	0		100	
f_{OSC}	Oscillator Frequency	External quartz crystal (see Oscillator Circuit on page 8)		32.768		kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Fast mode	1.3			µs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition[1]	Fast mode	0.6			µs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCLK Clock	Fast mode	1.3			µs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCLK Clock	Fast mode	0.6			µs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for a Repeated START Condition	Fast mode	0.6			µs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time[2]	Fast mode	0		0.9	µs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time[3]	Fast mode	100			µs
		Standard mode	250			
t_R	Rise Time of both SDA and SCLK signals	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		1000	
t_F	Fall Time of both SDA and SCLK signals	Fast mode	$20 + 0.1C_B$		300	ns
		Standard mode	$20 + 0.1C_B$		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			µs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line	Total capacitance of one bus line			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCLK)				10	pF

1. After this period, the first clock pulse is generated.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.
3. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCLK line is released.

Figure 3. I²C Timing Diagram



7 Typical Operating Characteristics

V_{CC} = 3.3V; T_A = +25ºC, (unless otherwise specified).

Figure 4. Timekeeping Current vs. Battery Voltage

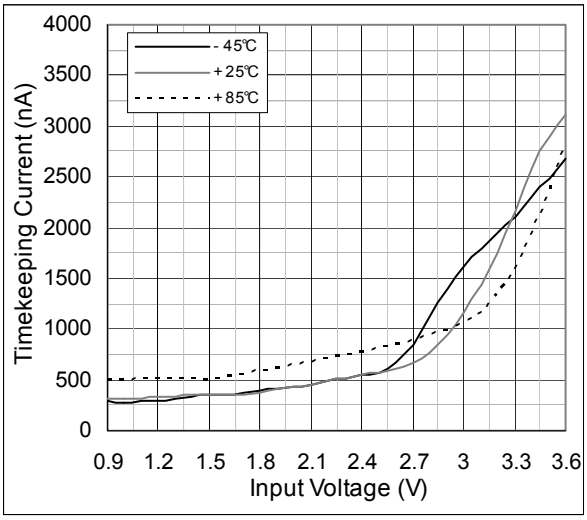
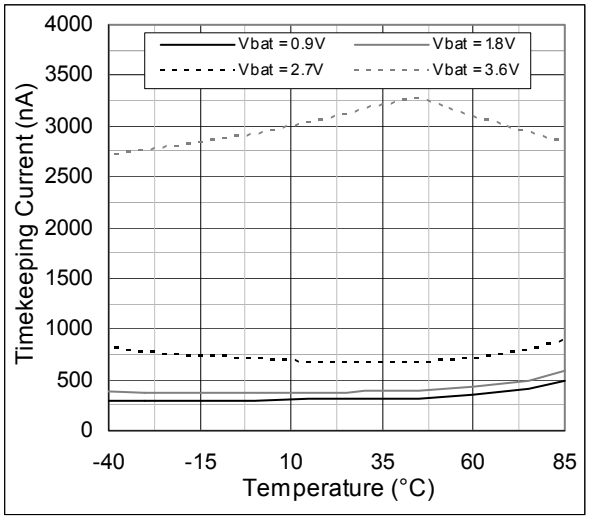


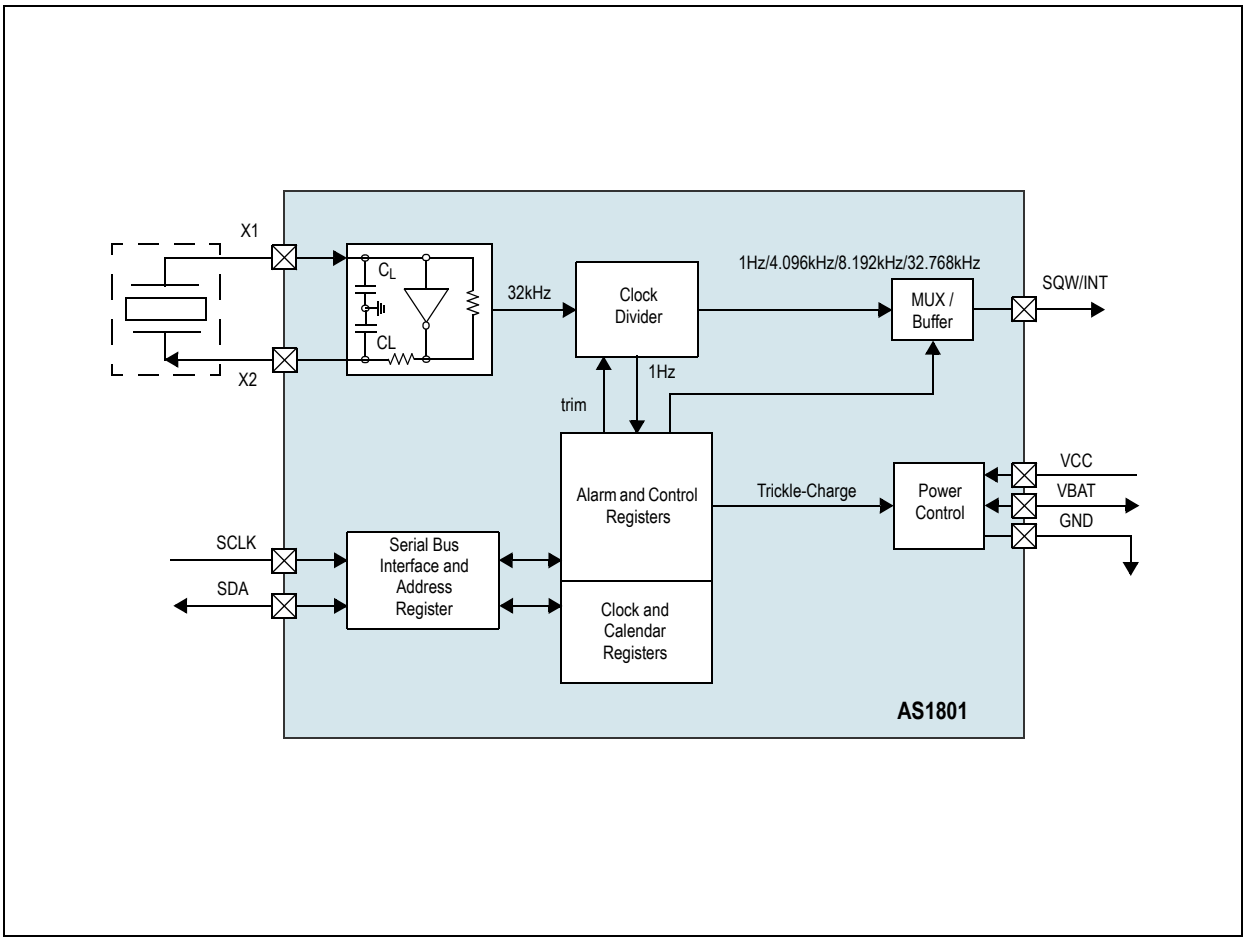
Figure 5. Timekeeping Current vs. Temperature



8 Detailed Description

The Block Diagram shows the main elements of the AS1801. As shown, communications to and from the AS1801 occur serially over an I²C bus. The AS1801 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I²C interface whenever VCC is between 3.6V and 1.8V. I²C operation is not guaranteed when VCC is below 1.8V. The AS1801 maintains the time and date when VCC is as low as 0.9V.

Figure 6. AS1801 - Block Diagram



8.1 Oscillator Circuit

The AS1801 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 5 specifies several crystal parameters for the external crystal. The Block diagram shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 5. Crystal Specifications[1]

Symbol	Parameter	Min	Typ	Max	Units
f_o	Nominal Frequency		32.768		kHz
ESR	Series Resistance			50	kΩ
C_L	Load Capacitance		6		pF

1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

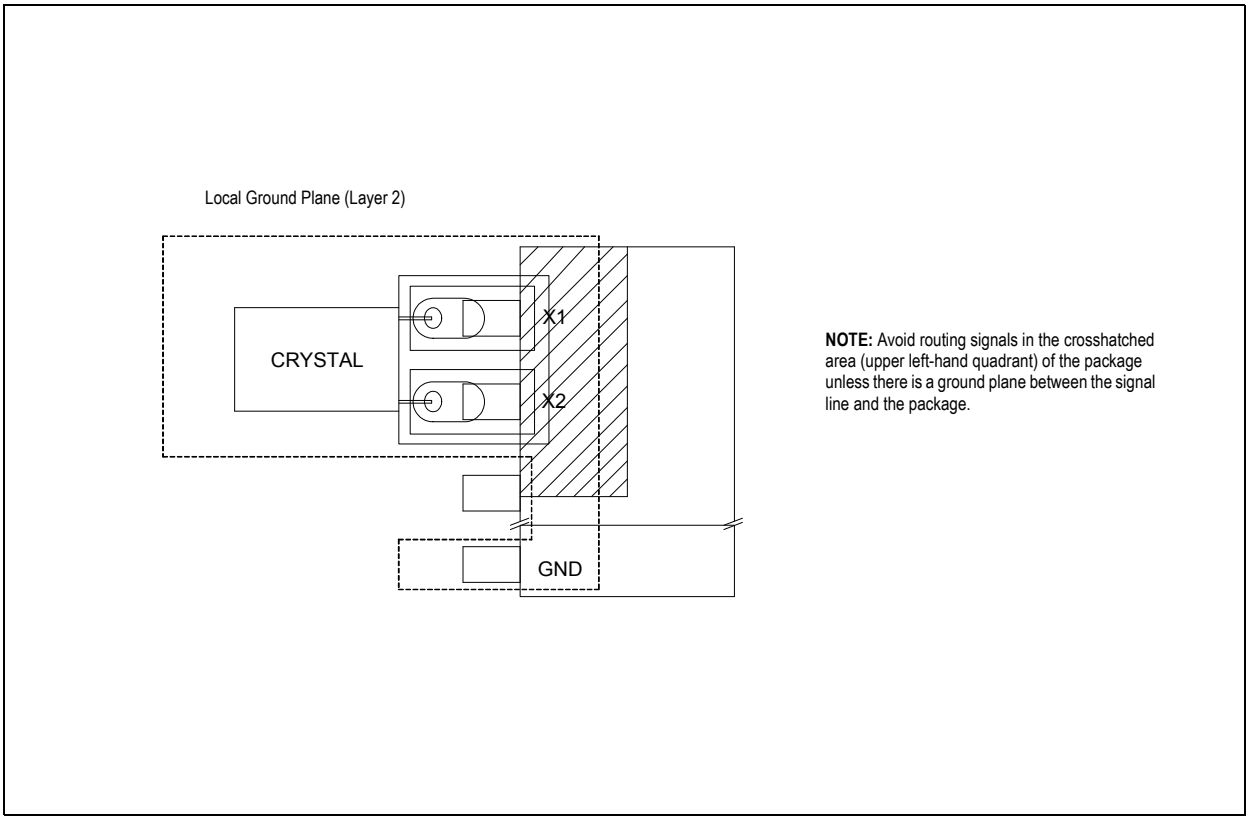
8.2 VCC to VBAT Changeover

The internal power supply changeover between VCC and VBAT is controlled by a comparator and low loss power switch. The reference point for the comparator is the voltage on VBAT. If VCC > VBAT, VCC is connected directly to the internal supply rails of the AS1801, and VBAT is disconnected from the internal supply. When VCC < VBAT, the VCC pin is disconnected from the internal supply, and VBAT is connected instead. The built-in hysteresis ensures clean switching and no reverse current flow.

8.3 Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 7 shows a typical PC board layout for isolating the crystal and oscillator from noise.

Figure 7. Typical PC Board Layout for Crystal



8.4 Address Map

Table 6 shows the address map for the AS1801 registers. During a multibyte access, when the address pointer reaches the end of the register space (1Fh) it wraps around to location 00h. On an I²C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 6. Timekeeper Registers

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range	
00H	0	10 Seconds			Seconds				Seconds	00-59	Calendar
01H	0	10 Minutes			Minutes				Minutes	00-59	
02H	0	12/24	AM/PM 10 Hour	10 Hour	Hour				Hours	1-12 +AM/PM 00-23	
03H	0	0	0	0	0	Day			Day	0-6	
04H	0	0	10 Date		Date				Date	01-31	
05H	Century	0	0	10 Month	Month				Month/Century	01-12 + Century	
06H	10 Year				Year				Year	00-99	
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59	Alarm & Control
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59	
09H	A1M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1-12 + AM/PM 00-23	
0AH	A1M4	DY/DT	10 Date		Day				Alarm 1 Day	1-7	
					Date				Alarm 1 Date	1-31	
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59	
0CH	A2M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1-12 + AM/PM 00-23	
0DH	A2M4	DY/DT	10 Date		Day				Alarm 2 Day	1-7	
					Date				Alarm 2 Date	1-31	
0EH	FREE[1]	0	WAITF	RS2	RS1	INTCN	A2IE	A1IE	Control	--	
0FH	OSF	0	0	0	0	TSA	A2F	A1F	Status	--	
10H	TRIM VALUE 1								Freq. Trimming (2 days)		
11H	0	0	0	TCS	DS1	DS0	ROUT1	ROUT0	Trickle Charger		
12H	TRIM VALUE 2								Freq. Trimming (8 seconds)		
13H	0	0	0	0	0	0	T1	T0	Test		res.[2]
14H	TESTMODES								Testmodes		

1. Free Bit for the user.
2. Don't touch. Reserved for Test & Evaluation.

8.5 Trickle-Charge Register

This register controls the trickle-charge characteristics of the AS1801. The simplified schematic of Figure 8 shows the basic components of the trickle charger. The trickle-charge register (bits 0 to 4) controls the selection of the trickle charger.

Table 7. Trickle-Charge Register (11h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	TCS	DS1	DS0	ROUT1	ROUT0

The AS1801 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 and 3) select whether no diode (ideal), one, two or three diodes are connected between VCC and VBAT. The ROUT bits (bits 0 and 1) select the resistor value that is connected between VCC and VBAT. The selectable resistor values are shown in Table 8. The TCS bit (bit 4) enables the trickle charger function.

Table 8. Trickle-Charge - ROUT values

ROUT Bits [1:0]	Resistor	Typical Value
00	R1	8kΩ
01	R2	4kΩ
10	R3	3kΩ
11	R4	2kΩ

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging.

Table 9. Trickle-Charge Register - Details

TCS bit [4]	DS bits [3:2]	Number of Diodes	Notes
0	-	-	Output OFF
1	00	0	Ideal diode
1	01	1	
1	10	2	
1	11	3	

The maximum charging current can be calculated as illustrated in the following example.

Assume that a system power supply of 3.6V is applied to VCC and a super cap is connected to VBAT. Also assume that the trickle charger has been enabled with no diode and resistor R4 between VCC and VBAT. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = \frac{3.6V - diodedrop}{R4} = \frac{3.6V - 0V}{2k\Omega} = 1.8mA \qquad \text{(EQ 1)}$$

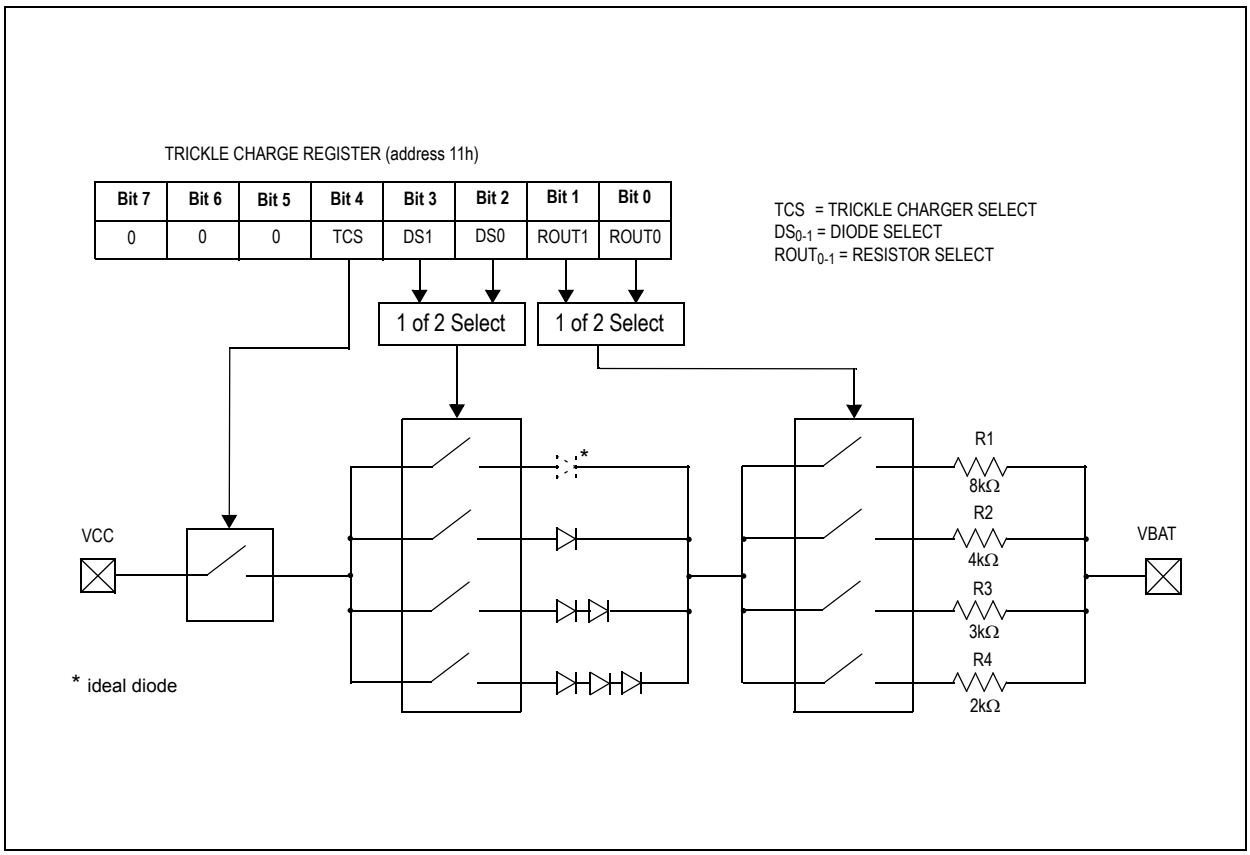
Where: TCS = '1', DSx = '00', RSx = '11'

As the super cap charges, the voltage drop between VCC and VBAT decreases and therefore the charge current decreases.

To prevent uncontrolled switching between VCC and VBAT a hysteresis of 20mV is implemented. So a 20mV difference is necessary before the change from VCC to VBAT and vice versa.

Note: If a lithium battery is used for backup, the trickle charger needs to be disabled.

Figure 8. Programmable Trickle Charger



8.6 Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Table 6 on page 10. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

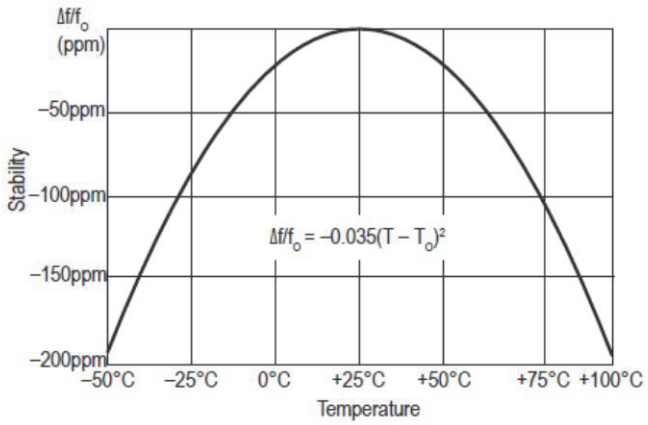
The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The AS1801 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). All hours values, including the alarms, must be re initialized whenever the 12/24-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99-00.

8.7 Frequency Adjustment

A calibrated oscillator (e.g. locked to an atomic standard) should be used to provide a reference against which production units are trimmed. Apart from the initial tolerance, the crystals vary with temperature and ageing. The temperature characteristic of the crystal 1MHz is a parabolic shape with a design turnover of 25ºC (see Figure 9).

Figure 9. Typical Frequency Stability Characteristic



As an example a given crystal has a basic untrimmed frequency of ±20ppm at 25ºC, with drift over temperature around ±100ppm. Ageing is 3ppm / year. Hence to obtain <20ppm overall production specification, the inverse of the drift with temperature is loaded into the two trim registers (see Table 10, Table 11) from the I²C interface. If the trim registers are not used, then the basic crystal drift sets the overall performance (e.g. ± 20ppm @ 25ºC).

8.8 Frequency Trimming (2 Day) Register 10H

The register controls the frequency trimming over a 2 day period. The trim correction is defined by Bits 0-4. The remainder are “don’t care” and are read as 000.

Table 10. 2-Day Interval Frequency Trimming (10H)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Trim 4	Trim 3	Trim 2	Trim 1	Trim 0

The table specifies two successive days with a (possibly) different number of seconds that have to be added or subtracted per day. The sequence “day1/day2” is repeated continuously.

Table 11. 2-Day Interval Frequency Trimming Register Details

Frequency Trim					Correction ppm	Seconds per Day 1	Seconds per Day 2
0	1	1	1	1	87.0	7	8
0	1	1	1	0	81.2	7	7
0	1	1	0	1	75.4	6	7
0	1	1	0	0	69.6	6	6
0	1	0	1	1	63.8	5	6
0	1	0	1	0	58.0	5	5
0	1	0	0	1	52.2	4	5
0	1	0	0	0	46.4	4	4

Table 11. 2-Day Interval Frequency Trimming Register Details

Frequency Trim					Correction ppm	Seconds per Day 1	Seconds per Day 2
0	0	1	1	1	40.6	3	4
0	0	1	1	0	34.8	3	3
0	0	1	0	1	29.0	2	3
0	0	1	0	0	23.2	2	2
0	0	0	1	1	17.4	1	2
0	0	0	1	0	11.6	1	1
0	0	0	0	1	5.8	0	1
0	0	0	0	0	0	0	0
1	1	1	1	1	-5.8	0	-1
1	1	1	1	0	-11.6	-1	-1
1	1	1	0	1	-17.4	-1	-2
1	1	1	0	0	-23.2	-2	-2
1	1	0	1	1	-29.0	-2	-3
1	1	0	1	0	-34.8	-3	-3
1	1	0	0	1	-40.6	-3	-4
1	1	0	0	0	-46.4	-4	-4
1	0	1	1	1	-52.2	-4	-5
1	0	1	1	0	-58.0	-5	-5
1	0	1	0	1	-63.8	-5	-6
1	0	1	0	0	-69.6	-6	-6
1	0	0	1	1	-75.4	-6	-7
1	0	0	1	0	-81.2	-7	-7
1	0	0	0	1	-87.0	-7	-8
1	0	0	0	0	-92.8	-8	-8

The RTC is always adjusted at the same time: **00:00 a.m. and 30 seconds**. (The 30 seconds is required to avoid conflicts with alarm settings which are defined to happen at 0 seconds.) Subtraction means that the specified number of 1 Hz pulses is ignored. This has the effect that the clock just stands still for the specified number of seconds.

Example: A crystal has a frequency that is 30ppm higher than specified. Therefore the RTC will run faster. Thus, the RTC has to correct in the negative direction, it must subtract seconds. Value '11011' (-29.0) will be chosen which means that on the first day (day1), 2 seconds are subtracted, then on the next day (day2), 3 seconds are subtracted, then 2 again and so on.

8.9 Frequency Trimming (Seconds) Register 12H

The register controls the frequency trimming over an 8 second interval using a sigma-delta technique.

Table 12. 8-Seconds Interval Frequency Trimming (12H)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ftrim sec 7	ftrim sec 6	ftrim sec 5	ftrim sec 4	ftrim sec 3	ftrim sec 2	ftrim sec 1	ftrim sec 0

The trim correction is defined by Bits 0-7.

Table 13. 8-Seconds Interval Frequency Trimming (12H)

step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm	step dec	code hex	F_corr ppm
-128	80	-488.28	-96	A0	-366.21	-64	C0	-244.14	-32	E0	-122.07	0	00	0.00	32	20	122.07	64	40	244.14	96	60	366.21
-127	81	-484.47	-95	A1	-362.40	-63	C1	-240.33	-31	E1	-118.26	1	01	3.81	33	21	125.89	65	41	247.96	97	61	370.03
-126	82	-480.65	-94	A2	-358.58	-62	C2	-236.51	-30	E2	-114.44	2	02	7.63	34	22	129.70	66	42	251.77	98	62	373.84
-125	83	-476.84	-93	A3	-354.77	-61	C3	-232.7	-29	E3	-110.63	3	03	11.44	35	23	133.51	67	43	255.58	99	63	377.66
-124	84	-473.02	-92	A4	-350.95	-60	C4	-228.88	-28	E4	-106.81	4	04	15.26	36	24	137.33	68	44	259.40	100	64	381.47
-123	85	-469.21	-91	A5	-347.14	-59	C5	-225.07	-27	E5	-103	5	05	19.07	37	25	141.14	69	45	263.21	101	65	385.28
-122	86	-465.39	-90	A6	-343.32	-58	C6	-221.25	-26	E6	-99.18	6	06	22.89	38	26	144.96	70	46	267.03	102	66	389.10
-121	87	-461.58	-89	A7	-339.51	-57	C7	-217.44	-25	E7	-95.37	7	07	26.70	39	27	148.77	71	47	270.84	103	67	392.91
-120	88	-457.76	-88	A8	-335.69	-56	C8	-213.62	-24	E8	-91.55	8	08	30.52	40	28	152.59	72	48	274.66	104	68	396.73
-119	89	-453.95	-87	A9	-331.88	-55	C9	-209.81	-23	E9	-87.74	9	09	34.33	41	29	156.40	73	49	278.47	105	69	400.54
-118	8A	-450.13	-86	AA	-328.06	-54	CA	-205.99	-22	EA	-83.92	10	0A	38.15	42	2A	160.22	74	4A	282.29	106	6A	404.36
-117	8B	-446.32	-85	AB	-324.25	-53	CB	-202.18	-21	EB	-80.11	11	0B	41.96	43	2B	164.03	75	4B	286.10	107	6B	408.17
-116	8C	-442.50	-84	AC	-320.43	-52	CC	-198.36	-20	EC	-76.29	12	0C	45.78	44	2C	167.85	76	4C	289.92	108	6C	411.99
-115	8D	-438.69	-83	AD	-316.62	-51	CD	-194.55	-19	ED	-72.48	13	0D	49.59	45	2D	171.66	77	4D	293.73	109	6D	415.80
-114	8E	-434.88	-82	AE	-312.81	-50	CE	-190.73	-18	EE	-68.66	14	0E	53.41	46	2E	175.48	78	4E	297.55	110	6E	419.62
-113	8F	-431.06	-81	AF	-308.99	-49	CF	-186.92	-17	EF	-64.85	15	0F	57.22	47	2F	179.29	79	4F	301.36	111	6F	423.43
-112	90	-427.25	-80	B0	-305.18	-48	D0	-183.11	-16	F0	-61.04	16	10	61.04	48	30	183.11	80	50	305.18	112	70	427.25
-111	91	-423.43	-79	B1	-301.36	-47	D1	-179.29	-15	F1	-57.22	17	11	64.85	49	31	186.92	81	51	308.99	113	71	431.06
-110	92	-419.62	-78	B2	-297.55	-46	D2	-175.48	-14	F2	-53.41	18	12	68.66	50	32	190.73	82	52	312.81	114	72	434.88
-109	93	-415.80	-77	B3	-293.73	-45	D3	-171.66	-13	F3	-49.59	19	13	72.48	51	33	194.55	83	53	316.62	115	73	438.69
-108	94	-411.99	-76	B4	-289.92	-44	D4	-167.85	-12	F4	-45.78	20	14	76.29	52	34	198.36	84	54	320.43	116	74	442.50
-107	95	-408.17	-75	B5	-286.1	-43	D5	-164.03	-11	F5	-41.96	21	15	80.11	53	35	202.18	85	55	324.25	117	75	446.32
-106	96	-404.36	-74	B6	-282.29	-42	D6	-160.22	-10	F6	-38.15	22	16	83.92	54	36	205.99	86	56	328.06	118	76	450.13
-105	97	-400.54	-73	B7	-278.47	-41	D7	-156.4	-9	F7	-34.33	23	17	87.74	55	37	209.81	87	57	331.88	119	77	453.95
-104	98	-396.73	-72	B8	-274.66	-40	D8	-152.59	-8	F8	-30.52	24	18	91.55	56	38	213.62	88	58	335.69	120	78	457.76
-103	99	-392.91	-71	B9	-270.84	-39	D9	-148.77	-7	F9	-26.7	25	19	95.37	57	39	217.44	89	59	339.51	121	79	461.58
-102	9A	-389.10	-70	BA	-267.03	-38	DA	-144.96	-6	FA	-22.89	26	1A	99.18	58	3A	221.25	90	5A	343.32	122	7A	465.39
-101	9B	-385.28	-69	BB	-263.21	-37	DB	-141.14	-5	FB	-19.07	27	1B	103.00	59	3B	225.07	91	5B	347.14	123	7B	469.21
-100	9C	-381.47	-68	BC	-259.4	-36	DC	-137.33	-4	FC	-15.26	28	1C	106.81	60	3C	228.88	92	5C	350.95	124	7C	473.02
-99	9D	-377.66	-67	BD	-255.58	-35	DD	-133.51	-3	FD	-11.44	29	1D	110.63	61	3D	232.70	93	5D	354.77	125	7D	476.84
-98	9E	-373.84	-66	BE	-251.77	-34	DE	-129.7	-2	FE	-7.63	30	1E	114.44	62	3E	236.51	94	5E	358.58	126	7E	480.65
-97	9F	-370.03	-65	BF	-247.96	-33	DF	-125.89	-1	FF	-3.81	31	1F	118.26	63	3F	240.33	95	5F	362.40	127	7F	484.47

Notes:

1. A positive trim value increases the frequency by steps * ppm / step (decreases the period time).
2. A negative trim value decreases the frequency by steps * ppm / step (increases the period time).

8.10 Alarms

The AS1801 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h - 0Ah. Alarm 2 can be set by writing to registers 0Bh - 0Dh. The alarms can be programmed (by the INTCN bit of the control register) to operate in two different modes. Each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (see Table 6 on page 10). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h - 06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 14 on page 16 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/DT bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 - 5 of that register reflects the day of the week or the date of the month. If DY/DT is written to logic 0, the alarm is the result of a match with date of the month. If DY/DT is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding alarm flag bit (A1F or A2F) is set to logic 1. If the corresponding alarm interrupt enable (A1IE or A2IE) is also set to logic 1, the alarm condition activates one of the interrupt output (VCC or SQW/INT) signals. The match is tested on the once-per-second update of the time and date registers.

Table 14. Alarm Mask Bits

$^{DY}\sqrt{DT}$	Alarm 1 Register Mask Bits (Bit7)				Alarm Rate
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

$^{DY}\sqrt{DT}$	Alarm 2 Register Mask Bits (Bit7)			Alarm Rate
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

8.11 Special-Purpose Registers

The AS1801 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Table 15. Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FREE	0	WAITF	RS2	RS1	INTCN	A2IE	A1IE

8.11.1 Bit 7: Free Bit (FREE)

This is a general purpose register flag for the user. When set to logic 0 it remains logic 0 without interfering with the other registers.

8.11.2 Bit 5: Wait Flag (WAITF)

The Wait flag is set to logic 1 after power on reset and after any write access to a calendar register (address 0 to 6). When WAITF is logic 1, the clock/calendar is stopped and the date/time can be entered. Set WAITF to logic 0 to clear the registers and to start the clock/calendar.

8.11.3 Bits 4 and 3: Rate Select (RS2 and RS1)

These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

Table 16. SQW/INT Output

Control Register [0EH], bits [4:0]					SQW/INT Output
RS2	RS1	INTCN	A2IE	A1IE	
X	X	1	X	1	Alarm 1 match out (A1F)
X	X	1	1	0	Alarm 2 match out (A2F)
0	0	0	X	X	1Hz
0	1	0	X	X	4096Hz
1	0	0	X	X	8192Hz
1	1	0	X	X	32kHz

8.11.4 Bit 2: Interrupt Control (INTCN)

This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers and a match between the timekeeping registers and the alarm 2 registers activates the SQW/INT pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is put on the SQW/INT pin. This bit is set to logic 0 when power is first applied.

8.11.5 Bit 1: Alarm 2 Interrupt Enable (A2IE)

When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert VCC (when INTCN = 0) or to assert SQW/INT (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

8.11.6 Bit 0: Alarm 1 Interrupt Enable (A1IE)

When set to logic 1, this bit permits the alarm 1 flag bit (A1F) in the status register to assert INTA. When the A1IE bit is set to logic 0, the A1F bit does not initiate the VCC signal. The A1IE bit is disabled (logic 0) when power is first applied.

Table 17. Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	TSA	A2F	A1F

8.11.7 Bit 7: Oscillator Stop Flag (OSF)

A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.

2) The voltage present on VCC is insufficient to support oscillation.

This bit remains at logic 1 until written to logic 0.

8.11.8 Bit 2: Time Setting Alarm Flag (TSA)

A logic 1 indicates, that a wrong input value for seconds, minutes, hours, weekday, day, month or year occurred. As long as this bit is not cleaned via the I²C interface the SQW/INT is not triggered.

A logic 0 indicates, that all values in the correct range.

8.11.9 Bit 1: Alarm 2 Flag (A2F)

A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on SQW/INT depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the INTA pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/INT pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

8.11.10 Bit 0: Alarm 1 Flag (A1F)

A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also logic 1, the SQW/INT pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

8.12 I²C Serial Data Bus

The AS1801 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCLK), controls the bus access and generates the START and STOP conditions must control the bus. The AS1801 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The AS1801 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCLK.

The following bus protocol has been defined (see Figure 10 on page 19):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

8.12.1 Bus Not Busy

Both data and clock lines remain HIGH.

8.12.2 Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

8.12.3 Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

8.12.4 Data Valid

The state of the data line represents valid data, after a START condition and the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can only change during the LOW period of the clock signal. There is one clock pulse per bit of data.

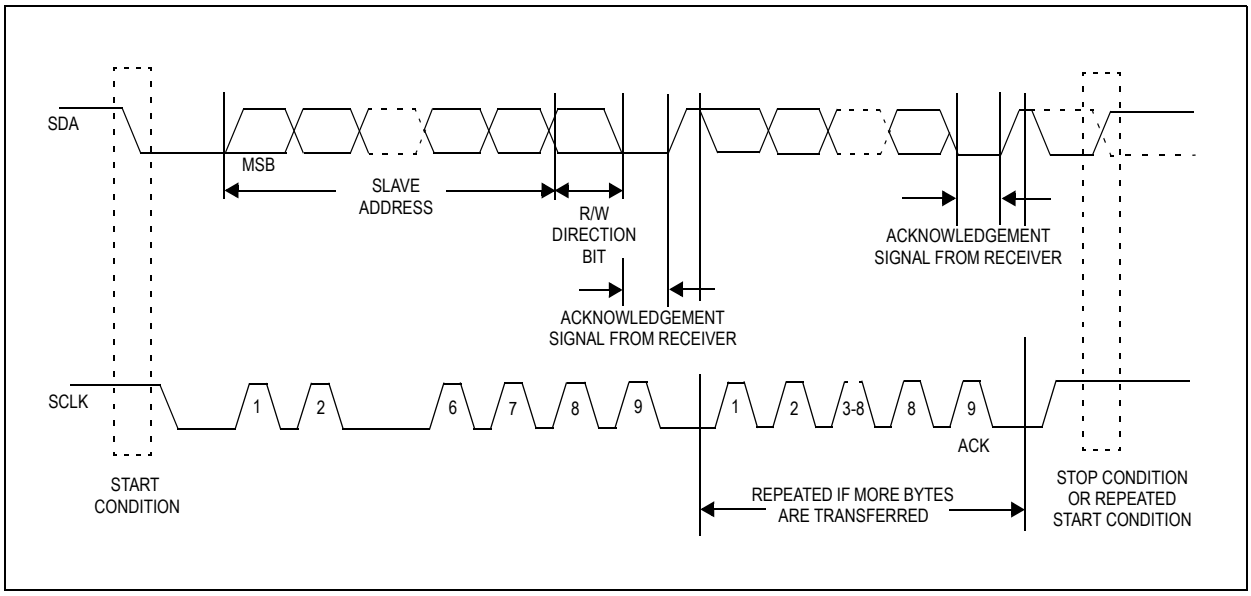
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

8.12.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 10. Data Transfer on I²C Serial Bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS1801 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCLK. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 11 on page 20). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS1801 address, which is 1101000, followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS1801 acknowledges the slave address + write bit, the master transmits a register address to the AS1801. This sets the register pointer on the AS1801. The master may then transmit zero or more bytes of data, with the AS1801 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1801 while the serial clock is input on SCLK. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 12 and Figure 13 on page 20). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS1801 address, which is 1101000, followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS1801 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS1801 must receive a “not acknowledge” to end a read.

Figure 11. Data Write - Slave Receiver Mode

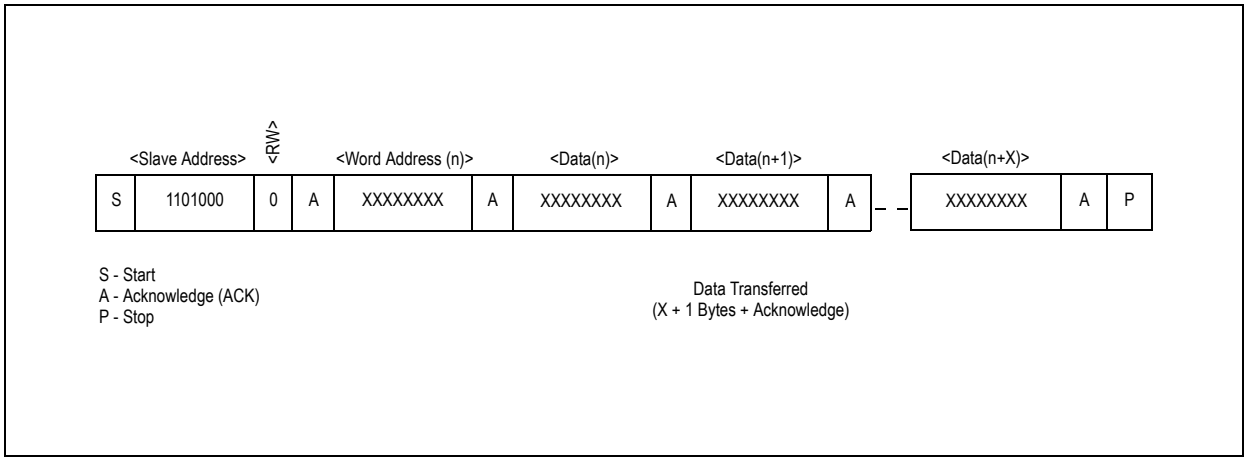


Figure 12. Data Read (from Current Pointer Location) - Slave Transmitter Mode

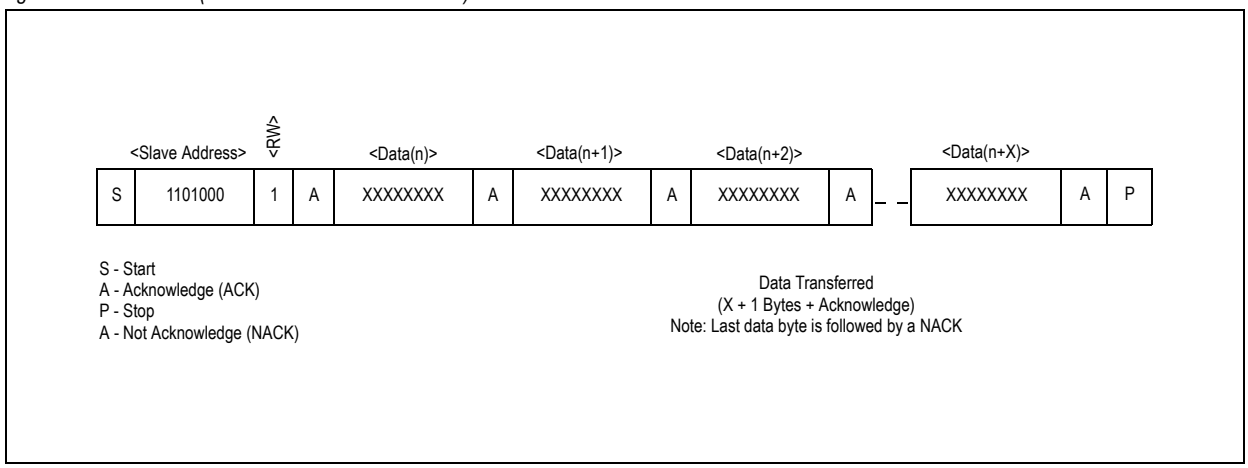
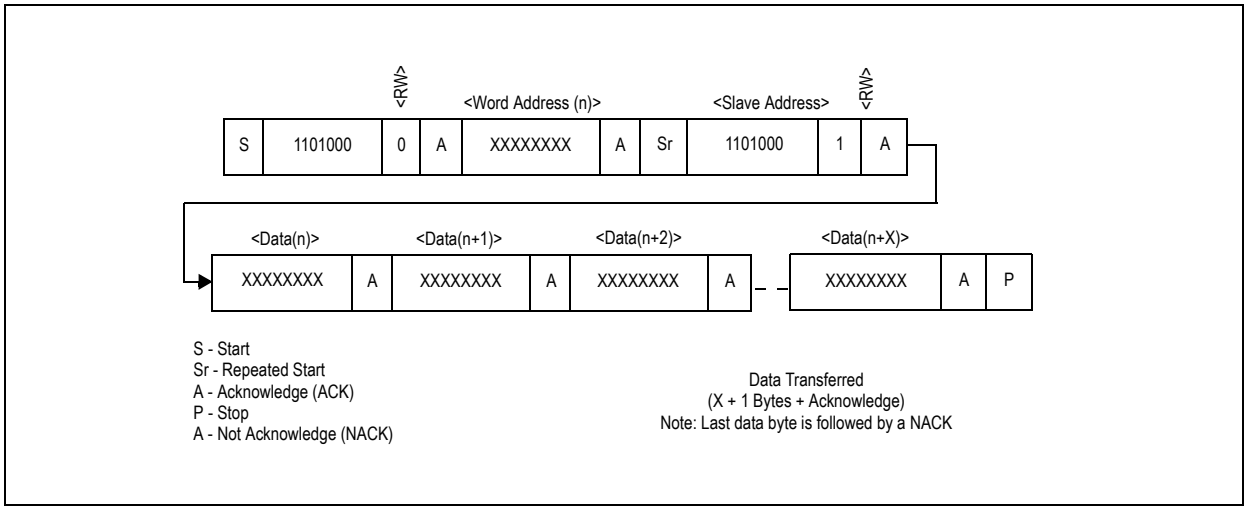


Figure 13. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



9 Application Information

9.1 Back-up Sources

There are some possibilities to choose as a back-up source for RTC back-up.

- Super Capacitors
- Lithium Manganese Dioxide Primary Coin Cells (e.g. CRxxxx types)
- Lithium Manganese Dioxide Rechargeable Coin Cells (e.g. MLxxxx types)
- Electric Double Layer Ultra-Capacitors (EDLC)

Nickel metal hydride and nickel cadmium types should not be used as they are incompatible with the trickle charging method of the AS1801. Choice of type will depend on back-up time, operating temperature, number of discharge cycles, and self-discharge.

Always refer to the manufacturer's recommendations, particularly for charging current and voltage when ML battery types are used. Charge voltage should never be >3.3V, and nominal charge current should be 2mA or lower (depends on cell size). Similarly, for ultra-capacitors, maximum operating voltage and temperature limits should be observed.

Coin cells are available from Maxell, Energiser, Panasonic, Varta and Duracell amongst others.

9.2 Estimating Back-up time with Super Capacitor Storage

The trickle charger can be used to charge a secondary battery or capacitor. The battery or capacitor is used to maintain operation of the clock when the supply voltage on VCC is absent. The energy stored in the capacitor or battery will maintain clock operation for a period of time that is determined by several factors.

The user determines the diode and resistor selection according to the maximum current required for capacitor charging. See the description of Trickle-Charge Register on page 11. Contact the manufacturer of the capacitor or check the capacitor datasheet for charging-current limits.

9.2.1 Charging-Current Calculations

The maximum charging current can be calculated as follows. Assume that a system power supply of 3.3V is applied to VCC and that the trickle charger has been enabled with no diode and a 2kΩ resistor. The maximum current, when the capacitor voltage is zero, would be calculated as:

$$I_{CHARGEmax} = \frac{V_{CC} - Vdiode}{R4} = \frac{3.3V - 0V}{2k\Omega} = 1.65mA \qquad \text{(EQ 2)}$$

9.2.2 Calculating Back-up Time

Given the desired backup time, several parameters are required before capacitor size can be determined. They are initial and final capacitor voltages, and drain current.

Assume that the RTC draws a constant current while running from V_{BACKUP}, then the worst-case backup time in seconds would be:

$$T_{BACKUP}[\mathrm{seconds}] = \frac{C \times (V_{BATstart} - V_{BATend})}{I_{BACKUP}} \qquad \text{(EQ 3)}$$

Where:

C [F] . . . . is the back-up capacitor value

$V_{BAT\ start}$ [V] . . . . is the initial voltage (the voltage applied to V_{BAT}, less the voltage drop from the diodes and resistors, if any, used in the charging circuit

$V_{BAT\ end}$ [V] . . . . is the ending voltage (minimum oscillator operating voltage)

I_{BACKUP} [A] . . . . is the maximum battery current from the datasheet and is very nearly constant down to an operating voltage of 0.9V. Storage capacitor self-leakage should be added to the backup current as necessary.

As an example, a back-up system with C = 0.2F, $V_{BAT\ start}$ = 3.3V, $V_{BAT\ end}$ = 0.9V and I_{BACKUP} = 0.5µA:

$$T_{BACKUP}[\mathrm{seconds}] = \frac{0.2 \times (3.3 - 0.9)}{0.5uA} = 960000\,\mathrm{sec} = 267h \qquad \text{(EQ 4)}$$

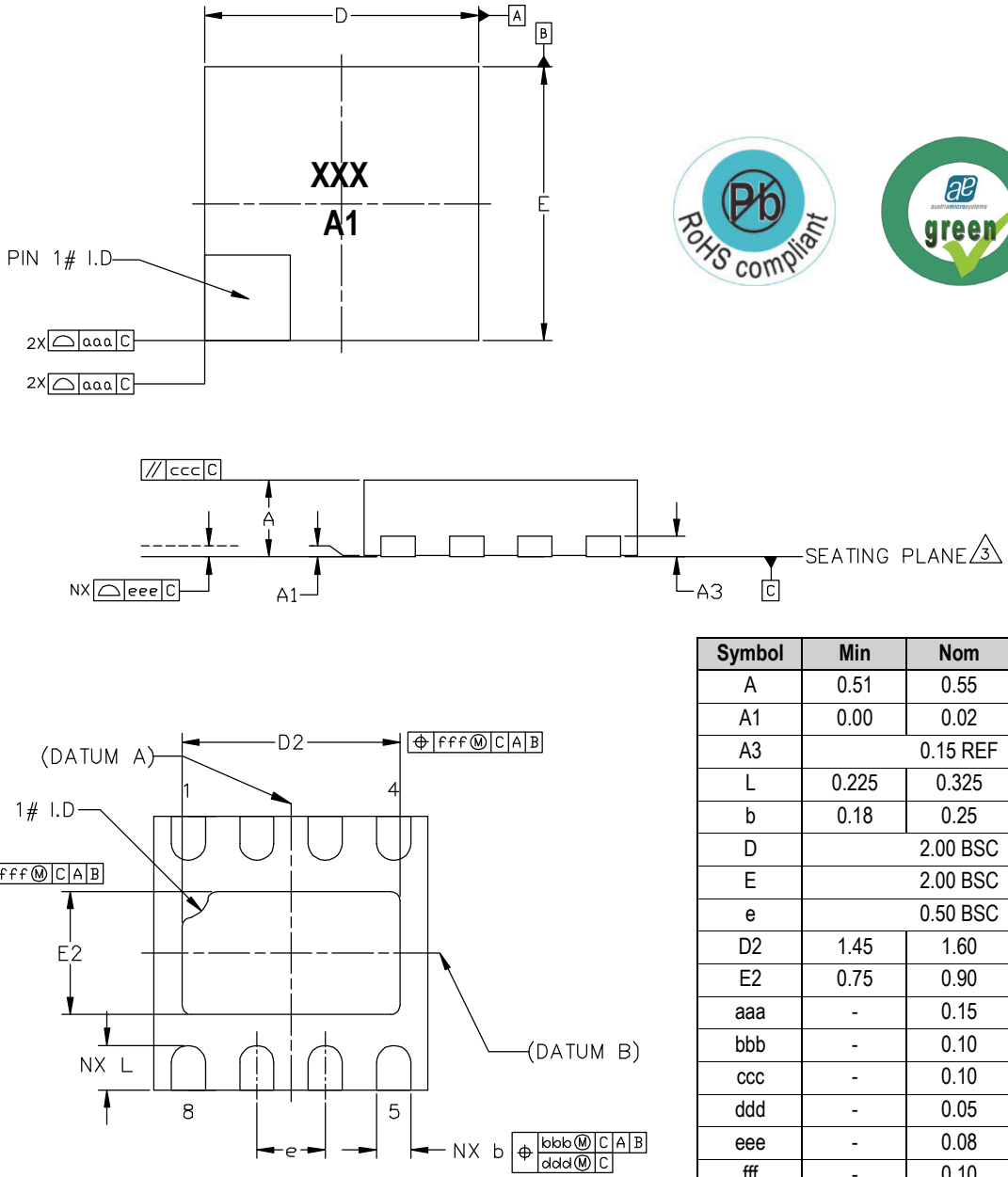
9.3 EDLC (Electric Double-layer Capacitor) Manufacturers

- Cooper Bussmann (http://www.cooperbussmann.com/)
- Elna America Inc (http://www.elna-america.com/)
- Illinois Capacitor Inc (http://illinoiscapacitor.com/)
- Maxwell Technologies Inc (http://www.maxwell.com/)
- NEC-Tokin (http://www.nec-tokin.com/)
- Nichicon (http://www.nichicon-us.com/)
- Panasonic Industrial Components (http://www.industrial.panasonic.com/)
- Taiyo Yuden (http://www.t-yuden.com/)

10 Package Drawings and Markings

The device is available in a 8-pin TDFN (2x2mm) package.

Figure 14. Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.51	0.55	0.60
A1	0.00	0.02	0.05
A3		0.15 REF	
L	0.225	0.325	0.425
b	0.18	0.25	0.30
D		2.00 BSC	
E		2.00 BSC	
e		0.50 BSC	
D2	1.45	1.60	1.70
E2	0.75	0.90	1.00
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		8	

Notes:

1. Dimensions & tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Revision History

Revision	Date	Owner	Description
-	-	-	Initial revision
1.6	09 Nov, 2011	afe	Updated trickle charge description and register information. Added new applications section.
1.7	14 Nov, 2011		Added VCC to VBAT Changeover (page 9)
1.8	20 Apr, 2012		Updated the section on Calculating Back-up Time (page 21)

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The devices are available as the standard products shown in Table 18.

Table 18. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1801-BTDT	A1	Ultra-Low Power, I²C Serial Real-Time Clock with Trickle Charger	Tape and Reel	8-pin TDFN (2x2mm)

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