AS1539/AS1541

DataSheet

8/4-Channel, 10-Bit I²C Analog-to-Digital Converter

1 General Description

The AS1539/AS1541 are single-supply, low-power, 10-bit data acquisition devices featuring a serial I²C interface and an 8-channel (AS1539) or 4-channel (AS1541) multiplexer.

The analog-to-digital (A/D) converters features a sample-and-hold amplifier an internal asynchronous clock and an internal reference.

The combination of an I^2C serial, 2-wire interface and micropower consumption makes the AS1539 and AS1541 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation.

The device is available in a TSSOP-16 or TQFN 4x4 16-pin package.

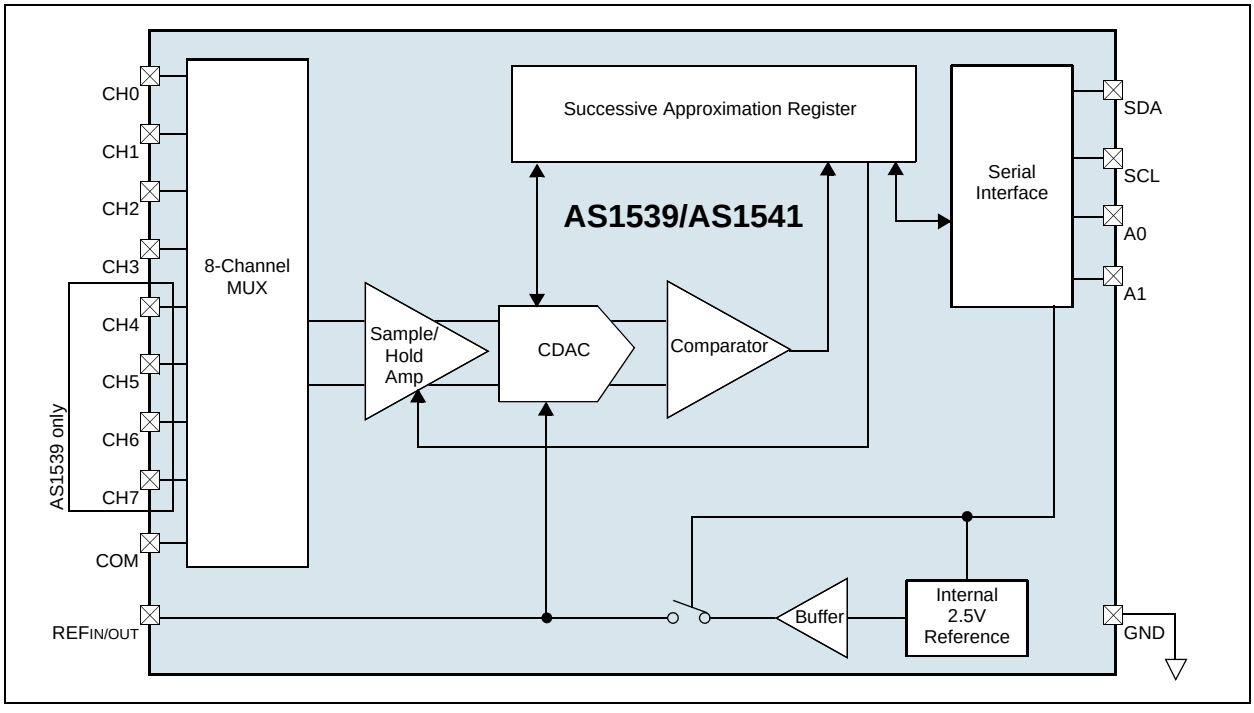
2 Key Features

- Single Supply: 2.7 to 5.25V
- 8-Channel Multiplexer (AS1539)
- 4-Channel Multiplexer (AS1541)
- Sampling Rate: 50kSPS
- No Missing Codes
- Internal Reference: 2.5V
- High Speed I^2C Interface at 3.4MHz
- <1.5µA Full Shutdown Current
- TSSOP-16 or TQFN 4x4 16-pin Package

3 Applications

The device is ideal for voltage-supply monitoring, isolated data acquisition, transducer interfaces, battery-operated systems, remote data acquisition or any other analog-to-digital conversion application.

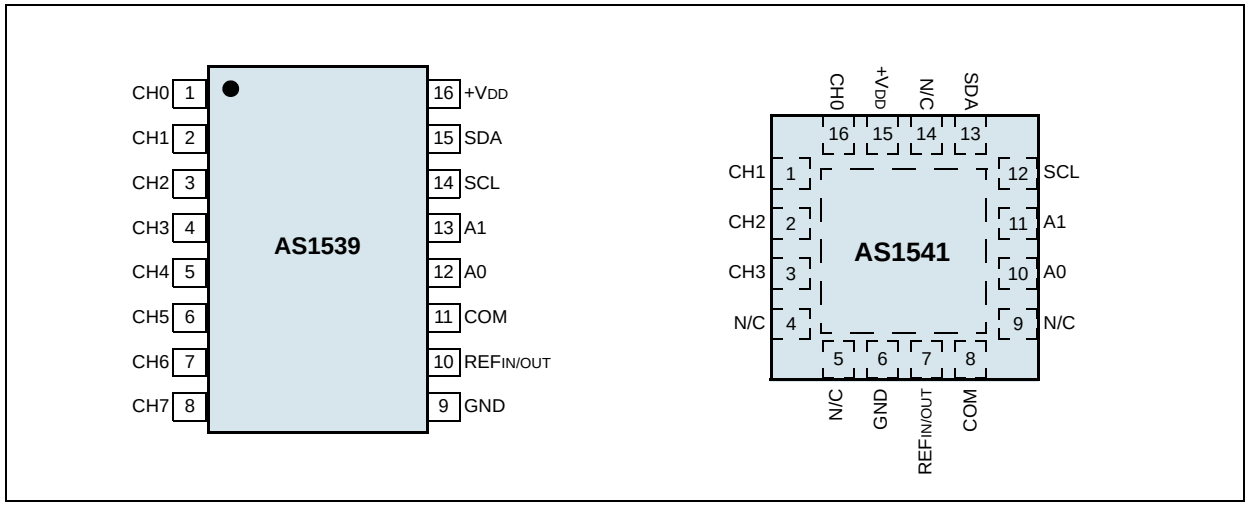
Figure 1. Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

AS1539	AS1541	Pin Name	Description
-	1:3,16	CH0:CH3	**Analog Input Channels 0 to 3**
1:8	-	CH0:CH7	**Analog Input Channels 0 to 7**
9	6	GND	**Analog Ground**
10	7	$REF_{IN/OUT}$	**Internal Reference/External Reference Input**
11	8	COM	**Analog Input Channel Common**
12	10	A0	**Slave Address Bit 0**
13	11	A1	**Slave Address Bit 1**
14	12	SCL	**Serial Clock**
15	13	SDA	**Serial Data**
16	15	$+V_{DD}$	**Power Supply Input**. 2.7 to 5.25V.
-	4, 5, 9, 14	NC	**Not Connected**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
+V_{DD} to GND	-0.3	+6	V	
Digital Input Voltage to GND	-0.3	+V_{DD} + 0.3	V	
Thermal Resistance θ_{JA}		100	°C/W	on PCB
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Junction Temperature (T_{JMAX})		150	ºC	
ESD	1.5		kV	*HBM MIL-Std. 883E 3015.7* methods
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

Electrical Characteristics

+V_{DD} = +2.7 to +5.25V, V_{REF} = +2.5V external, SCL = 3.4MHz, T_{AMB} = -40 to +85ºC (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Analog Input						
	Fullscale Input Span	Positive input, negative input	0		V_{REF}	V
	Absolute Input Range	Positive input	-0.3		$+V_{DD}$ + 0.3	V
		Negative Input	-0.3		$+V_{DD}$ + 0.3	V
	Capacitance	Track Mode		15		pF
		Hold Mode		8		
I_{LEAK}	Leakage Current			±0.1	±1	µA
Static Performance						
	No Missing Codes		10			Bits
	Integral Linearity Error	V_{REF} = 2.5V, 1 LSB = 610µV		±0.2	±0.375	LSB
	Differential Linearity Error			±0.125	±0.25	LSB
	Offset Error			±0.125	±1.5	LSB
	Offset Error Match[1]			±0.025	±.5	LSB
	Gain Error			±0.25	±1.5	LSB
	Gain Error Match[1]			±0.025	±0.5	LSB
	Power Supply Rejection			1		mV
Dynamic Performance						
	Throughput Frequency				50	kHz
	Conversion Time				6.67	µs
AC Accuracy						
THD	Total Harmonic Distortion [2]	V_{IN} = 2.5V_{P-P} @ 10kHz		-70		dB
	Signal-to-Noise Ratio	V_{IN} = 2.5V_{P-P} @ 10kHz		61.5		dB
	Signal-to-Noise (+ Distortion) Ratio	V_{IN} = 2.5V_{P-P} @ 10kHz		61.5		dB
	Spurious-Free Dynamic Range	V_{IN} = 2.5V_{P-P} @ 10kHz		70		dB
Voltage Reference Output						
	Range		2.475	2.5	2.525	V
	Internal Reference Drift			30		ppm/ºC
	Output Impedance			30		Ω
	Quiescent Current			440		µA
Voltage Reference Input						
	Range		1		V_{DD}	V
	Input Resistance			1		GΩ
	Reference Input Current	PD = 01 Internal Ref. OFF, ADC ON @ 50kSPS		4		µA

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CMOS Digital I/O						
V_{IH}	Input High Logic Level		$+V_{DD}$ x 0.7		$+V_{DD}$ + 0.5	V
V_{IL}	Input Low Logic Level		-0.3		$+V_{DD}$ x 0.3	V
V_{OL}	Output Low Logic Level	3mA sink current			0.4	V
I_{IH}	Input High Leakage Current	$V_{IH} = +V_{DD}$			1	µA
I_{IL}	Input Low Leakage Current	V_{IL} = GND	-1			µA
	Data Format	Straight binary				
Power Supply Requirements						
$+V_{DD}$	Power Supply Voltage	Specified performance	2.7		5.25	V
I_{QSTAT}	Analog Current in Static Mode, 3.6V	PD = 00 Full Power-Down		0.04	1.2	µA
		PD = 01 Internal Ref. OFF, ADC ON		400	500	
		PD = 10 Internal Ref. ON, ADC OFF		500	600	
		PD = 11 Internal Ref. ON, ADC ON		800	900	
	Analog Current in Static Mode, 5.25V	PD = 00 Full Power-Down		0.04	1.5	µA
		PD = 01 Internal Ref. OFF, ADC ON		450	550	
		PD = 10 Internal Ref. ON, ADC OFF		550	650	
		PD = 11 Internal Ref. ON, ADC ON		850	950	
I_Q	Quiescent Current at Full Speed, 3.6V	PD = 01 Internal Ref. OFF, ADC ON		500	600	µA
		PD = 11 Internal Ref. ON, ADC ON		850	950	
	Quiescent Current at Full Speed, 5.25V	PD = 01 Internal Ref. OFF, ADC ON		650	800	µA
		PD = 11 Internal Ref. ON, ADC ON		915	1150	

1. Guaranteed by design and characterized on sample base.
2. THD measure out to 5th harmonic.

Timing Characteristics

$+V_{DD}$ = +2.7 to 5.25V, T_{AMB} = -40 to +85ºC (unless otherwise specified). All values referenced to V_{IHMIN} and V_{ILMAX} levels.

Table 4. Timing Characteristics

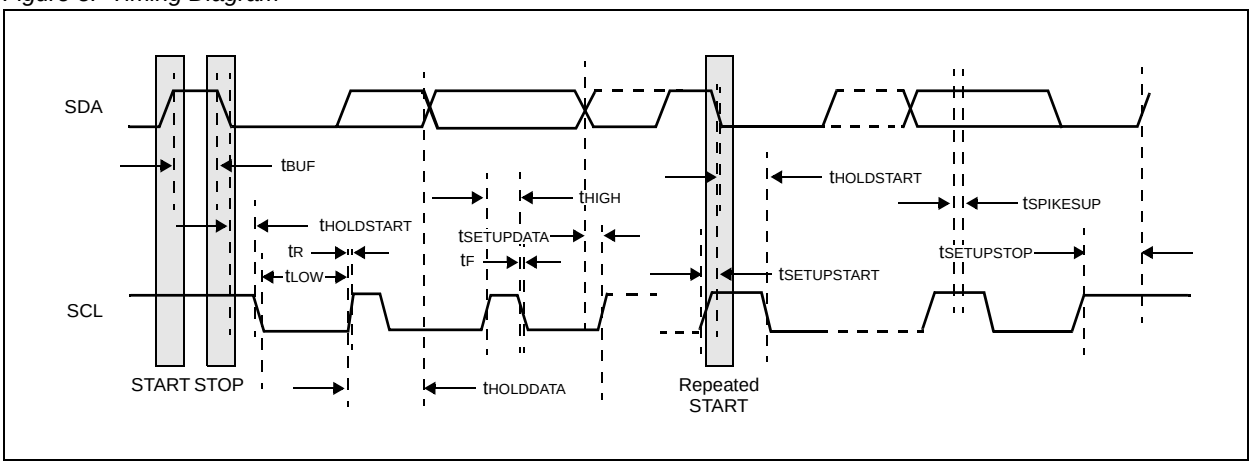
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCL}	SCL Frequency		0.1		3.4	MHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		1.3			µs
$T_{HOLDSTART}$	Hold Time for Repeated START Condition		160			ns
t_{LOW}	SCL Low Period		50		75	ns
t_{HIGH}	SCL High Period		50		75	ns
$T_{SETUPSTART}$	Setup Time for Repeated START Condition		100			ns
$T_{SETUPDATA}$	Data Setup Time		10			ns
$T_{HOLDDATA}$	Data Hold Time				70	ns
$T_{RISESCLK}$[1]	SCL Rise Time		10		40	ns
$T_{RISESCLK1}$[1]	SCL Rise Time after Repeated START Condition and After an ACK Bit		10		80	ns

Table 4. Timing Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{FALLSCLK}$[1]	SCL Fall Time		10		40	ns
$T_{RISESDA}$[1]	SDA Fall Time		20		80	ns
$T_{FALLSDA}$[1]	SDA Fall Time		20		80	ns
$T_{SETUPSTOP}$	STOP Condition Setup Time		160			ns

1. Guaranteed by design and characterized on sample base.

Figure 3. Timing Diagram



7 Typical Operating Characteristics

V_{DD} = 3.6V; V_{REF} = 2.5V (internal), f_{SCL} = 3.4MHz, C_{REF} = 4.7µF, T_{AMB} = +25ºC (unless otherwise specified).

Figure 4. DNL vs. Digital Output Code, Int. Reference

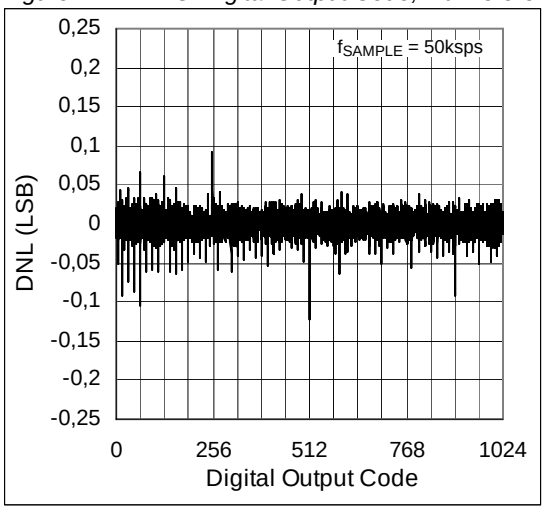


Figure 5. INL vs. Digital Output Code, Int. Reference

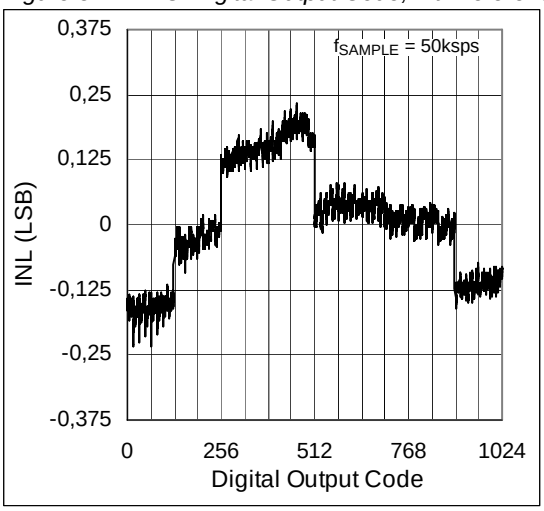


Figure 6. DNL vs. Digital Output Code, Ext. Reference

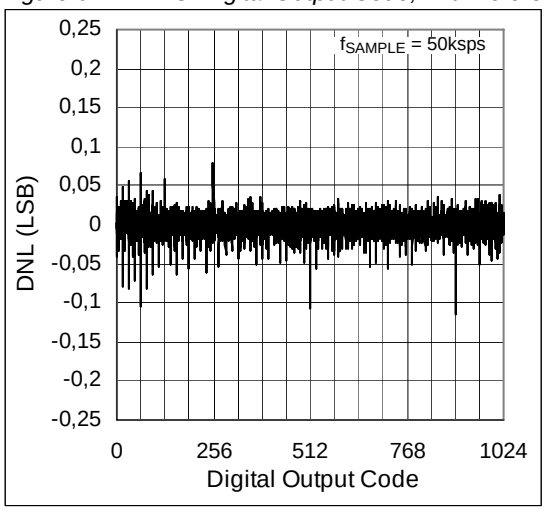


Figure 7. INL vs. Digital Output Code, Ext. Reference

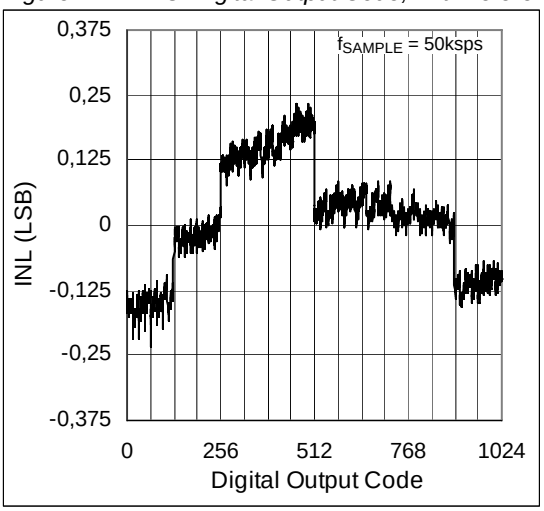


Figure 8. Offset Error vs. Temperature

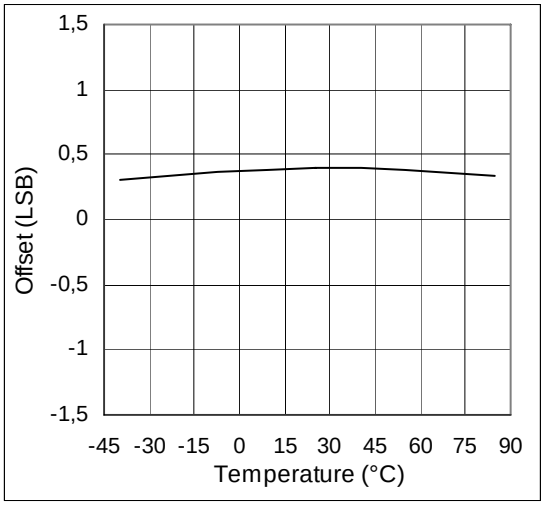


Figure 9. Offset Matching vs. Temperature

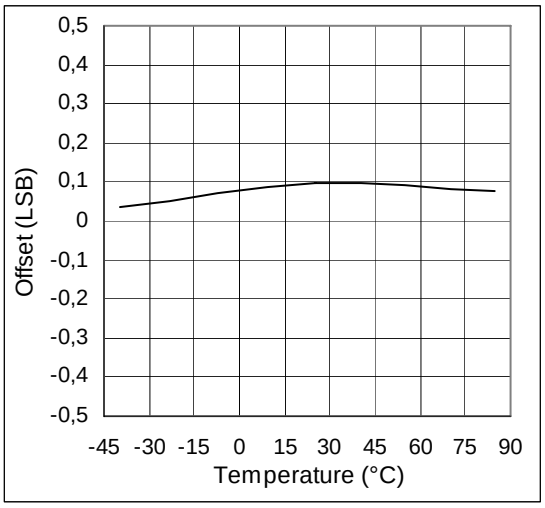


Figure 10. Offset Error vs. Supply Voltage

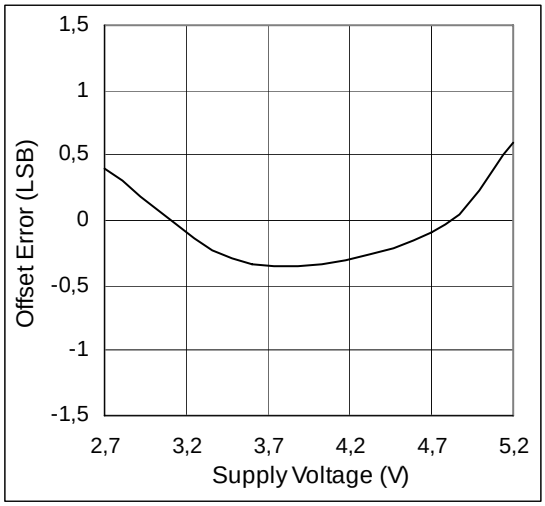


Figure 11. Offset Matching vs. Supply Voltage

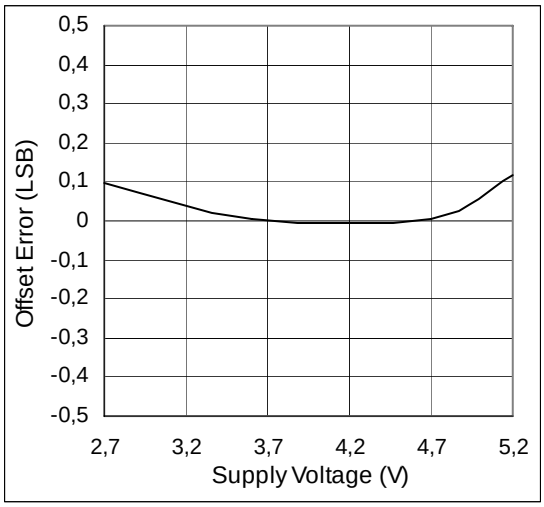


Figure 12. Gain Error vs. Temperature

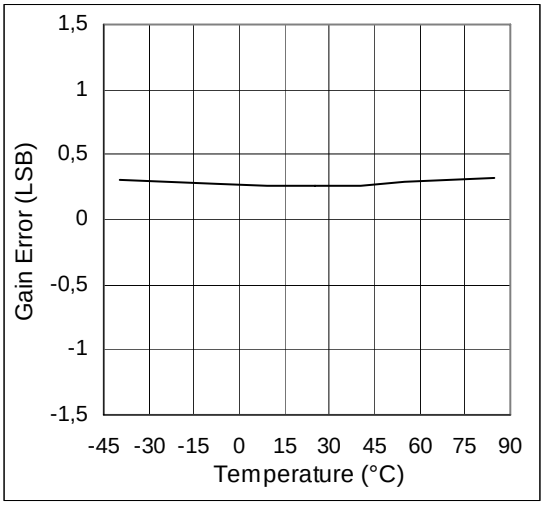


Figure 13. Gain Matching vs. Temperature

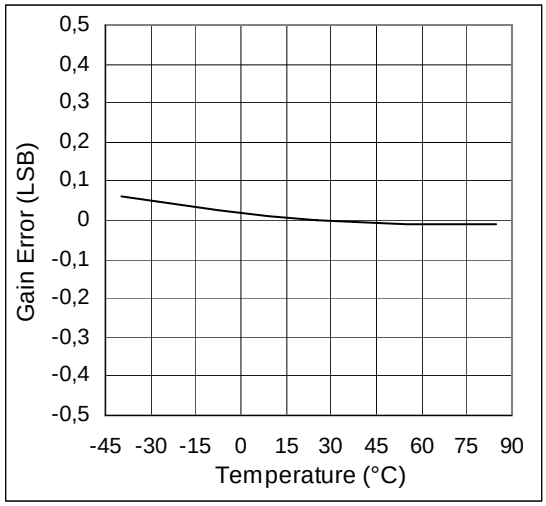


Figure 14. Gain Error vs. Supply Voltage

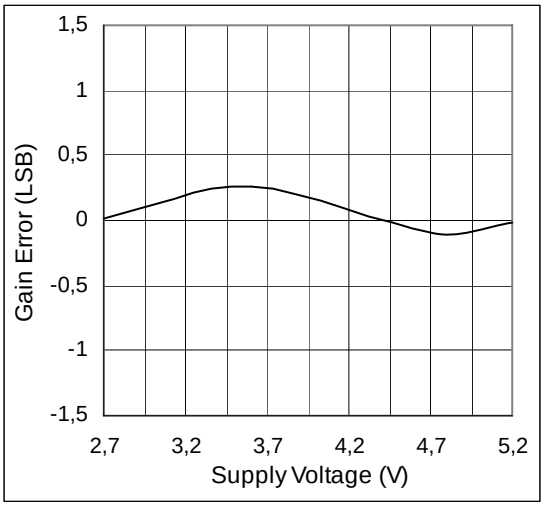


Figure 15. Gain Matching vs. Supply Voltage

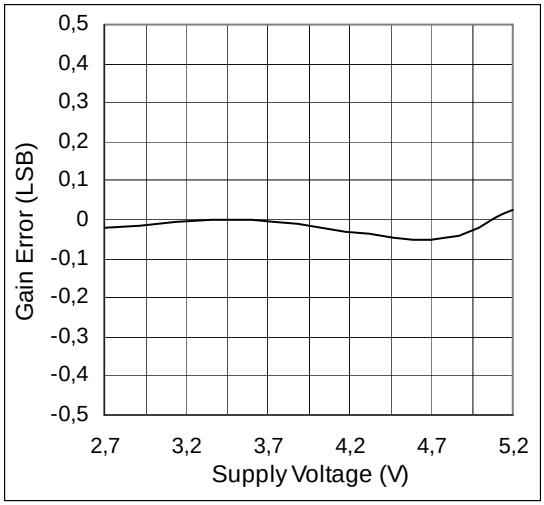


Figure 16. Supply Current vs. Supply Voltage, PD=00

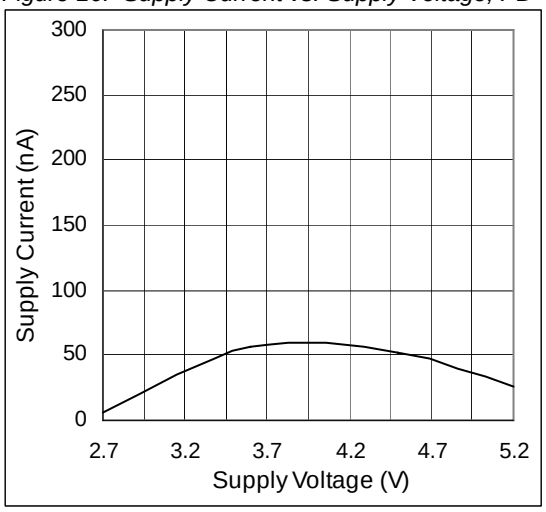


Figure 17. Supply Current vs. Supply Voltage, PD=01

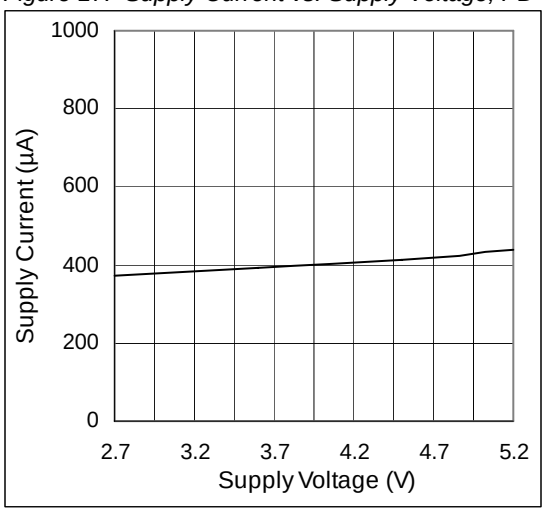


Figure 18. Supply Current vs. Supply Voltage, PD=11

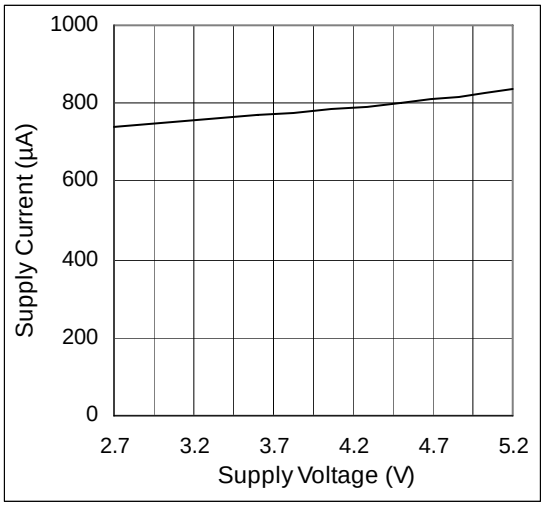


Figure 19. Supply Current vs. Sampling Rate, PD = 11

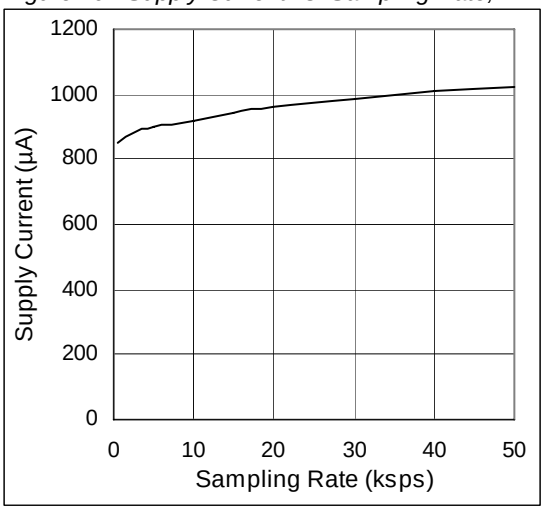


Figure 20. FFT, Int. Reference

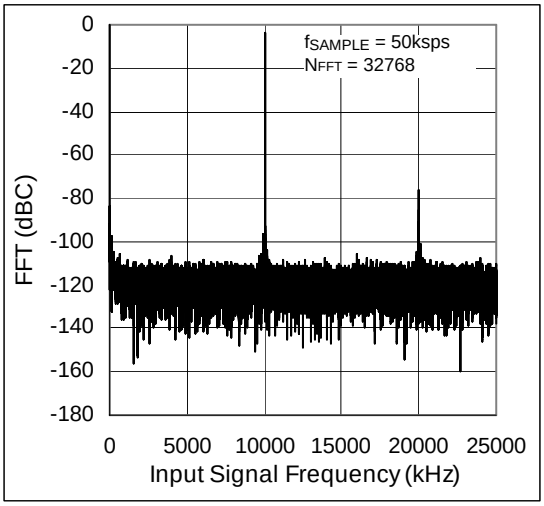
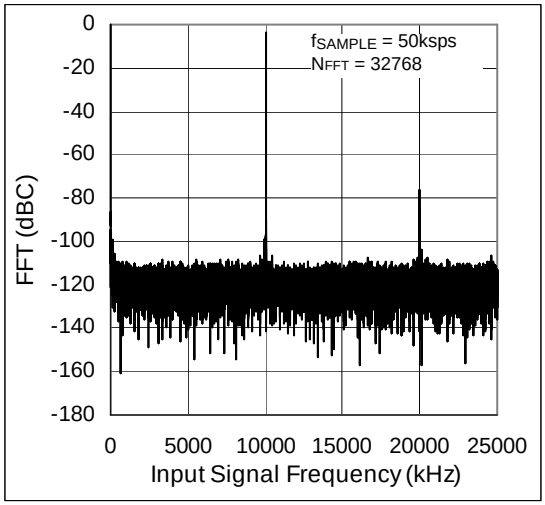


Figure 21. FFT, Ext. Reference

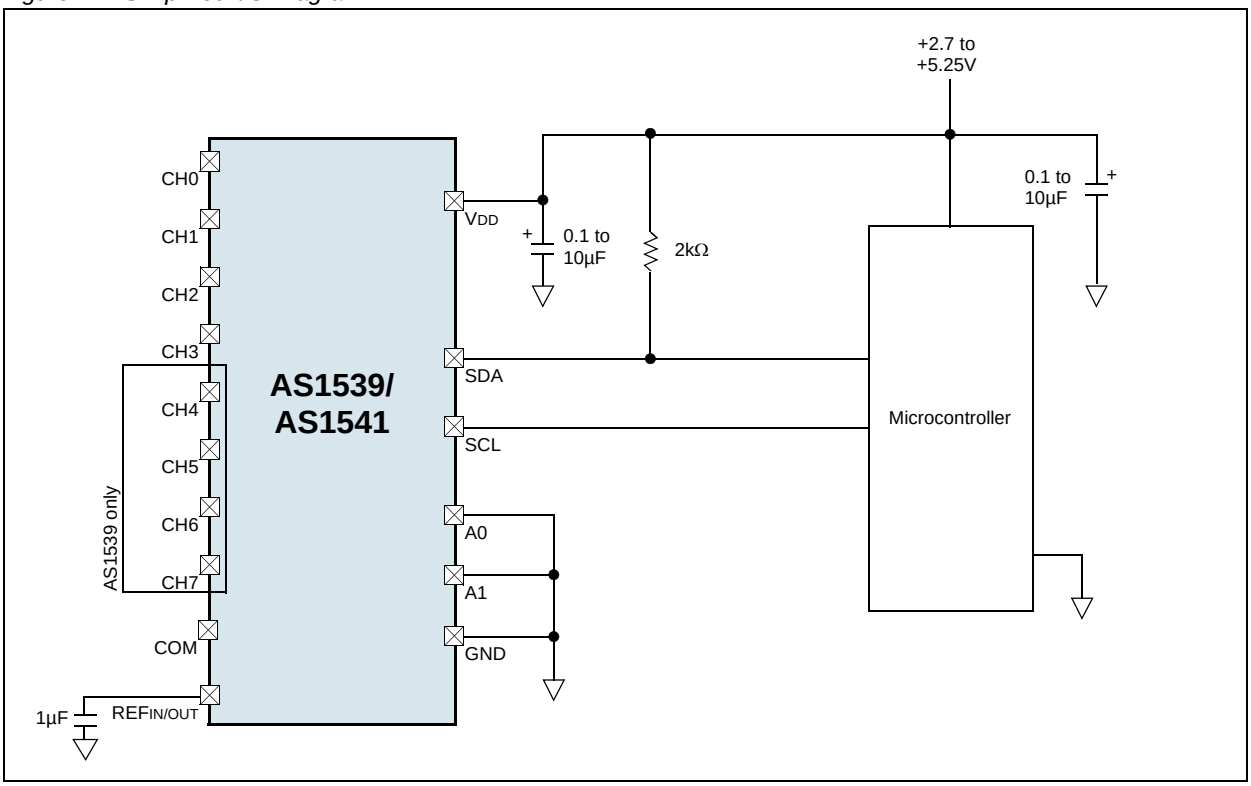


8 Detailed Description

The AS1539/AS1541 successive approximation register (SAR) A/D converter architecture is based on capacitive redistribution which inherently includes a sample-and- hold function.

The AS1539/AS1541 core is controlled by an internally generated free-running clock. When the device is not performing conversions or being addressed, the A/D converter-core and internal clock are powered off.

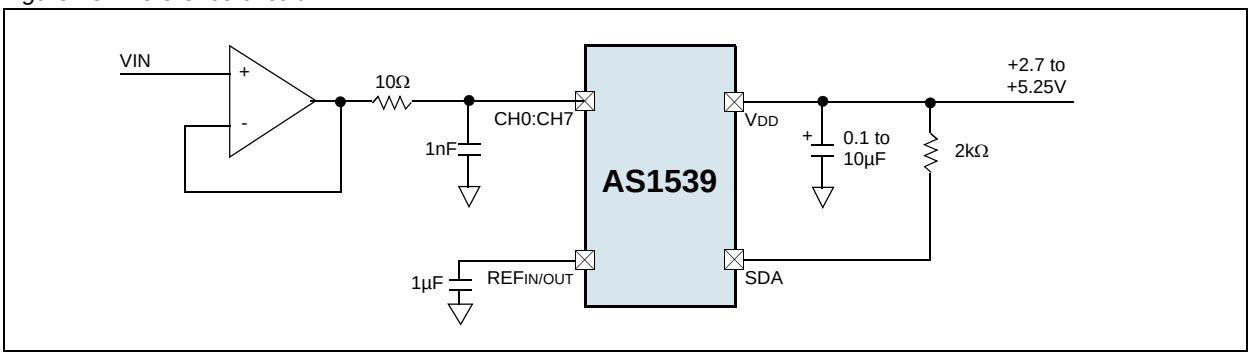
Figure 22. Simplified I/O Diagram



Analog Input

When the converter enters the hold mode, the voltage on the selected CH*x* pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 15pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

Figure 23. Reference circuit



Reference Voltage

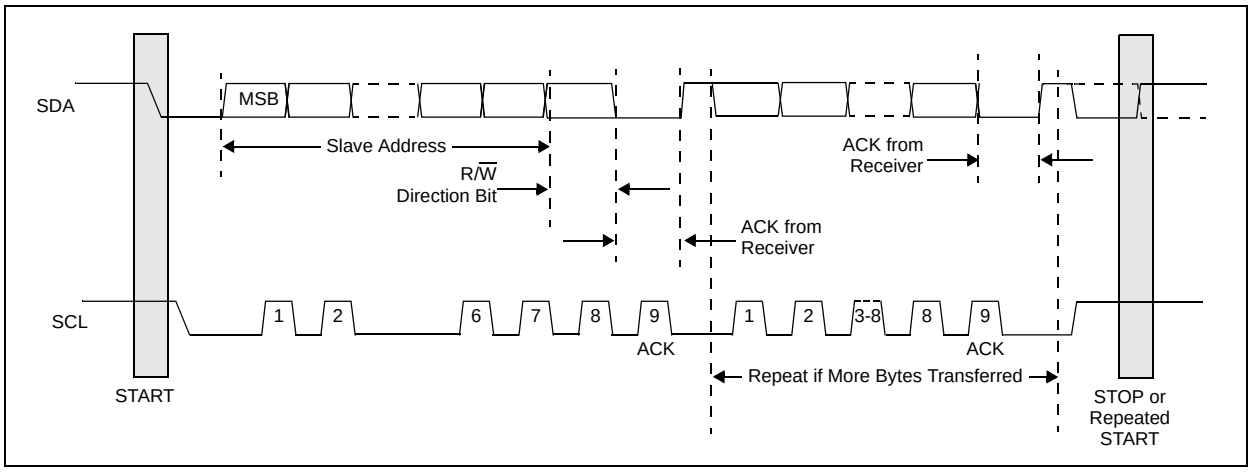
The AS1539/AS1541 can operate with an internal 2.5V reference or an external reference. If a +5V supply is used, an external +5V reference is required in order to provide full dynamic range for a 0V to +VDD analog input. The external reference can be as low as 1V. When using a +2.7V supply, the internal +2.5V reference will provide full dynamic range for a 0V to +2.5V analog input.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 1024. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

Digital Interface

The AS1539/AS1541 supports the I^2C serial bus and data transmission protocol in high-speed mode at 3.4MHz. The AS1539/AS1541 operates as a slave on the I^2C bus. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA.

Figure 24. Bus Protocol



The bus protocol (as shown in Figure 24) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.
- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfe**r. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.
  Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

  Within the I^2C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge

bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 24 on page 11 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

- **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The AS1539 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1539 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Address Byte

The address byte (see Figure 25) is the first byte received following the START condition from the master device.

Figure 25. Address Byte

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

- The first five bits (MSBs) of the slave address are factory-set to 10010.
- The next two bits of the address byte are the device select bits, A1 and A0, which are set by the state of pins A1 and A0 at startup. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time. Pins A1/A0 can be connected to +V_{DD} or digital ground.
- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS1539 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The AS1539/AS1541 operation, including powerdown (see Table 5) and channel selection (see Table 6) is determined by a command byte (see Figure 26).

Figure 26. Command Byte

MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	X	X

Where:

SD: Single-Ended/Differential Inputs
0: Differential Inputs
1: Single-Ended Inputs
C2, C1, C0: Channel Selections
PD1, PD0: Power-Down Selection
X: Unused

Powerdown Selection

Powerdown modes for the AS1539/AS1541 are selected by setting bits PD0 and PD1 of a command byte (see Command Byte on page 12).

Table 5. Powerdown Mode Bit Settings

PD1	PD0	Description
0	0	Powerdown between A/D converter conversions.
0	1	Internal reference off and A/D converter on.
1	0	Internal reference on and A/D converter off.
1	1	Internal reference on and A/D converter on.

Channel Selection

Channel selection for the AS1539/AS1541 is made using a command byte (see Command Byte on page 12).

Table 6. Channel Selection Bit Settings[1]

	SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
	0	0	0	0	+IN	–IN	-	-	-	-	-	-	-
	0	0	0	1	-	-	+IN	–IN	-	-	-	-	-
AS1539 only	0	0	1	0	-	-	-	-	+IN	–IN	-	-	-
	0	0	1	1	-	-	-	-	-	-	+IN	–IN	-
	0	1	0	0	–IN	+IN	-	-	-	-	-	-	-
	0	1	0	1	-	-	–IN	+IN	-	-	-	-	-
AS1539 only	0	1	1	0	-	-	-	-	–IN	+IN	-	-	-
	0	1	1	1	-	-	-	-	-	-	–IN	+IN	-
	1	0	0	0	+IN	-	-	-	-	-	-	-	–IN
	1	0	0	1	-	-	+IN	-	-	-	-	-	–IN
AS1539 only	1	0	1	0	-	-	-	-	+IN	-	-	-	–IN
	1	0	1	1	-	-	-	-	-	-	+IN	-	–IN
	1	1	0	0	-	+IN	-	-	-	-	-	-	–IN
	1	1	0	1	-	-	-	+IN	-	-	-	-	–IN
AS1539 only	1	1	1	0	-	-	-	-	-	+IN	-	-	–IN
	1	1	1	1	-	-	-	-	-	-	-	+IN	–IN

1. For the 4-channel AS1541 only combinations of CH0:CH3 applies.

9 Application Information

Initiating a Conversion

After the AS1539/AS1541 has been write-addressed by the bus master, the A/D converter circuitry is powered on, and conversions will begin when a command byte bit C0 (see Command Byte on page 12) is received. If the address byte is valid, the AS1539/AS1541 will return an ACK.

Reading Data

Data can be read from the AS1539/AS1541 by read-addressing the device (LSB of address byte set to 1 (see Command Byte on page 12)) and receiving the transmitted bytes. Converted data can only be read from the AS1539/AS1541 once a conversion has been initiated as described in Initiating a Conversion.

Each 12-bit data word (see Figure 27) is returned in two bytes, where D9 is the MSB of the data word, and D0 is the LSB. Byte 0 is sent first, followed by Byte 1.

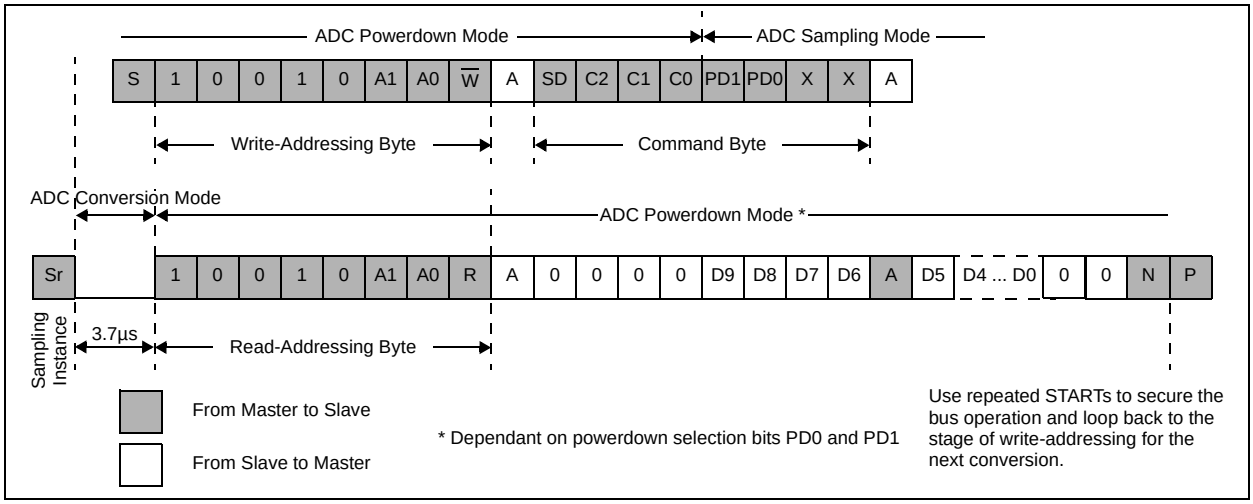
Figure 27. Data Word

	MSB	6	5	4	3	2	1	LSB
Byte 0	0	0	0	0	D9	D8	D7	D6
Byte 1	D5	D4	D3	D2	D1	D0	0	0

Figure 28 illustrates the interaction between the master and the slave AS1539/AS1541.

The most efficient way to perform continuous conversions is to issue repeated STARTs to the AS1539/AS1541 (to secure the bus for subsequent ADC conversions) after reading each conversion. It is recommended that during the conversion mode no data is clocked into the ADC to prevent internal noise. Therefore, after the repeated start commend it is recommanded not to clock in or out any data from the converter for 3.7µs. The ADC powers up after the PD0 bit is clocked in and it takes 1.4µs to fully power up. At a clock frequency of 3.4MHz this time is automatically achieved and no extra delay should be included.

Figure 28. Read Sequence



Where:

A: Acknowledge (SDA Low)
N: Not Acknowledge (SDA High)
S: START Condition
P: STOP Condition
Sr: Repeated START Condition
W: 0 (Write)
R: 1 (Read)

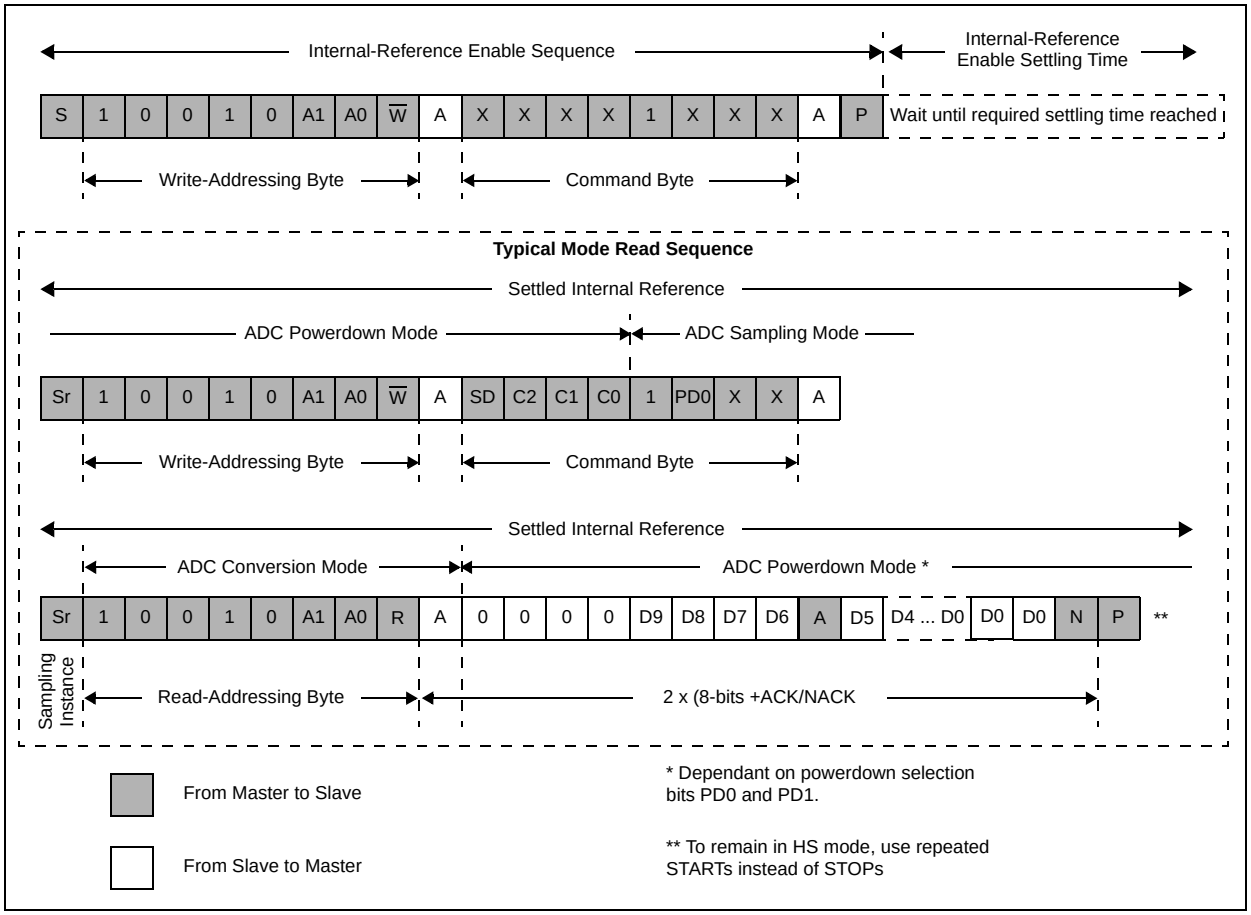
Reading with Internal Reference On/Off

The internal reference defaults to off when the AS1539/AS1541 power is on. If the reference (internal or external) is continuously turned on and off, a proper amount of settling time must be added before a normal conversion cycle can be started. The exact amount of settling time needed varies depending on the reference capacitor. For example for a reference capacitor of 4.7µF and considering the output impedance of the internal reference of 30Ω and the amount of time to fully charge the capacitor will be 1.4ms. If the reference capacitor is not fully discharged this time can be reduced greatly.

Figure 29 shows the correct internal reference enable sequence before issuing the typical read sequences required for the mode when an internal reference is used.

Note: Typical read sequences can be re-used once the internal reference has settled.

Figure 29. Internal Reference Enable Sequence and Typical Read Sequence



Where:

A: Acknowledge (SDA Low)
N: Not Acknowledge (SDA High)
S: START Condition
P: STOP Condition
Sr: Repeated START Condition
W: 0 (Write)
R: 1 (Read)
X: Dont Care

When using the internal reference:

1. Bit PD1 off the command byte must always be set to logic 1 for each sample conversion that is issued by the sequence, as shown in Figure 28 on page 14.
2. In order to achieve 10-bit accuracy conversion when using the internal reference, the internal reference settling time must be considered.

   If bit PD1 has been set to logic 0 while using the AS1539/AS1541, then the settling time must be reconsidered after PD1 is set to logic 1 (i.e., whenever the internal reference is turned on after it has been turned off, the settling time must be long enough to get 10-bit accuracy conversion).
3. When the internal reference is off, it is not turned on until both the first command byte with PD1 = 1 is sent and then a STOP condition or repeated START condition is issued. (The actual turn-on time occurs once the STOP or repeated START condition is issued.) Any command byte with PD1 = 1 issued after the internal reference is turned on serves only to keep the internal reference on. Otherwise, the internal reference would be turned off by any command byte with PD1 = 0.

The example in Figure 29 can be generalized for a conversion cycle by simply swapping the timing of the conversion cycle.

Note: If an external reference is used, PD1 must be set to 0, and the external reference must be settled. The typical sequence in Figure 28 on page 14 or Figure 29 on page 15 can then be used.

Layout

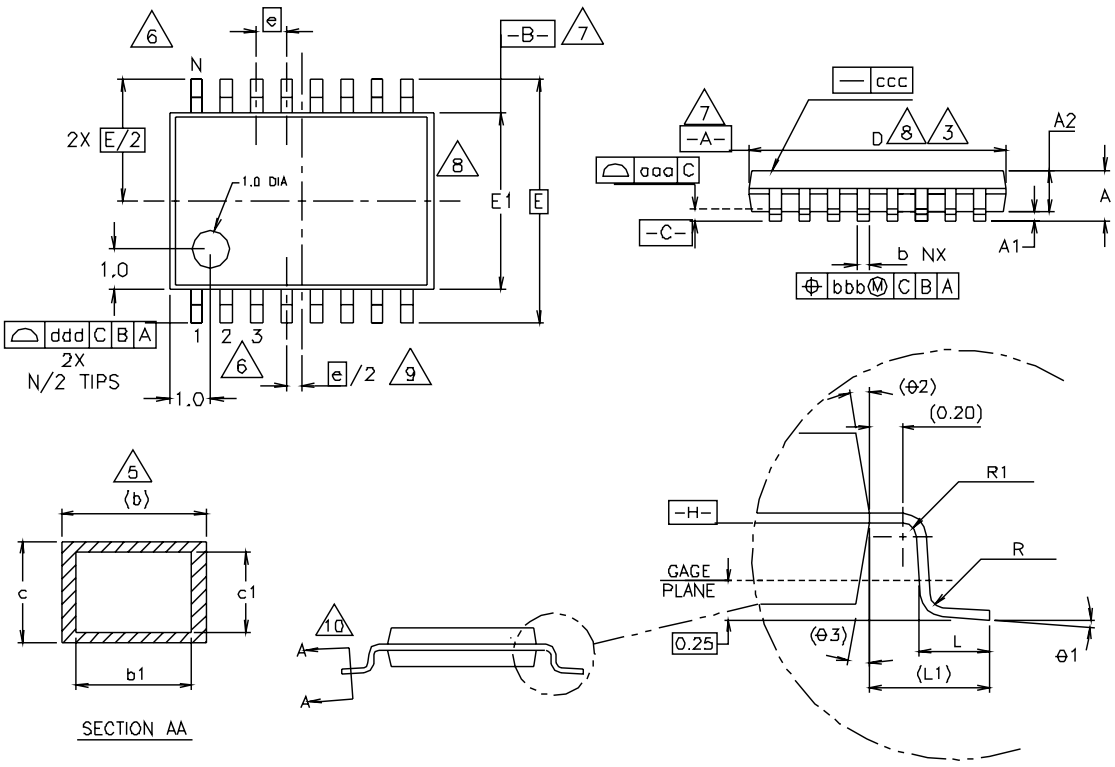
For optimum performance, care should be taken with the physical layout of the AS1539/AS1541 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

- Power to the AS1539/AS1541 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1 to 10µF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.
- The AS1539/AS1541 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results.
- While high-frequency noise can be filtered out, voltage variation due to line frequency (50 or 60Hz) can be difficult to remove.
- The GND pin should be connected to a clean ground point. In many cases, this will be the analog ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor.
- The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

Note: For additional information download the evaluation board application note on our website.

10 Package Drawings and Markings

Figure 30. TSSOP-16 *Package*

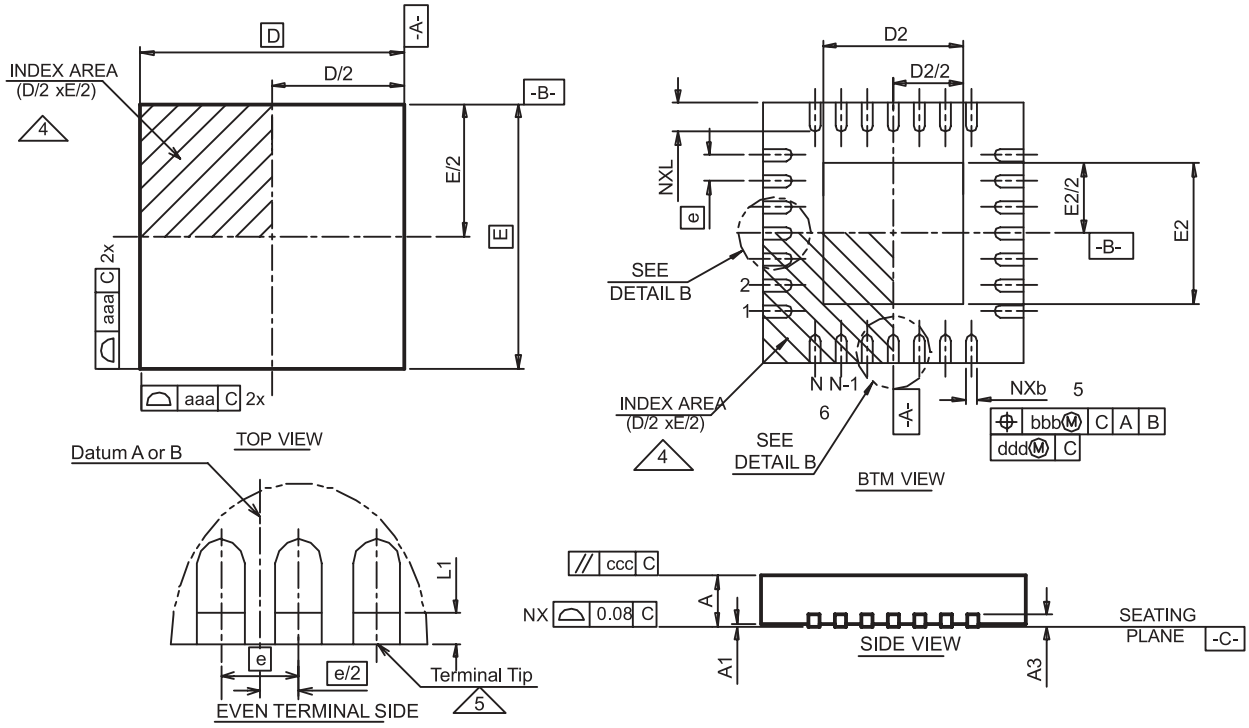


Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensioning and tolerancing per *ASME Y14.5M – 1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
6. Terminal numbers are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 are to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

Symbol	Min	Typ	Max	Notes
A	-	-	1.10	1,2
A1	0.05	-	0.15	1,2
A2	0.85	0.90	0.95	1,2
L	0.50	0.60	0.75	1,2
R	0.09	-	-	1,2
R1	0.09	-	-	1,2
b	0.19	-	0.30	1,2,5
b1	0.19	0.22	0.25	1,2
c	0.09	-	0.20	1,2
c1	0.09	-	0.16	1,2
θ1	0º	-	8º	1,2
L1	1.0REF			1,2
aaa	0.10			1,2
bbb	0.10			1,2
ccc	0.05			1,2
ddd	0.20			1,2
e	0.65BSC			1,2
θ2	12ºREF			1,2
θ3	12ºREF			1,2
Variations				
D	4.90	5.00	5.10	1,2,3,8
E1	4.30	4.40	4.50	1,2,4,8
E	6.4BSC			1,2
e	0.65BSC			1,2
N	16			1,2,6

Figure 31. TQFN 4x4 16-pin Package



Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
L	0.45	0.55	0.65	1, 2
L1	0.03		0.15	1, 2
K	0.20			1, 2
aaa		0.10		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		4.00		1, 2
E BSC		4.00		1, 2
D2	2.00	2.15	2.25	1, 2
E2	2.00	2.15	2.25	1, 2
b	0.25	0.30	0.35	1, 2, 5
e		0.65		
N		16		1, 2
ND		4		1, 2, 5

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminals.
4. Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the area indicated. The terminal #1 identifier may be either a mold, embedded metal or mark feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.
6. ND refers to the maximum number of terminals on D side.
7. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

11 Ordering Information

The device is available as the standard products shown in Table 7.

Table 7. Ordering Information

Model	Marking	Description	Delivery Form	Package
AS1539-BTST	AS1538	8-Channel, 10-Bit I²C Analog-to-Digital Converter	Tape and Reel	TSSOP-16
AS1539-BTSU	AS1538	8-Channel, 10-Bit I²C Analog-to-Digital Converter	Tubes	TSSOP-16
AS1541-BQFT	AS1540	4-Channel, 10-Bit I²C Analog-to-Digital Converter	Tape and Reel	TQFN 4x4 16-pin

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