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# AS1334

## 650mA, Ultra low Ripple Step Down DC/DC Converter



### 1 General Description

The AS1334 is a step-down DC-DC converter designed to power portable applications from a single Li-Ion battery. The device also achieves high-performance in mobile phones and other applications requiring low dropout voltage.

The AS1334 operates from an input voltage range of 2.7 to 5.5V while providing output voltages of 1.2, 1.5, 1.8, 2.5, 3.0 and 3.3V.

Fixed-frequency PWM operation minimizes RF interference. Shutdown function turns the device off and reduces battery consumption to 0.01µA (typ).

The AS1334 is available in a TDFN(3x3) 8-pin package. A high switching frequency (2 MHz) allows use of tiny surface-mount components. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

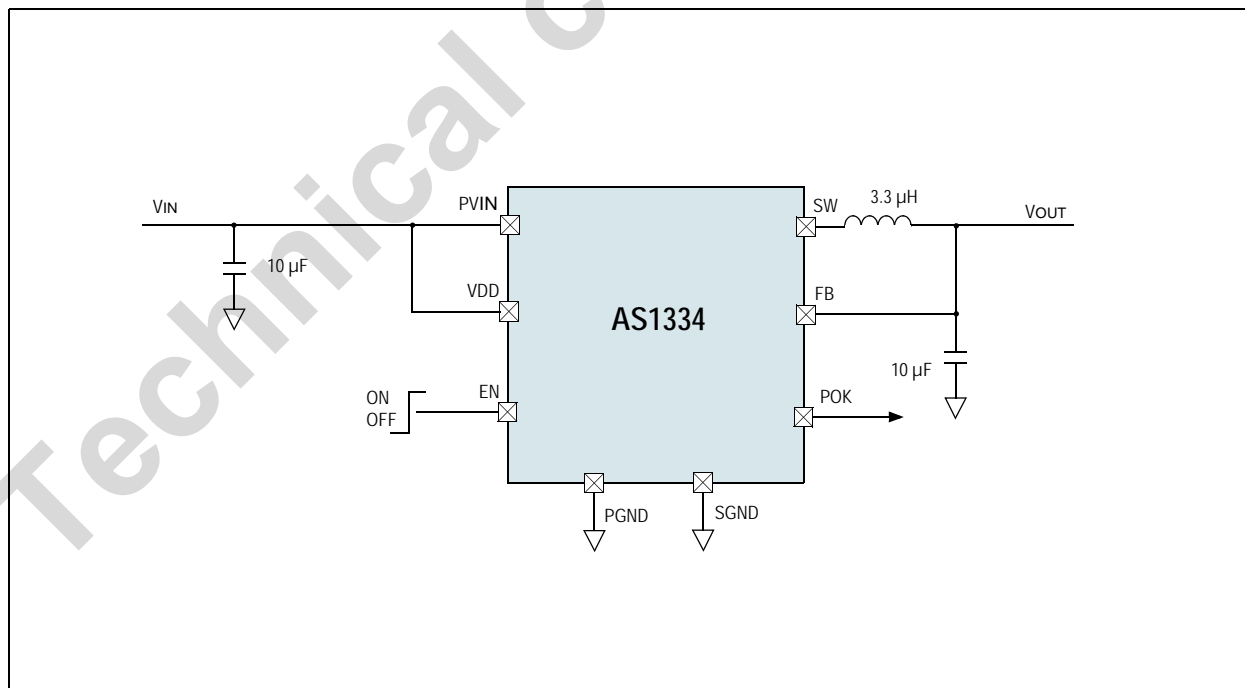
### 2 Key Features

- Output Voltage Ripple: 2mV
- PWM Switching Frequency: 2MHz
- Single Lithium-Ion Cell Operation
- Output Voltage Range: 1.2V to 3.4V (available in 100mV steps, see [Ordering Information on page 17](#))
- Fixed Output Voltages: - 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V
- Maximum Load Capability of 650mA
- 97% High Efficiency, 94% Average Efficiency
- Current Overload Protection
- Thermal Overload Protection
- Power-OK
- Soft Start
- Low Dropout Voltage (140 mΩ Typ PFET)
- TDFN(3x3) 8-pin

### 3 Applications

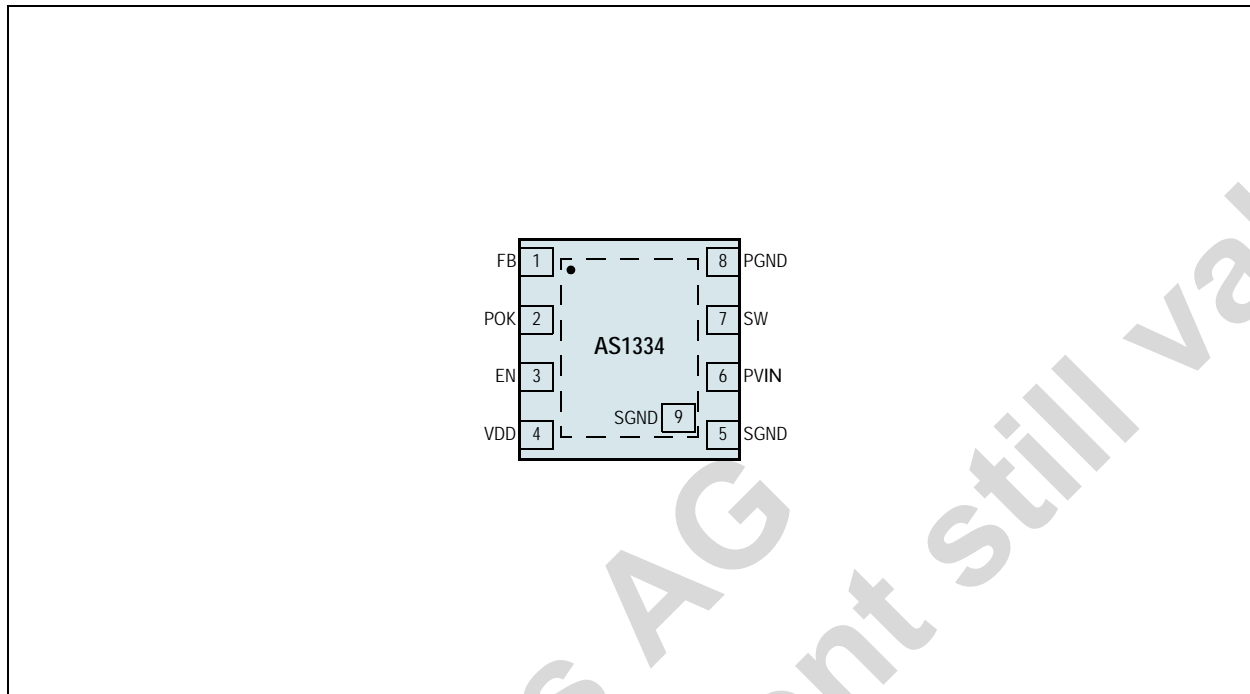
The AS1334 is an ideal solution to supply noise sensitive applications as cellular phones, hand-held radios, RF PC cards, battery powered RF devices, RFID chipsets, A/D Converter, Sensors and OpAmps.

Figure 1. AS1334 - Typical Application Circuit



## 4 Pin Assignments

Figure 2. Pin Configuration



### 4.1 Pin Descriptions

Table 1. Pin Descriptions

| Pin Number | Pin Name | Description  |
|------------|----------|--|
| 1          | FB       | Feedback Pin. Connect to the output at the output filter capacitor.  |
| 2          | POK      | Power-OK.<br>0 = $V_{OUT} < 90\%$ of $V_{OUTNOM}$ .<br>1 = $V_{OUT} > 90\%$ of $V_{OUTNOM}$ .  |
| 3          | EN       | Enable Input. Set this digital input high for normal operation. For shutdown, set low.   |
| 4          | VDD      | +2.7V to +5.5V Power Supply Voltage. Analog Supply Input.  |
| 5, 9       | SGND     | Analog and Control Ground. Connect these pins with low resistance to PGND.   |
| 6          | PVIN     | +2.7V to +5.5V Power Supply Voltage. Input to the internal PFET switch.  |
| 7          | SW       | Switch Pin. Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum switch peak current limit specification of the AS1334. |
| 8          | PGND     | Power Ground. Connect this pin with low resistance to SGND.  |

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter  | Min        | Max        | Units | Notes  |
|--|------------|------------|-------|--|
| <b>Electrical Parameters</b>                     |            |            |       |  |
| VDD, PVIN to SGND                                | -0.3       | +7.0       | V     |  |
| PGND to SGND                                     | -0.3       | +0.3       | V     |  |
| POK, EN, FB                                      | SGND - 0.3 | VDD + 0.3  | V     | 7.0V max   |
| SW   | PGND - 0.3 | PVIN + 0.3 | V     |  |
| PVIN to VDD                                      | -0.3       | +0.3       | V     |  |
| Input Voltage Range                              | 2.7        | 5.5        | V     |  |
| Recommended Load Current                         |            | 650        | mA    |  |
| Ambient Temperature (T <sub>A</sub> ) Range      | -40        | +85        | °C    | In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated.<br>Maximum ambient temperature (T <sub>A-MAX</sub> ) is dependent on the maximum operating junction temperature (T <sub>J-MAX-OP</sub> = 125°C), the maximum power dissipation of the device in the application (P <sub>D-MAX</sub> ), and the junction-to ambient thermal resistance of the part/package in the application (θ <sub>JA</sub> ), as given by the following equation: T <sub>A-MAX</sub> = T <sub>J-MAX-OP</sub> - (θ <sub>JA</sub> × P <sub>D-MAX</sub> ). |
| <b>Electrostatic Discharge</b>                   |            |            |       |  |
| Human Body Model                                 |            | 2          | kV    | Norm: MIL 883 E method 3015  |
| <b>Temperature Ranges and Storage Conditions</b> |            |            |       |  |
| Junction Temperature (T <sub>J-MAX</sub> )       |            | +150       | °C    |  |
| Storage Temperature Range                        | -55        | +150       | °C    |  |
| Package Body Temperature                         |            | +260       | °C    | The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> .<br>The lead finish for Pb-free leaded packages is matte tin (100% Sn).   |
| Humidity   | 5          | 86         | %     | Non-condensing   |
| Moisture Sensitive Level                         | 1          |            |       | Represents a max. floor life time of unlimited   |

## 6 Electrical Characteristics

$T_A = T_J = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $PV_{IN} = V_{DD} = EN = 3.6\text{V}$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ .

Table 3. Electrical Characteristics

| Symbol              | Parameter                       | Conditions   | Min   | Typ  | Max   | Units              |
|---------------------|---------------------------------|--|-------|------|-------|--------------------|
| $T_A$               | Operating Temperature Range     |  | -40   |      | +85   | $^{\circ}\text{C}$ |
| $V_{OUT}$           | Output Voltage                  | $PV_{IN} = 3.6\text{V}$                                | 1.176 | 1.2  | 1.224 | V                  |
|                     |                                 |  | 1.47  | 1.5  | 1.53  | V                  |
|                     |                                 |  | 1.764 | 1.8  | 1.836 | V                  |
|                     |                                 |  | 2.45  | 2.5  | 2.55  | V                  |
|                     |                                 |  | 2.94  | 3.0  | 3.06  | V                  |
|                     |                                 |  | 3.234 | 3.3  | 3.366 | V                  |
| $I_{SHDN}$          | Shutdown supply current         | $EN = SW = 0\text{V}^1$                                |       | 0.01 | 2     | $\mu\text{A}$      |
| $I_Q$               | DC bias current into VDD        | $FB = 0\text{V}$ , No Switching <sup>2</sup>           |       | 1    | 1.4   | mA                 |
| $R_{DS(on)(P)}$     | Pin-Pin Resistance for PFET     | $I_{SW} = 200\text{mA}$ ; $T_A = +25^{\circ}\text{C}$  |       | 140  | 200   | m $\Omega$         |
|                     |                                 | $I_{SW} = 200\text{mA}$                                |       |      | 230   |                    |
| $R_{DS(on)(N)}$     | Pin-Pin Resistance for NFET     | $I_{SW} = -200\text{mA}$ ; $T_A = +25^{\circ}\text{C}$ |       | 300  | 415   | m $\Omega$         |
|                     |                                 | $I_{SW} = -200\text{mA}$                               |       |      | 485   |                    |
| $I_{LIM,PFET}$      | Switch peak current limit       |  | 935   | 1100 | 1200  | mA                 |
| <b>POK Output</b>   |                                 |  |       |      |       |                    |
| $V_{OL}$            | POK Output Low Voltage          | POK sinking 0.1mA                                      |       | 0.05 | 0.2   | V                  |
|                     | POK Output High Leakage Current | POK = 3.6V   |       |      | 500   | nA                 |
|                     | POK Threshold                   | Falling edge, referenced to $V_{OUT(NOM)}$             | 87    | 90   | 93    | %                  |
| <b>Enable Input</b> |                                 |  |       |      |       |                    |
| $V_{IH,EN}$         | Logic high input threshold      |  | 1.2   |      |       | V                  |
| $V_{IL,EN}$         | Logic low input threshold       |  |       |      | 0.5   | V                  |
| $I_{PIN,ENABLE}$    | Pin pull down current           |  |       | 5    | 10    | $\mu\text{A}$      |
| <b>Oscillator</b>   |                                 |  |       |      |       |                    |
| $F_{OSC}$           | Internal oscillator frequency   |  | 1.8   | 2    | 2.2   | MHz                |

1. Shutdown current includes leakage current of PFET.
2.  $I_Q$  specified here is when the part is operating at 100% duty cycle.

## 6.1 System Characteristics

$T_A = 25^\circ\text{C}$ ;  $P_{VIN} = V_{DD} = EN = 3.6\text{V}$ , unless otherwise noted. The following parameters are verified by characterisation and are not production tested.

Table 4. System Characteristics

| Symbol            | Parameter   | Conditions   | Min | Typ | Max | Units         |
|-------------------|---|--|-----|-----|-----|---------------|
| $T_{ON}$          | Turn on time (from Enable low to high transition)                         | $EN = \text{Low to High}$ , $V_{IN} = 4.2\text{V}$ , $C_{OUT} = 10\mu\text{F}$ , $I_{OUT} \leq 1\text{mA}$   |     | 210 | 350 | $\mu\text{s}$ |
| $\eta$            | Efficiency ( $L = 3.3\mu\text{H}$ , $\text{DCR} \leq 100\text{m}\Omega$ ) | $V_{IN} = 3.6\text{V}$ , $I_{OUT} = 400\text{mA}$  |     | 96  |     | %             |
| $V_{OUT\_ripple}$ | Ripple voltage, PWM mode <sup>1</sup>                                     | $V_{IN} = 4.2\text{V}$ , $I_{OUT} = 10\text{mA to } 400\text{mA}$  |     | 5   |     | mVp-p         |
| Line_tr           | Line transient response   | $V_{IN} = 600\text{mV}$ perturbation, over $V_{IN}$ range 3.4V to 5.5V; $T_{RISE} = T_{FALL} = 10\mu\text{s}$ , $V_{OUT} = 3.0\text{V}$ , $I_{OUT} = 100\text{mA}$ |     | 50  |     | mVpk          |
| Load_tr           | Load transient response   | $V_{IN} = 4.2\text{V}$ , $V_{OUT} = 3.0\text{V}$ , transients up to 100mA, $T_{RISE} = T_{FALL} = 10\mu\text{s}$   |     | 50  |     | mVpk          |

1. Ripple voltage should be measured at  $C_{OUT}$  electrode on good layout PC board and under condition using suggested inductors and capacitors.

**Note:** All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

## 7 Typical Operating Characteristics

Circuit in Figure 23 on page 11,  $PV_{IN} = V_{DD} = EN = 3.6V$ ,  $L = 3.3\mu H$  (LPS4018-332ML<sub>-</sub>),  $C_{IN} = C_{OUT} = 10\mu F$  (GRM21BR61C106KA01) unless otherwise noted.

Figure 3. Quiescent Current vs.  $V_{IN}$

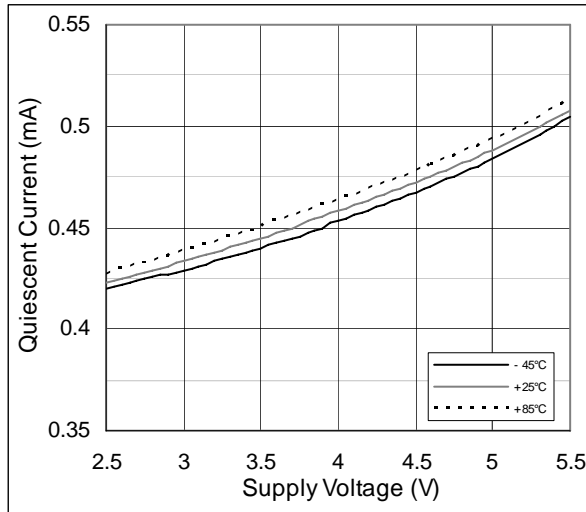


Figure 4. Shutdown Current vs. Temperature

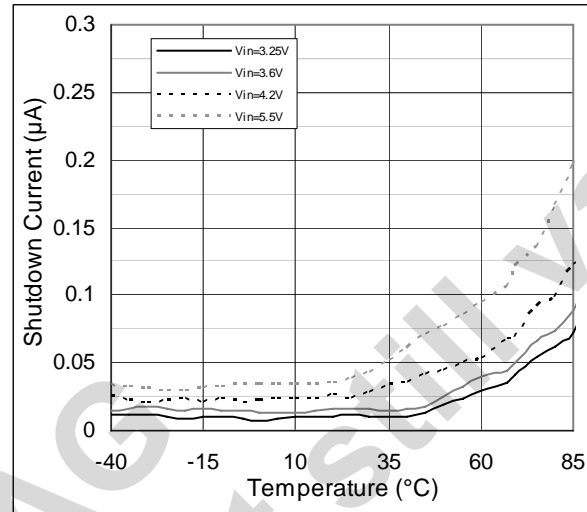


Figure 5. Switching Frequency Variation vs. Temperature

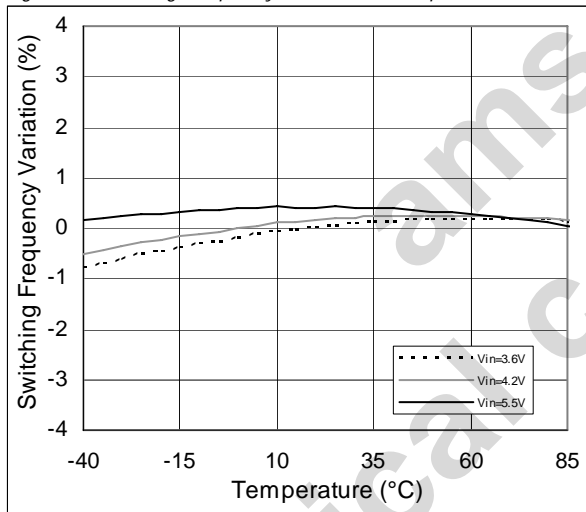


Figure 6. Output Voltage vs. Supply Voltage

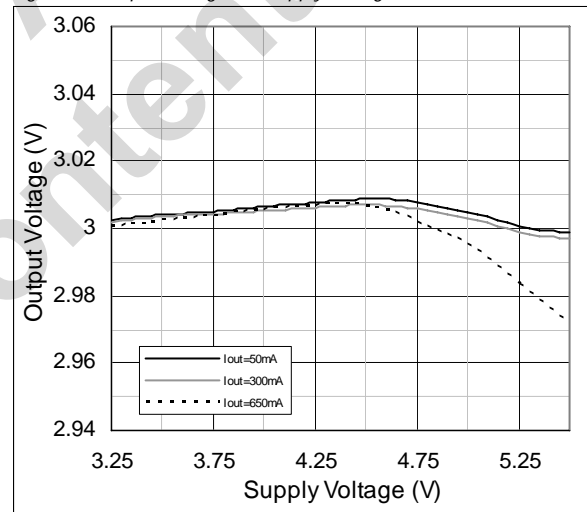


Figure 7. Output Voltage vs. Temperature

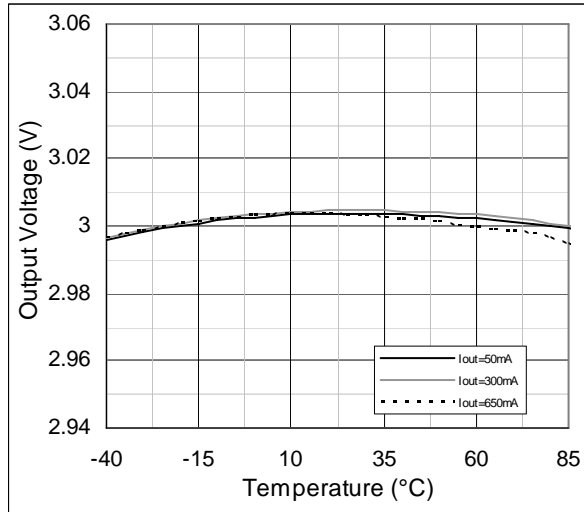


Figure 8. Efficiency vs. Output Current

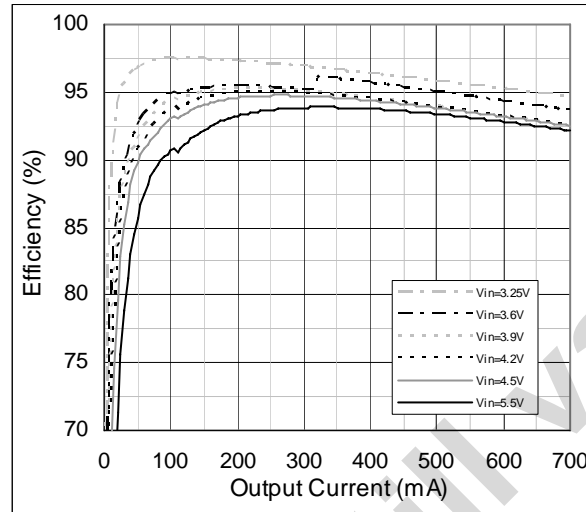


Figure 9. Switch Peak Current Limit vs. Temperature; closed loop

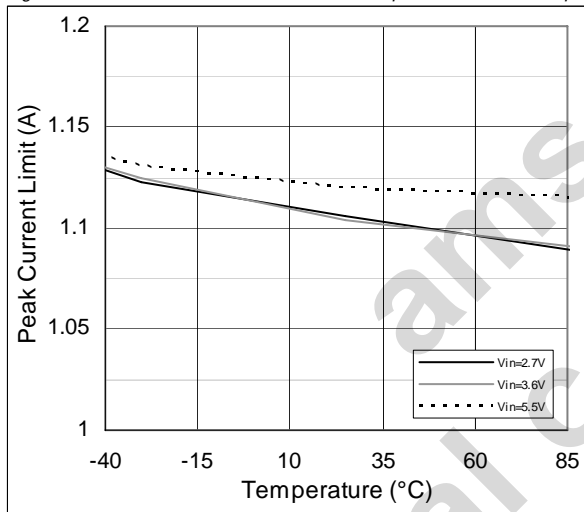


Figure 10. Load Transient Response; V<sub>OUT</sub> = 3.0V, V<sub>IN</sub> = 4.2V

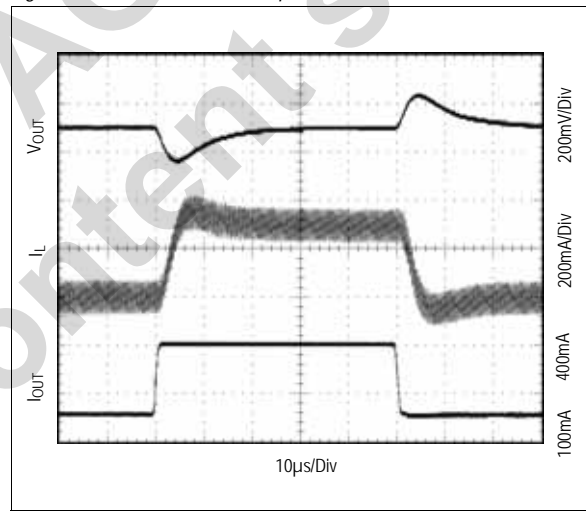


Figure 11. Startup; V<sub>IN</sub> = 3.6V, V<sub>OUT</sub> = 3.0V, I<sub>OUT</sub> < 1mA, R<sub>LOAD</sub> = 3.3kΩ

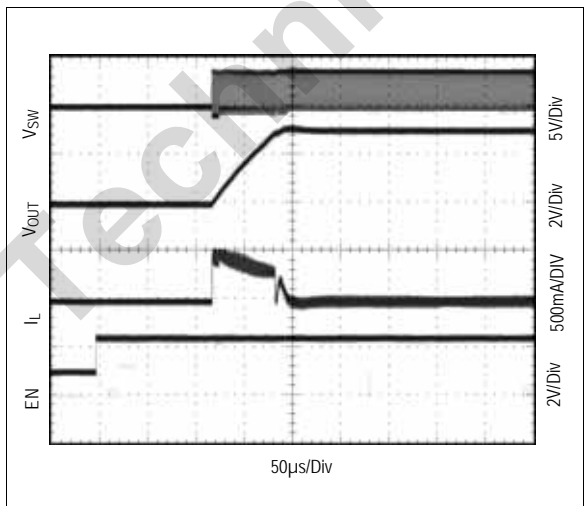


Figure 12. Startup; V<sub>IN</sub> = 4.2V, V<sub>OUT</sub> = 3.0V, I<sub>OUT</sub> < 1mA, R<sub>LOAD</sub> = 3.3kΩ

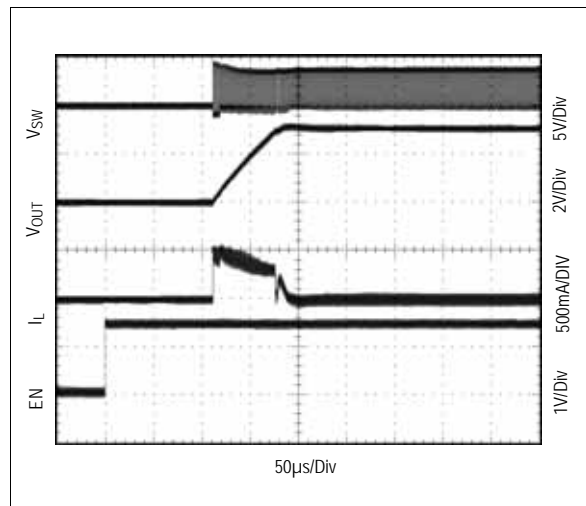




Figure 13. Shutdown Response;  $V_{IN}=3.6V$ ,  $V_{OUT}=3.0V$ ,  
 $R_{LOAD}=5\Omega$

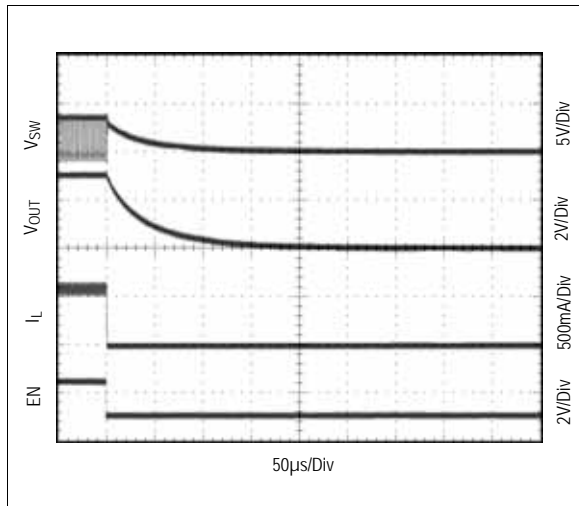


Figure 14. Shutdown Response;  $V_{IN}=4.2V$ ,  $V_{OUT}=3.0V$ ,  
 $R_{LOAD}=5\Omega$

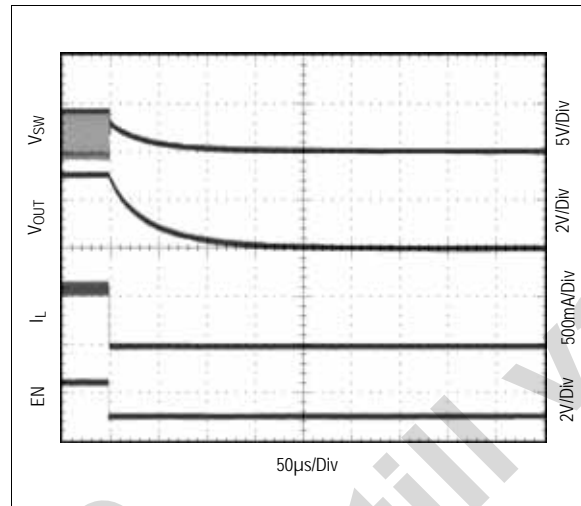


Figure 15. Line Transient Response;  $V_{IN}=3.3V$  to  $3.9V$ ,  
 $I_{OUT}=100mA$ ,  $V_{OUT}=3.0V$



Figure 16. Timed Current Limit Response;  $V_{IN}=3.6V$ ,  $V_{OUT}=3.0V$

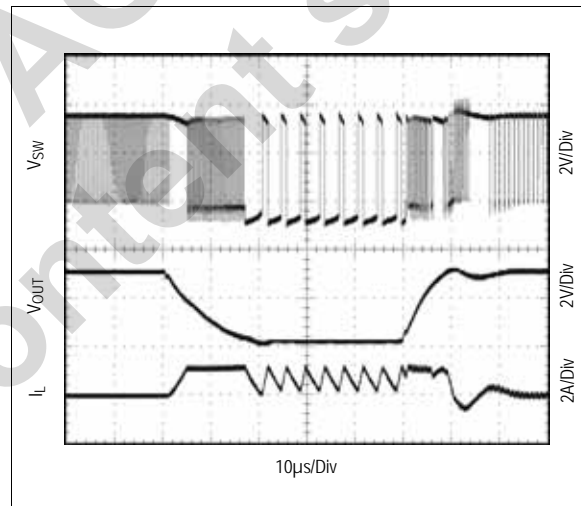


Figure 17. Output Voltage Ripple;  $V_{OUT} = 3.0V$ ,  $I_{OUT} = 200mA$

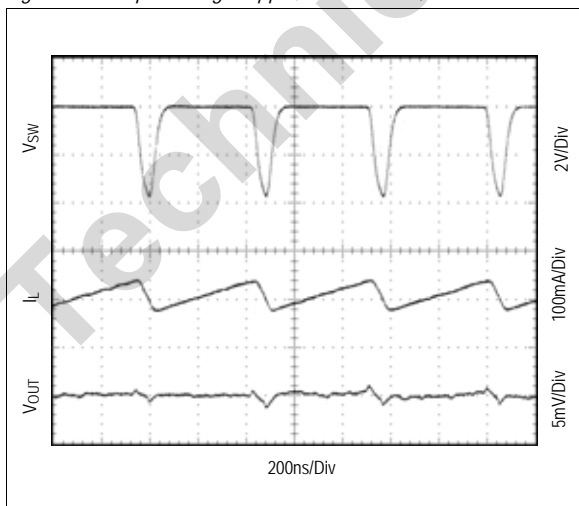


Figure 18.  $V_{OUT}$  Ripple in Skip Mode;  $V_{IN}=3.31V$ ,  $V_{OUT}=3.0V$ ,  
 $R_{LOAD}=5\Omega$

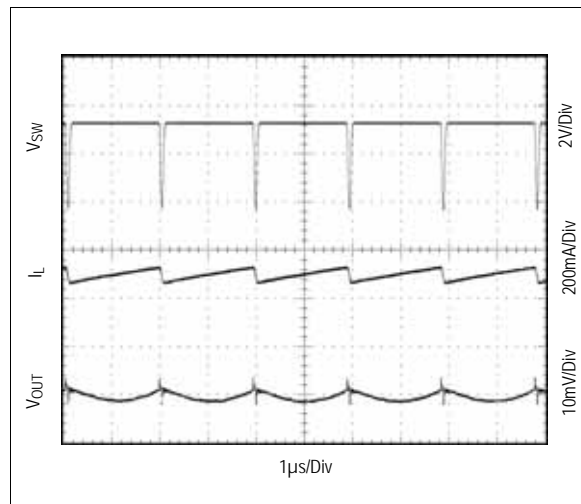


Figure 19.  $R_{DS(on)}$  (P-Channel) vs. Temp.;  $I_{sw}=200mA$

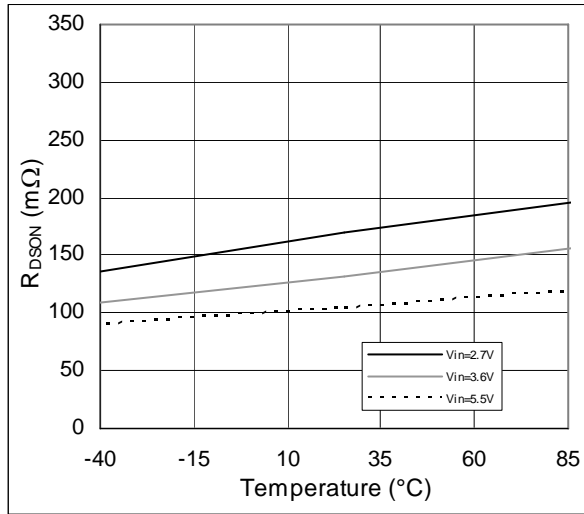


Figure 20.  $R_{DS(on)}$  (N-Channel) vs. Temp.;  $I_{sw}=-200mA$

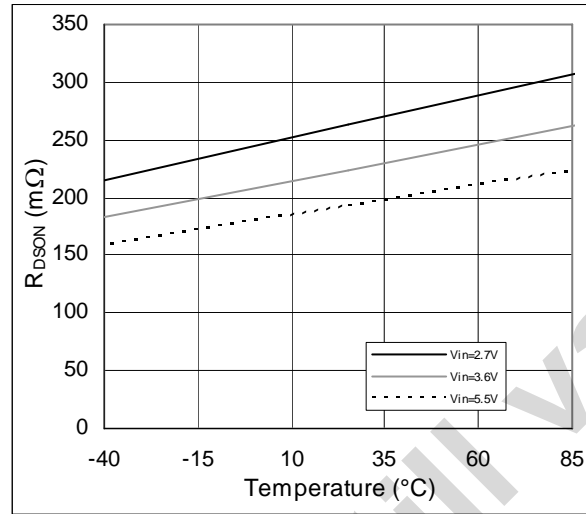
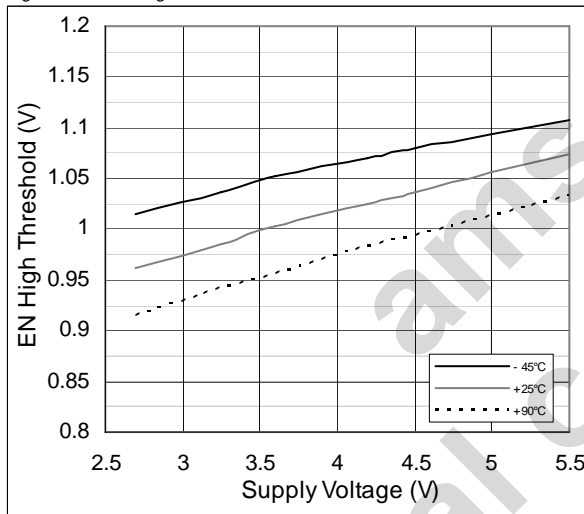


Figure 21. EN High Threshold vs.  $V_{in}$

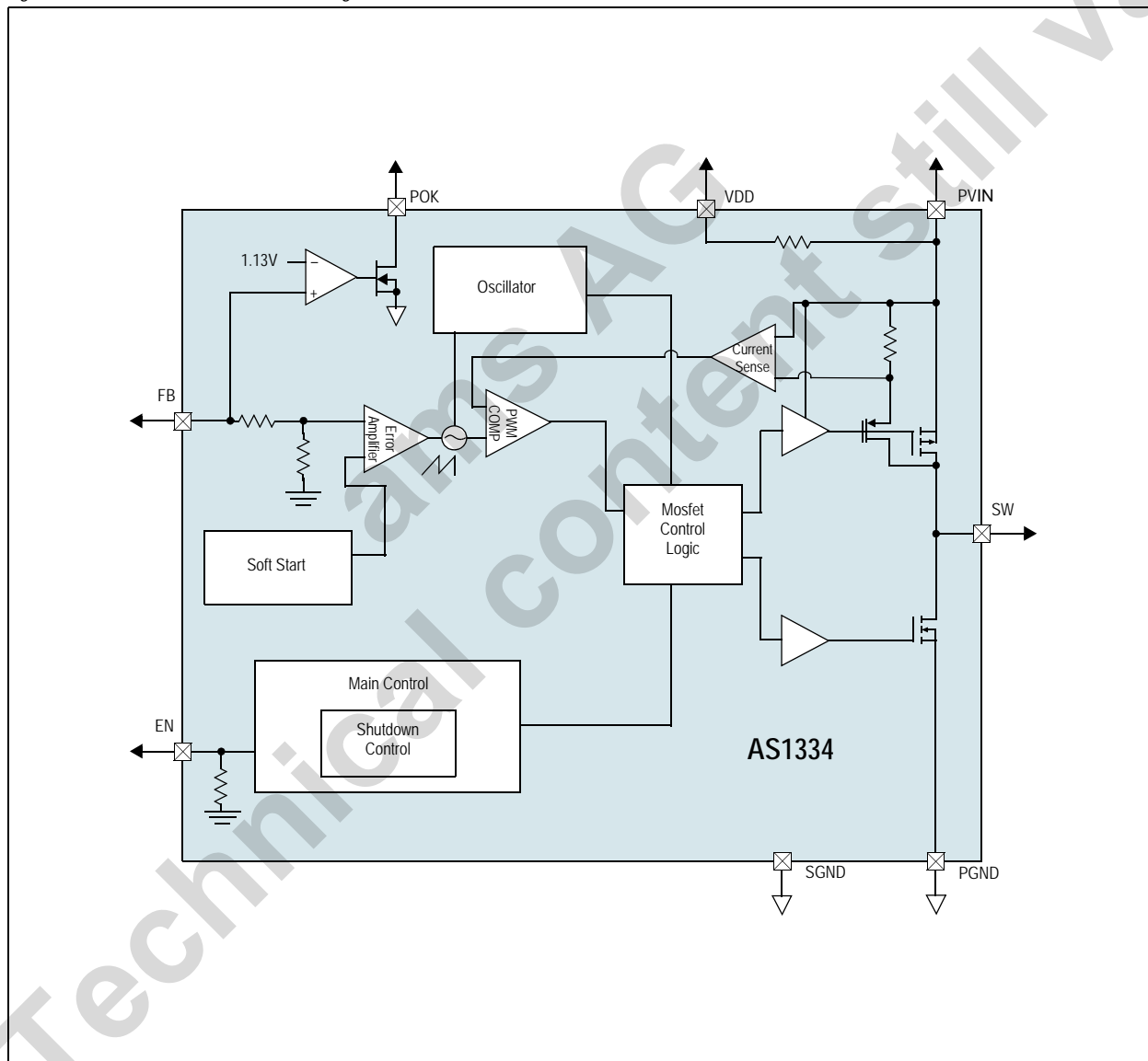


## 8 Detailed Description

The AS1334 is a simple, step-down DC-DC converter optimized for powering portable applications that require low dropout voltages such as mobile phones, portable communicators, and similar battery powered RFID devices. Besides being packed with numerous features like current overload protection, thermal overload shutdown and soft start, AS1334 displays the following characteristics:

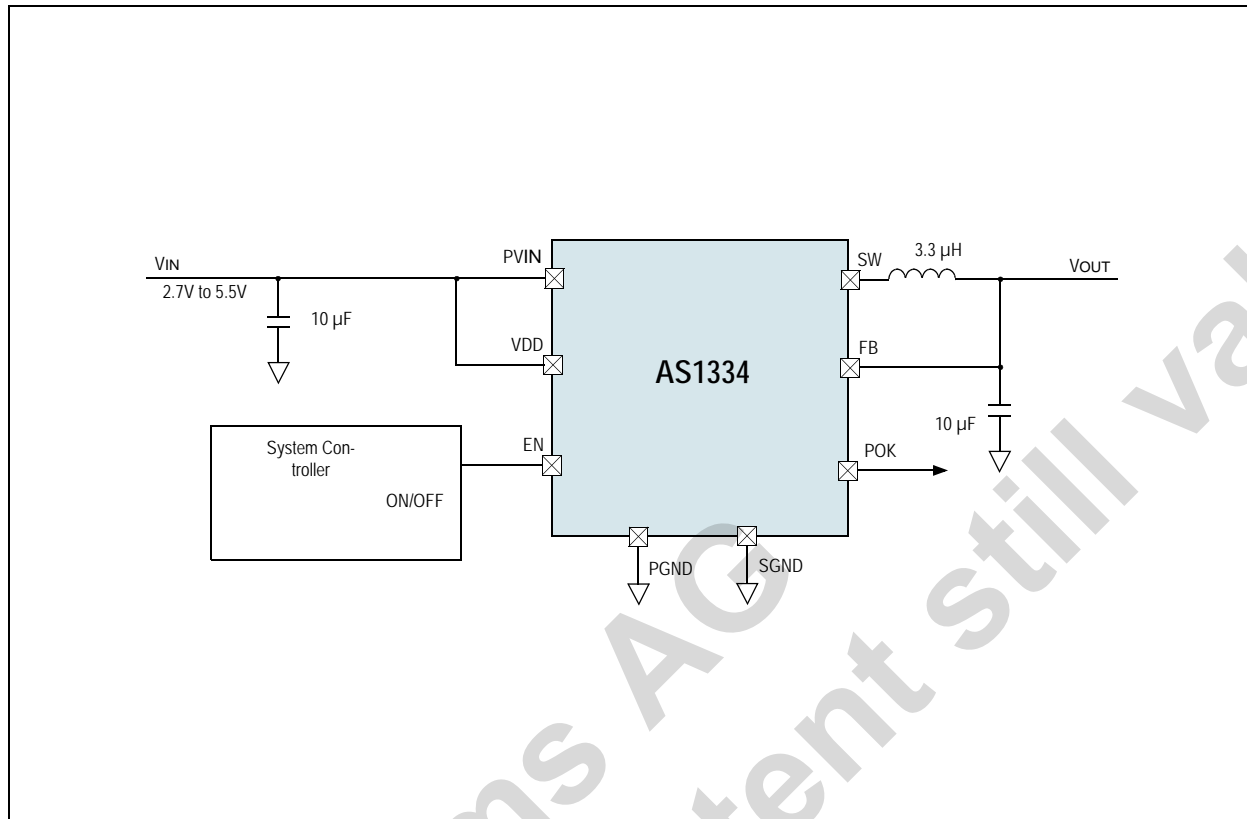
- Its operation is based on current-mode buck architecture with synchronous rectification for high efficiency.
- Allows the application to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell.
- Provides for a maximum load capability of 650mA in PWM mode, wherein the maximum load range may vary depending on input voltage, output voltage and the selected inductor.
- Is ranked at an efficiency of around 96% for a 400mA load with a 3.6V input voltage.

Figure 22. AS1334 - Functional Block Diagram



The size of the external components is reduced by using a high switching frequency (2MHz). [Figure 1 on page 1](#) demonstrates that only three external power components are required for implementation. Also, the system controller should set EN low during power-up and other low supply voltage conditions. [See Shutdown Mode on page 12](#).

Figure 23. Typical Operating System Circuit



## 8.1 Operating the AS1334

AS1334's control block turns on the internal PFET (P-channel MOSFET) switch during the first part of each switching cycle, thus allowing current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around  $(V_{IN} - V_{OUT}) / L$ , by storing energy in a magnetic field.

During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. As a result, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load.

While the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around  $V_{OUT} / L$ . The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor.

The output voltage is equal to the average voltage at the SW pin.

While in operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle.

If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load. Before appearing at the PWM comparator, a slope compensation ramp from the oscillator is subtracted from the error signal for stability of the current feedback loop. The minimum on time of PFET in PWM mode is 50ns (typ).

## 8.2 Internal Synchronous Rectifier

To reduce the rectifier forward voltage drop and the associated power loss, the AS1334 uses an internal NFET as a synchronous rectifier. The big advantage of a synchronous rectification is the higher efficiency in a condition where the output voltage is low compared to the voltage drop across an ordinary rectifier diode. During the inductor current down slope in the second part of each cycle the synchronous rectifier is turned on. Before the next cycle the synchronous rectifier is turned off.

There is no need for an external diode because the NFET is conducting through its intrinsic body diode during the transient intervals before it turns on.

## 8.3 Power-OK

The POK output indicates if the output voltage is within 90% of the nominal voltage level. As long as the output voltage is within regulation the open-drain POK output sinks current.

## 8.4 Shutdown Mode

If EN is set to high (>1.2V) the AS1334 is in normal operation mode. During power-up and when the power supply is less than 2.7V minimum operating voltage, the chip should be turned off by setting EN low. In shutdown mode the following blocks of the AS1334 are turned off, PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry. The AS1334 is designed for compact portable applications, such as mobile phones where the system controller controls operation mode for maximizing battery life and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

**Note:** Setting the EN digital pin low (<0.5V) places the AS1334 in a 0.01 $\mu$ A (typ) shutdown mode.

## 8.5 Thermal Overload Protection

To prevent the AS1334 from short-term misuse and overload conditions the chip includes a thermal overload protection. To block the normal operation mode the device is turning the PFET and the NFET off in PWM mode as soon as the junction temperature exceeds 150°C. To resume normal operation the temperature has to drop below 140°C.

**Note:** Continuing operation in thermal overload conditions may damage the device and is considered bad practice.

## 8.6 Current Limiting For Protection

If in the PWM mode the cycle-by-cycle current limit of 1200mA (max.) is reached the current limit feature takes place and protects the device and the external components. A timed current limiting mode is working when a load pulls the output voltage down to approximately 0.375V. In this timed current limit mode the inductor current is forced to ramp down to a safe value. This is achieved by turning off the internal PFET switch and delaying the start of the next cycle for 3.5 $\mu$ s. The synchronous rectifier is also turned off in the timed current limit mode.

The advantage of the timed current limit mode is to prevent the device from the loss of the current control.

## 9 Application Information

### 9.1 Inductor Selection

For the external inductor, a 3.3 $\mu$ H inductor is recommended. Minimum inductor size is dependant on the desired efficiency and output current. Inductors with low core losses and small DCR at 2MHz are recommended.

Table 5. Recommended Inductor

| Part Number    | L           | DCR            | Current Rating | Dimensions (L/W/T) | Manufacturer  |
|----------------|-------------|----------------|----------------|--------------------|---|
| LPS4018-222ML_ | 2.2 $\mu$ H | 0.070 $\Omega$ | 2.9A           | 3.9x3.9x1.7mm      | Coilcraft<br><a href="http://www.coilcraft.com">www.coilcraft.com</a> |
| LPS4018-332ML_ | 3.3 $\mu$ H | 0.080 $\Omega$ | 2.4A           | 3.9x3.9x1.7mm      |   |
| LPS4018-472ML_ | 4.7 $\mu$ H | 0.125 $\Omega$ | 1.9A           | 3.9x3.9x1.7mm      |   |

### 9.2 Capacitor Selection

A 10 $\mu$ F capacitor is recommended for C<sub>IN</sub> as well as a 10 $\mu$ F for C<sub>OUT</sub>. Small-sized X5R or X7R ceramic capacitors are recommended as they retain capacitance over wide ranges of voltages and temperatures.

#### 9.2.1 Input and Output Capacitor Selection

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Also low ESR capacitors should be used to minimize V<sub>OUT</sub> ripple. Multi-layer ceramic capacitors are recommended since they have extremely low ESR and are available in small footprints.

For input decoupling the ceramic capacitor should be located as close to the device as practical. A 4.7 $\mu$ F input capacitor is sufficient for most applications. Larger values may be used without limitations.

A 2.2 $\mu$ F to 10 $\mu$ F output ceramic capacitor is sufficient for most applications. Larger values up to 22 $\mu$ F may be used to obtain extremely low output voltage ripple and improve transient response.

Table 6. Recommended Input and Output Capacitor

| Part Number       | C           | TC Code | Rated Voltage | Dimensions (L/W/T) | Manufacturer   |
|-------------------|-------------|---------|---------------|--------------------|--|
| GRM188R60J475KE19 | 4.7 $\mu$ F | X5R     | 6.3V          | 0603               | Murata<br><a href="http://www.murata.com">www.murata.com</a> |
| GRM219R60J475KE19 | 4.7 $\mu$ F | X5R     | 6.3V          | 0805               |  |
| GRM21BR61C475KA88 | 4.7 $\mu$ F | X5R     | 16V           | 0805               |  |
| GRM31CR71E475KA88 | 4.7 $\mu$ F | X7R     | 25V           | 1206               |  |
| GRM188R60J106ME47 | 10 $\mu$ F  | X5R     | 6.3V          | 0603               |  |
| GRM21BR60J106KE19 | 10 $\mu$ F  | X5R     | 6.3V          | 0805               |  |
| GRM21BR61A106KE19 | 10 $\mu$ F  | X5R     | 10V           | 0805               |  |
| GRM32DR71C106KA01 | 10 $\mu$ F  | X7R     | 16V           | 1210               |  |
| GRM21BR60J226ME39 | 22 $\mu$ F  | X5R     | 6.3V          | 0805               |  |
| GRM32ER71A226KE20 | 22 $\mu$ F  | X7R     | 10V           | 1210               |  |

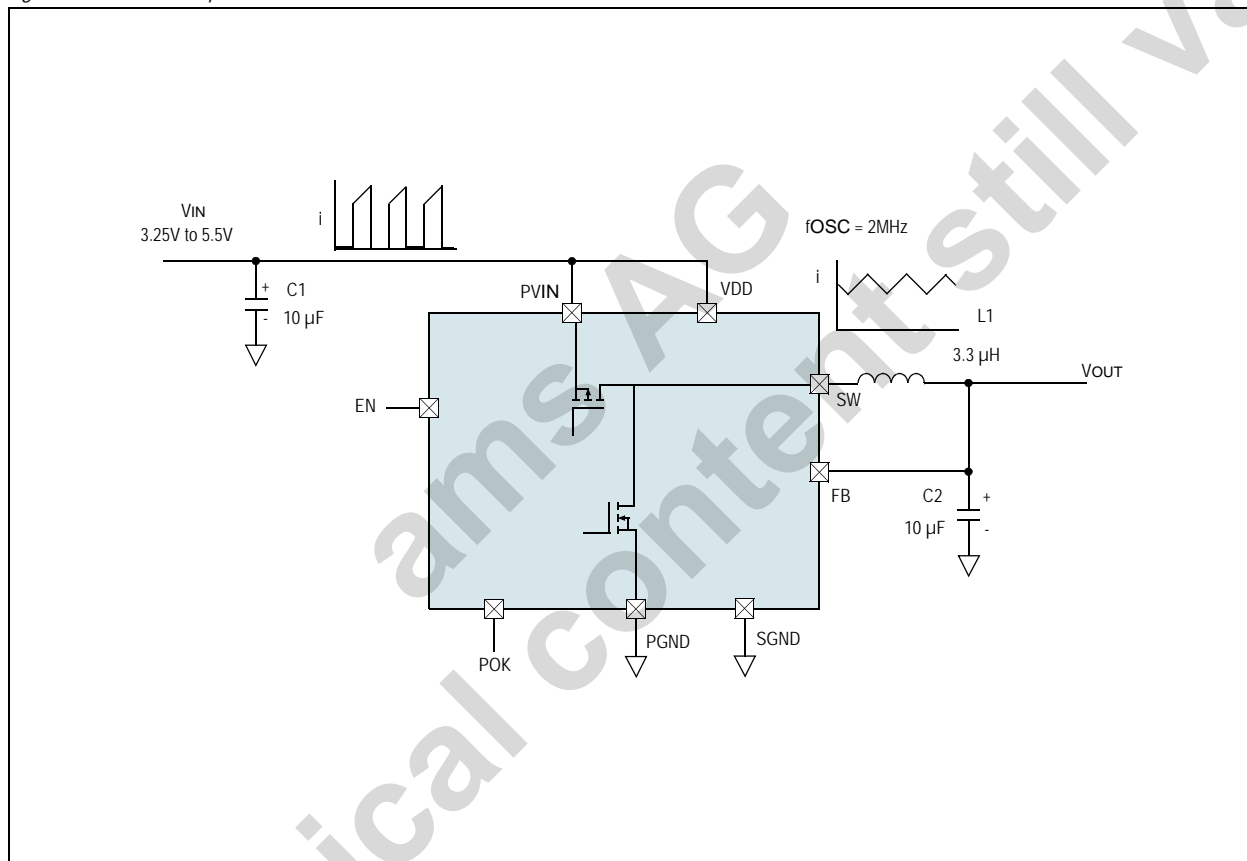
### 9.3 EN Pin Control

Drive the EN pin using the system controller to turn the AS1334 ON and OFF. Use a comparator, Schmidt trigger or logic gate to drive the EN pin. Set EN high (>1.2V) for normal operation and low (<0.5V) for a 0.01 $\mu$ A (typ) shutdown mode. Set EN low to turn off the AS1334 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The part is out of regulation when the input voltage is less than 2.7V.

## 9.4 Layout Considerations

The AS1334 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on, the input voltage is applied to the inductor, and the current flows from PVDD line to the output capacitor (C2) through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2). Referring to Figure 24, the AS1334 has two major current loops where pulse and ripple current flow. The loop shown in the left hand side is most important, because pulse current shown in Figure 24 flows in this path. The right hand side is next. The current waveform in this path is triangular, as shown in Figure 24. Pulse current has many high-frequency components due to fast di/dt. Triangular ripple current also has wide high-frequency components. Board layout and circuit pattern design of these two loops are the key factors for reducing noise radiation and stable operation. Other lines, such as from battery to C1(+) and C2(+) to load, are almost DC current, so it is not necessary to take so much care. Only pattern width (current capability) and DCR drop considerations are needed.

Figure 24. Current Loop



## 10 Package Drawings and Markings

Figure 25. TDFN(3x3) 8-pin Marking

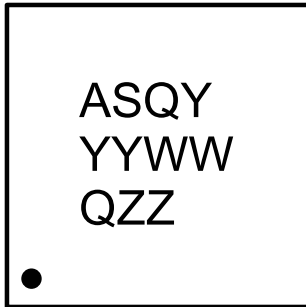
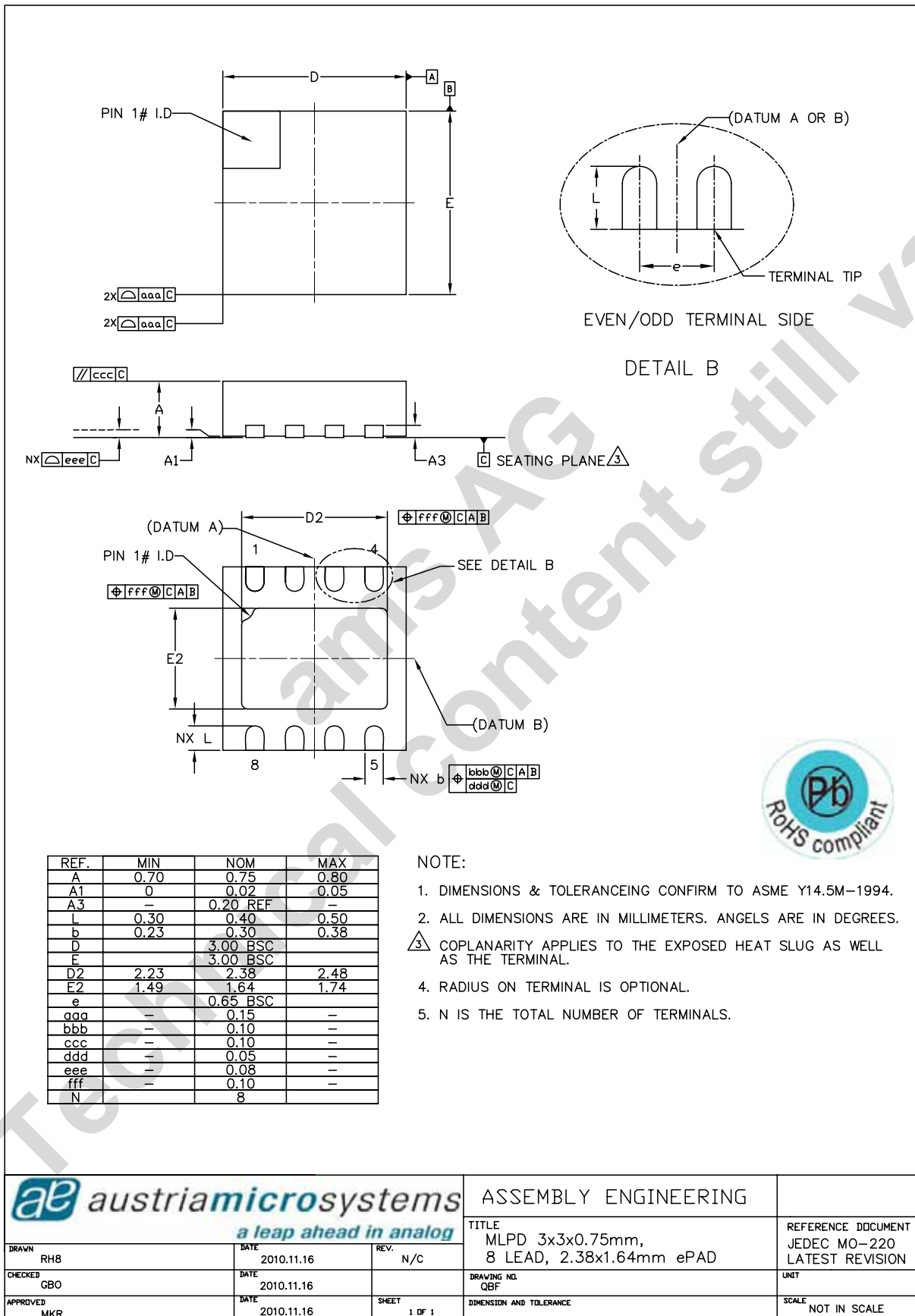


Table 7. Packaging Code YYWWQZZ

| YY              | WW                 | Q                | ZZ                              |
|-----------------|--------------------|------------------|---------------------------------|
| year identifier | manufacturing week | plant identifier | free choice / traceability code |



Figure 26. TDFN(3x3) 8-pin Package



## 11 Ordering Information

The device is available as the standard products shown in [Table 8](#).

Table 8. Ordering Information

| Ordering Code               | Marking | Output | Description                                       | Delivery Form | Package         |
|-----------------------------|---------|--------|---|---------------|-----------------|
| AS1334-BTDT-12              | ASR2    | 1.2V   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |
| AS1334-BTDT-15              | ASR3    | 1.5V   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |
| AS1334-BTDT-18              | ASR4    | 1.8V   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |
| AS1334-BTDT-25              | ASR5    | 2.5V   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |
| AS1334-BTDT-30              | ASQY    | 3.0V   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |
| AS1334-BTDT-33              | ASR6    | 3.3V   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |
| AS1334-BTDT-xx <sup>1</sup> | xxxx    | xxxx   | 650mA, Ultra low Ripple Step Down DC/DC Converter | Tape and Reel | TDFN(3x3) 8-pin |

1. Non-standard devices are available between 1.2V and 3.4V in 100mV steps. For more information and inquiries contact <http://www.austriamicrosystems.com/contact>

**Note:** All products are RoHS compliant.

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Design the AS1334 online at <http://www.austriamicrosystems.com/analogbench>

*analogbench* is a powerful design and simulation support tool that operates in on-line and off-line mode to evaluate performance and generate application-specific bill-of-materials for austriamicrosystems' power management devices.



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