AS1160/AS1161

20MHz - 66MHz, 10-Bit Bus, IEEE 1149.1 (JTAG) Compliant LVDS Serializer/Deserializer

1 General Description

The AS1160 (serializer) is designed to convert 10-bit wide parallel LVCMOS/LVTTL data bus signals into a single high-speed LVDS serial data stream with clock. The AS1161 (deserializer) transforms the high-speed LVDS serial data stream back into a 10-bit wide parallel data bus with recovered parallel clock.

Both devices are compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture (including the defined boundary-scan test logic and test access port consisting of Test Data Input, Test Data Out, and Test Mode Select, Test Clock, and Test Reset).

The devices also feature an at-speed BIST mode which allows the interconnects between the serializer and deserializer to be verified at-speed.

The single differential-pair data-path makes PCB design easier, and reduced cable/PCB-trace count and connector size significantly reduce cost. Since one output transmits clock and data bits serially, clock-to-data and data-to-data skew are eliminated.

Powerdown mode reduces supply current when both devices are idle.

Both devices are available in a CTBGA 49-bumps pin package.

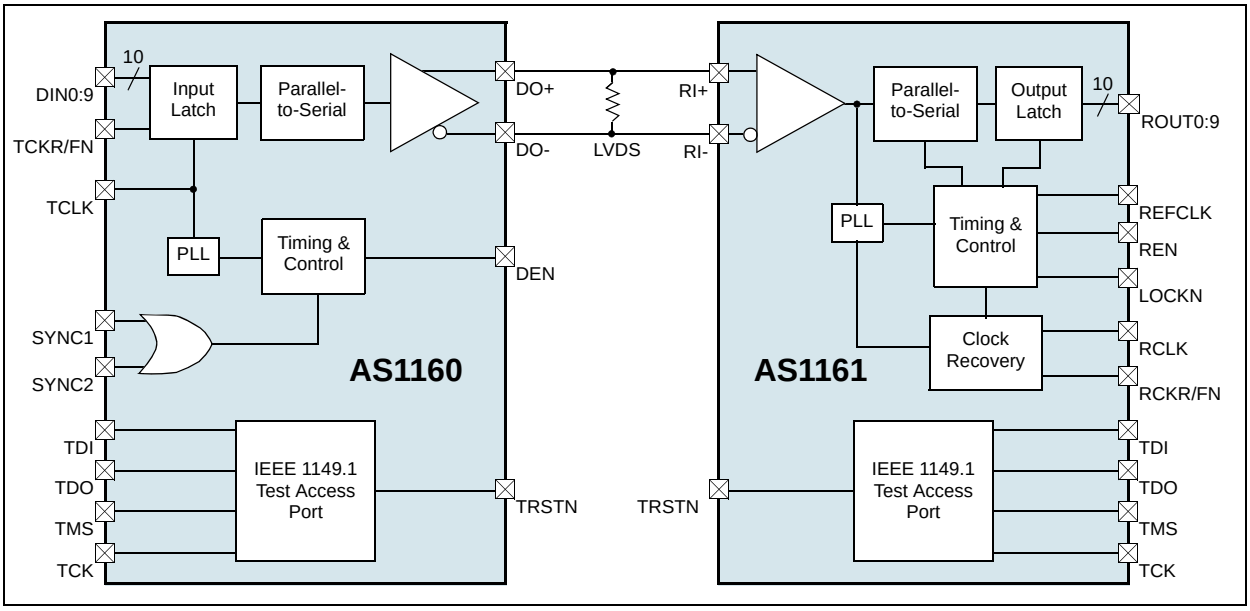
2 Key Features

- Serial Bus LVDS Data Rate: 660 Mbps @ 66MHz Clock
- 10-bit Parallel Interface
- Synchronization Mode and Lock Indicator
- Programmable Edge Trigger on Clock
- High Impedance on Rx Inputs during Poweroff
- Bus LVDS Serial Output Load: 28Ω
- IEEE 1149.1 (JTAG) Compliant and At-Speed BIST Test Mode
- Clock Recovery from PLL Lock to Random Data Patterns
- Guaranteed Transition each Data Transfer Cycle
- Chipset (Tx + Rx) Power Consumption: < 500 mW @ 66MHz
- Single Differential-Pair eliminates Multi-Channel Skew
- Flow-Through Pinout for Simple PCB Layout
- Small CTBGA 49-bumps Package

3 Applications

The devices are ideal for cellular phone base stations, add drop muxes, digital cross-connects. DSLAMs, networkswitches and routers or backplane interconnect.

Figure 1. Block Diagrams



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4 Pinout

Pin Assignments and Descriptions

Figure 2. AS1160 Pin Assignments (Top View)

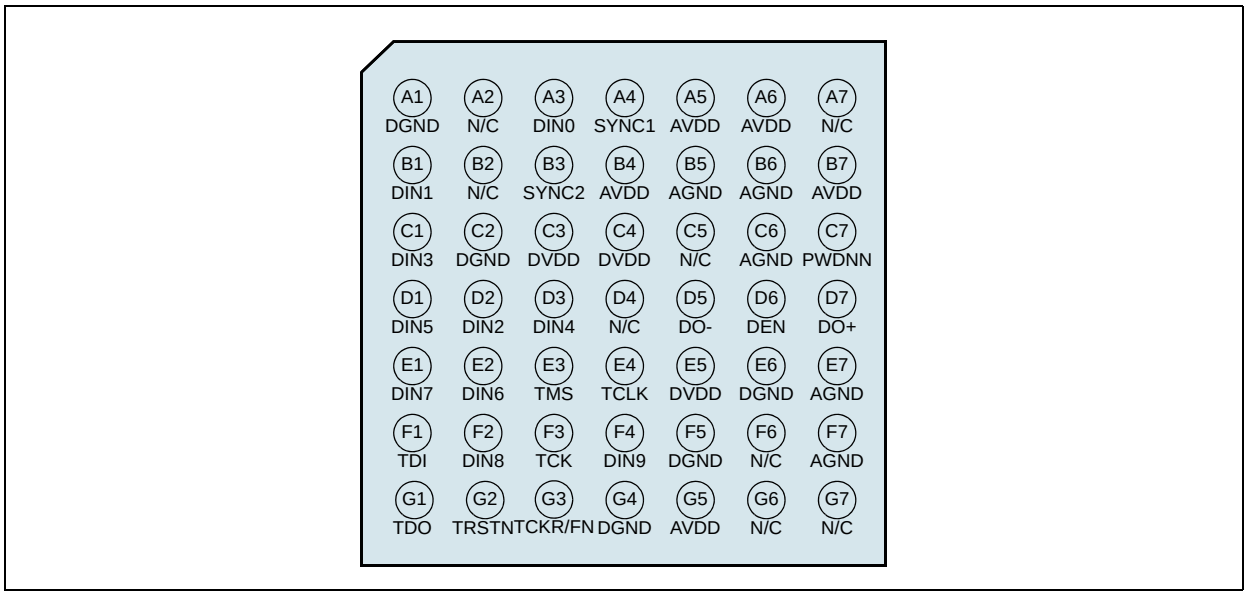


Table 1. AS1160 Pin Descriptions

Pin Number	Pin Name	Description
See Figure 2	DIN0:DIN9	**Data Input.** LVTTL levels inputs. Data on these pins are loaded into a 10-bit input register.
	TCKR/FN	**Transmit Clock Rising/Falling Strobe Select.** LVTTL level input. Selects TCLK active edge for strobing of DIN*x* data. 1 = Rising edge. 0 = Falling edge.
	DO+	**+ Serial Data Output**. Non-inverting Bus LVDS differential output.
	DO-	**- Serial Data Output**. Inverting Bus LVDS differential output.
	DEN	**Serial Data Output Enable.** LVTTL level input. If DEN is set to logic low the Bus LVDS outputs are in tri-state condition.
	PWDNN	**Powerdown.** LVTTL level input. Driving this pin low shuts down the PLL, tri-states the outputs and puts the device into low power sleep mode.
	TCLK	**Transmit Clock.** LVTTL level input. Input for 20MHz to 66MHz system clock.
	SYNC1, SYNC2	**Synchronization.** LVTTL level input. Assertion of SYNC (high) for at least 5 clock cycles to be transmit a synchronization signal (SYNCPAT) on the Bus LVDS serial output. Synchronization symbols continue to be sent if SYNC*x* continues to be asserted. SYNC1 and SYNC2 pins are combined through an OR gate.
	DVDD	**+3.0V to +3.6V Digital Circuit Power Supply.** This is the supply for all digital circuitry.
	DGND	**Digital Circuit Ground.** GND reference point for the digital part of the AS1160.
	AVDD	**+3.0V to +3.6V Analog Power Supply** (PLL and Analog Circuits)**.** AVDD and DVDD should be at the same potential and must not be more than 0.3V apart even on transient basis. Both supplys should be decoupled by a capacitor of typically 10nF.
	AGND	**Analog Ground** (PLL and Analog Circuits).
	TDI	**IEEE 1149.1 Test Data Input**
	TDO	**IEEE 1149.1 Test Data Output**
	TMS	**IEEE 1149.1 Test Mode Select Input**
	TCK	**IEEE 1149.1 Test Clock Input**
	TRSTN	**IEEE 1149.1 Test Reset Input**
	N/C	**No Connection.** Leave open-circuit, do not connect these pins.

Figure 3. AS1161 Pin Assignments (Top View)

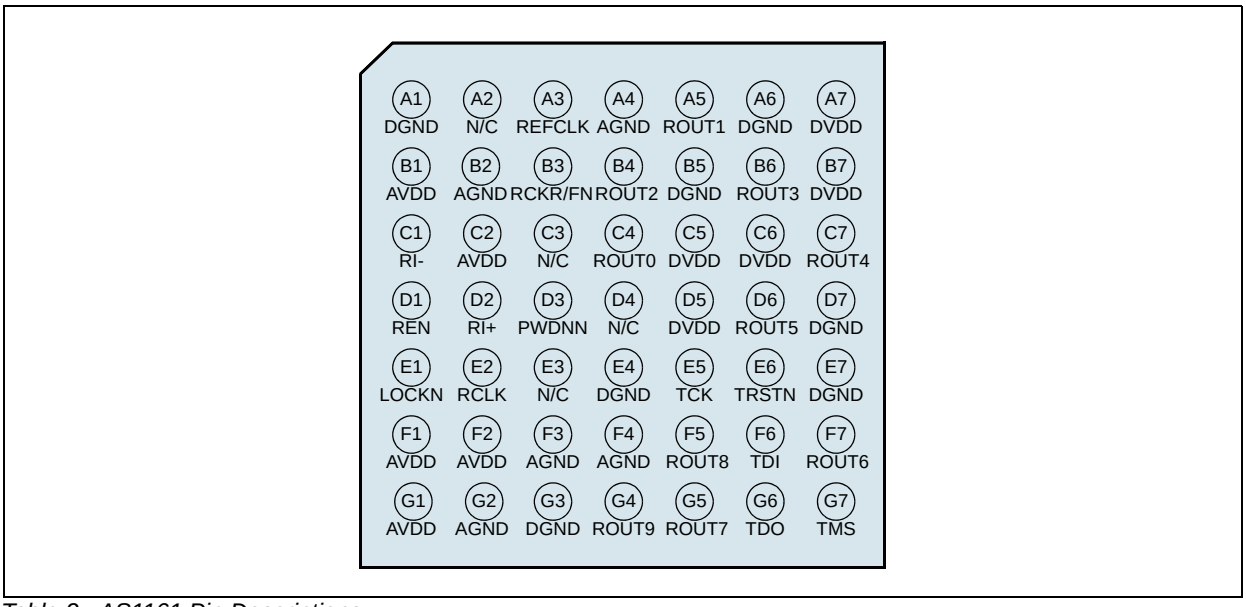


Table 2. AS1161 Pin Descriptions

Pin Number	Pin Name	Description
See Figure 3	ROUT0:ROUT9	**Data Output.** ±4mA CMOS level outputs.
	RCKR/FN	**Recovered Clock Rising/Falling Strobe Select.** LVTTL level input. Selects RCLK active edge for strobing of ROUT0:ROUT9 data. 1 = Rising edge. 0 = Falling edge.
	REFCLK	**Reference Clock Input.** LVTTL level input. Input for 20MHz - 66MHz system clock.
	RI+	**+ Serial Data Input.** Non-inverting Bus LVDS differential input.
	RI-	**- Serial Data Input.** Inverting Bus LVDS differential input.
	PWDNN	**Powerdown.** LVTTL level input. Driving this pin low shuts down the PLL, tri-states the outputs and puts the device into low power sleep mode.
	LOCKN	**Lock.** CMOS level output. This signal goes low when the deserializer PLL locks onto the embedded clock edge.
	RCLK	**Recovered Clock.** CMOS level output. Parallel data rate clock recovered from embedded clock. Used to strobe ROUT0:ROUT9.
	REN	**Output Enable.** LVTTL level input. If REN is set to logic low ROUT0:ROUT9 and RCLK are in tri-state condition.
	DVDD	**+3.0V to +3.6V Digital Circuit Power Supply.** This is the supply for all digital circuitry.
	DGND	**Digital Circuit Ground**
	AVDD	**+3.0V to +3.6V Analog Power Supply** (PLL and Analog Circuits)**.** AVDD and DVDD should be at the same potential and must not be more than 0.3V apart even on transient basis. Both supplys should be decoupled by a capacitor of typically 10nF.
	AGND	**Analog Ground** (PLL and Analog Circuits).
	TDI	**IEEE 1149.1 Test Data Input**
	TDO	**IEEE 1149.1 Test Data Output**
	TMS	**IEEE 1149.1 Test Mode Select Input**
	TCK	**IEEE 1149.1 Test Clock Input**
	TRSTN	**IEEE 1149.1 Test Reset Input**
	N/C	**No Connection.** Leave open-circuit, do not connect these pins.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
AVDD, DVDD	-0.3	+4	V	
LVCMOS/LVTTL Input	-0.3	V_{DD} + 0.3	V	
LVCMOS/LVTTL Output	-0.3	V_{DD} + 0.3	V	
Bus LVDS Receiver Input/Output	-0.3	+3.9	V	
Bus LVDS Output Short-Circuit Duration		10	ms	
Power Dissipation		1.47	W	Derate at 11.8mW/ºC above 25ºC
θ_{JA}		85	ºC/W	
ESD	2		kV	*HBM MIL-Std. 883E 3015.7 methods;*
Operating Temperature	-40	+85	ºC	
Storage Temperature	-65	+150	ºC	
Junction Temperature		+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

AV_{DD} = DV_{DD} = 3V to 3.6V, T_{AMB} = -40°C to +85°C, R_{LOAD}=28Ω, C_{LOAD} = 10pF, typical values @ T_{AMB} = +25°C and V_{DD} = 3.3V (unless otherwise specified).

Serializer Electrical Characteristics

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serializer LVCMOS/LVTTL DC Specifications (pins DINx, TCLK, PWDNN, TCKR/FN, SYNC1, SYNC2, DEN)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V	-1		+1	µA
Serializer Bus LVDS DC Specifications (pins DO+ and DO-)						
V_{OD}	Output Differential Voltage (DO+ to DO-)	Figure 34 on page 18	200	360		mV
ΔV_{OD}	Output Differential Voltage Unbalance			1	35	mV
V_{OS}	Offset Voltage		1.1	1.2	1.3	V
ΔV_{OS}	Offset Voltage Unbalance			2	35	mV
I_{OS}	Output Short-Circuit Current	DO = 0V, DIN = High, PWDNN and DEN = V_{DD}		-13	-20	mA
I_{OZ}	Tri-State Output Current	PWDNN or DEN = GND, DO = 0V or V_{DD}	-1		+1	µA
I_{OX}	Power-Off Output Current	PWDNN = DEN = V_{DD} = 0V, DO = 0V or 3.6V	-1		+1	µA
Serializer Supply Current (pins DVDD and AVDD)						
I_{CCD}	Serializer Supply Current (Worst Case) ICC-Pattern	Figure 16 on page 12, f = 20MHz		35	50	mA
		Figure 16 on page 12, f = 66MHz		70	90	
I_{CCXD}	Serializer Supply Current (Powerdown)	PWDNN = GND, f_{CLK} = DC (off)		400	700	µA

Serializer Timing Requirements for TCLK

Table 5. Serializer Timing Requirements for TCLK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	Transmit Clock Freq.	Figure 20 on page 13	20		66	MHz
t_{TCP}	Transmit Clock Period		15.15		50	ns
t_{TCDC}	Transmit Clock Duty Cycle		40		60	%
t_{CLKT}	TCLK Input Transition Time			3	6	ns
t_{JIT}	TCLK Input Jitter				150	ps (RMS)

Serializer Switching Characteristics

Table 6. Serializer Switching Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LLHT}	Bus LVDS Low-to-High Transition Time	Figure 18 on page 13		0.25	0.4	ns
t_{LHLT}	Bus LVDS High-to-Low Transition Time			0.25	0.4	ns

Table 6. Serializer Switching Characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{DIS}	DIN_x Setup to TCLK Time	Figure 21 on page 13		0			ns
t_{DIH}	DIN_x Hold from TCLK Time			4			ns
t_{HZD}	DO+, DO- High-to-Tri-State Delay	Figure 22 on page 14 [2]			1.5	5	ns
t_{LZD}	DO+, DO- Low-to-Tri-State Delay				1.5	5	ns
t_{ZHD}	DO+, DO- Tri-State-to-High Delay				1.5	5	ns
t_{ZLD}	DO+, DO- Tri-State-to-Low Delay				1.5	5	ns
t_{PWDL}	PWDNN minimum low time after V_{DD} is in regulation	Figure 23 on page 14		50			µs
t_{SPW}	SYNC Pulse Width	Figure 25 on page 15		5 x t_{TCP}			ns
t_{PLD}	Serializer PLL Lock Time	Figure 24 on page 14				400 x t_{TCP}	ns
t_{SD}	Serializer Delay	Figure 26 on page 15		$t_{TCP}/2$	$t_{TCP}/2$ + 3	$t_{TCP}/2$ + 5	ns
t_{DJIT}	Deterministic Jitter (p-p) (Worst Case) ICC-Pattern	Figure 32 on page 18	f = 20MHz		150	300	ps (pp)
			f = 66MHz		50	100	ps (pp)
t_{RJIT}	Random Jitter (Worst Case) ICC-Pattern		f = 20MHz		25	45	ps (RMS)
			f = 66MHz		8	15	

1. Guaranteed by simulation and characterization.
2. Because the serializer is in tri-state mode, the deserializer will lose PLL lock and have to resynchronize before data transfer.

Deserializer Electrical Characteristics

AV_{DD} = DV_{DD} = 3V to 3.6V, T_{AMB} = -40°C to +85°C, R_{LOAD}=28Ω, C_{LOAD} = 15pF, Receiver Input Range: 0V to 2.4V, typical values @ T_{AMB} = +25°C and V_{DD} = 3.3V (unless otherwise specified).

Table 7. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Deserializer Bus LVDS DC Specifications (pins RI+ and RI-)						
V_{TH}	Differential Threshold High Voltage	V_{CM} = +1.2V		+10	+75	mv
V_{TL}	Differential Threshold Low Voltage		-75	-20		
I_{IN}	Input Current	V_{IN} = 2.4V, V_{DD} = 3.6V or 0V	-1		+1	µA
		V_{IN} = 0V, V_{DD} = 3.6V or 0V	-1		+1	
Deserializer LVCMOS/LVTTL DC Specifications (input pins PWDNN, RCKR/FN, REN, REFCLK; output pins ROUT0:ROUT9, RCLK, LOCKN)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V	-1		+1	µA

Table 7. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{ILR}	Input Current, TMS, TDI, TRSTN inputs	V_{IN} = 0V			-30	-60	µA
V_{OH}	High Level Output Voltage	I_{OH} = -4 mA		2.2	3.0	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OH} = 4 mA		GND	0.25	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		-15	-35	-60	mA
I_{OS}	Output Short Circuit Current, TDO output			-80	-150	-220	mA
I_{OZ}	Tri-State Output Current	PWDNN or REN = 0V, V_{OUT} = 0V or V_{DD}		-1		+1	µA
Deserializer Supply Current (pins DVDD and AVDD)							
I_{CCR}	Deserializer Supply Current (Worst Case)	Figure 17 on page 12	f = 20MHz		45	60	mA
			f = 66MHz		100	130	
I_{CCXR}	Deserializer Supply Current (Powerdown)	PWDNN = 0V, REN = 0V			0.75	1.0	mA

Deserializer Timing Requirements for REFCLK

Table 8. Deserializer Timing Requirements for REFCLK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RFCLK}	REFCLK Frequency		20		66	MHz
t_{RFCP}	REFCLK Period		15.15	T	50	ns
t_{RFDC}	REFCLK Duty Cycle		30	50	70	%
t_{RFCP}/t_{TCP}	REFCLK-to-TCLK Ratio		95	1	105	
t_{RFTT}	REFCLK Transition Time			3	6	ns

Deserializer Switching Characteristics

Table 9. Deserializer Switching Characteristics[1]

Symbol	Parameter	Conditions	Pin/ Frequency	Min	Typ	Max	Unit
t_{RCP}	Receiver Out Clock Period	t_{RCP} = t_{TCP}, Figure 26 on page 15	RCLK	15.15		50	ns
t_{CLH}	CMOS/TTL Low-to-High Transition Time	Figure 19 on page 13	RCLK, R_{OUTx}, LOCKN		1.5	4	ns
t_{CHL}	CMOS/TTL High-to-Low Transition Time				1.4	4	ns
t_{DD}	Deserializer Delay, Figure 27 on page 16	All temperatures, all frequencies		1.6 x t_{RCP} + 1.0		1.75 x t_{RCP} + 7.0	ns
		Room temperature, 3.3V	20MHz	1.6 x t_{RCP} + 2.0	1.6 x t_{RCP} + 4.0	1.6 x t_{RCP} + 6.0	
		Room temperature, 3.3V	66MHz	1.75 x t_{RCP} + 2.0	1.75 x t_{RCP} + 4.0	1.75 x t_{RCP} + 6.0	
t_{ROS}	R_{OUT} Data Valid Before RCLK Time	Figure 28 on page 16	20MHz	0.4 x t_{RCP}	0.5 x t_{RCP}		ns
			66MHz	0.38 x t_{RCP}	0.5 x t_{RCP}		
t_{ROH}	R_{OUT} Data Valid After RCLK Time	Figure 28 on page 16	20MHz	-0.4 x t_{RCP}	0.5 x t_{RCP}		ns
			66MHz	-0.38 x t_{RCP}	-0.5 x t_{RCP}		

Table 9. Deserializer Switching Characteristics[1]

Symbol	Parameter	Conditions	Pin/ Frequency	Min	Typ	Max	Unit
t_{RDC}	RCLK Duty Cycle			45	50	55	ns
t_{HZR}	High to Tri-State Delay	Figure 29 on page 16	ROUTx	3	6		ns
t_{LZR}	Low to Tri-State Delay		ROUTx	3	6		ns
t_{ZHR}	Tri-State to High Delay		ROUTx	4	6		ns
t_{ZLR}	Tri-State to Low Delay		ROUTx	4	6		ns
t_{DSR1}[2]	Deserializer PLL Lock Time from PWDNN (with SYNCPAT)	Figure 30 on page 17, Figure 31 on page 17	20MHz		5.2	7.5	µs
			66MHz		1.8	3	µs
t_{DSR2}[2]	Deserializer PLL Lock Time from SYNCPAT		20MHz		5.1	7.5	µs
			66MHz		1.9	3	µs
t_{ZHLK}	Tri-State to High Delay (Powerup)		LOCKN		4	12	ns
t_{RCLKL}[1]	RCLK low time before LOCK achieved		RCLK		32xt_{RFCP}		ns
t_{RNM}[3]	Deserializer Noise Margin	Figure 33 on page 18	20MHz	0.8	1		ns
			66MHz	200	300		ps

1. Guaranteed by simulation and characterization.
2. For the purpose of specifying deserializer PLL performance, t_{DSR1} and t_{DSR2} are specified with the REFCLK running and stable, and with specific conditions for the incoming data stream synchronization patterns (SYNCPATs). The derserializer should be initialized using either t_{DSR1} or t_{DSR2}.
   t_{DSR1} is the time required for the deserializer to indicate lock upon power-up or when leaving the power-down mode. SYNCPATs should be sent to the device before initiating either condition.
   t_{DSR2} is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI-) conditions change from not receiving data to receiving SYNCPATs.
3. t_{RNM} is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. The deserializer noise margin is guaranteed by design using statistical analysis.

Scan Circuitry Timing Requirements

Table 10. Scan Circuitry Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TCK}	TCK Clock Frequency	Figure 15 on page 12		25		MHz
t_{TCK}	TCK Clock Period			40		ns
t_S	TCK to TDI, TMS Setup Time		2.0			ns
t_H	TCK to TDI, TMS Hold Time		3.0			ns
t_{WH}, t_{WL}	TCK Pulse Width, High or Low		10.0			ns
t_{WR}	TRSTN Pulse Width, Low		2.5			ns
t_{REC}	TRSTN-to-TCK Recovery Time		2.0			ns
t_D	TCK to TDO Delay				10	ns
t_Z	TCK to TDO High Z Delay				10	ns

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics AS1160

V_{DD} = 3.6V, R_{LOAD} = 28Ω, C_{LOAD} = 10pF, *T_{AMB} = +25ºC (unless otherwise specified);*

Figure 4. Supply Current vs Supply Voltage

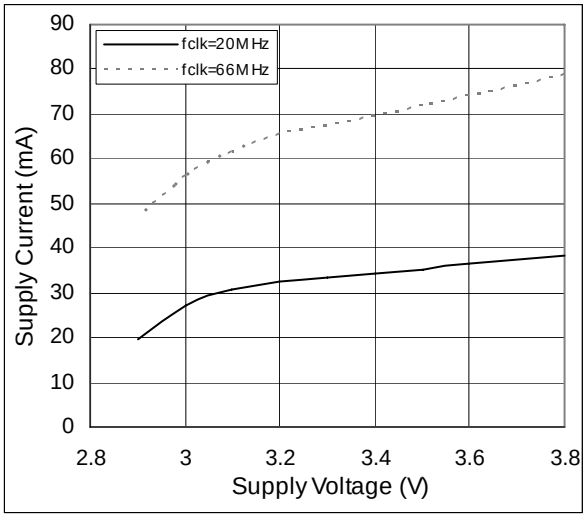


Figure 5. Power-Down Current vs Supply Voltage

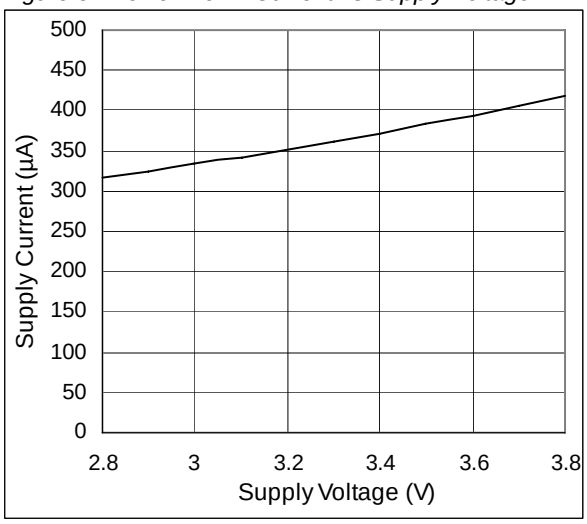


Figure 6. Supply Current vs Clock Frequency

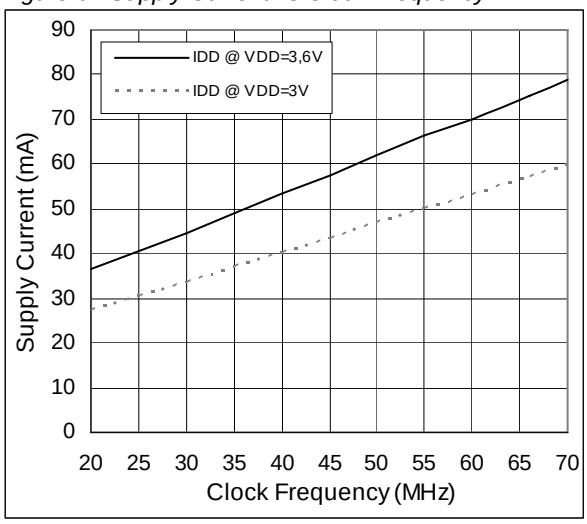


Figure 7. Supply Current vs Temperature

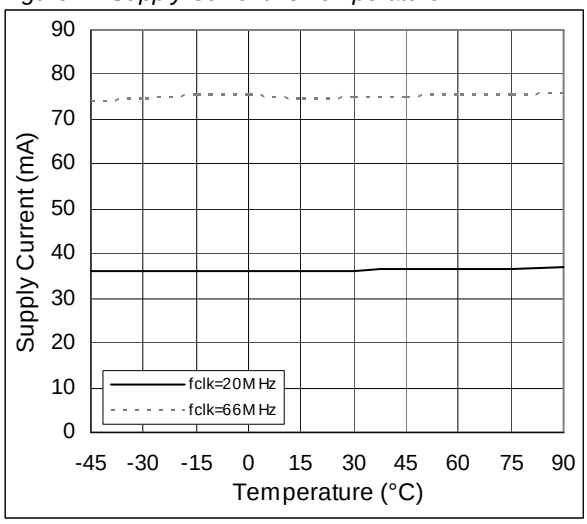


Figure 8. Power-Down Current vs. Temperature

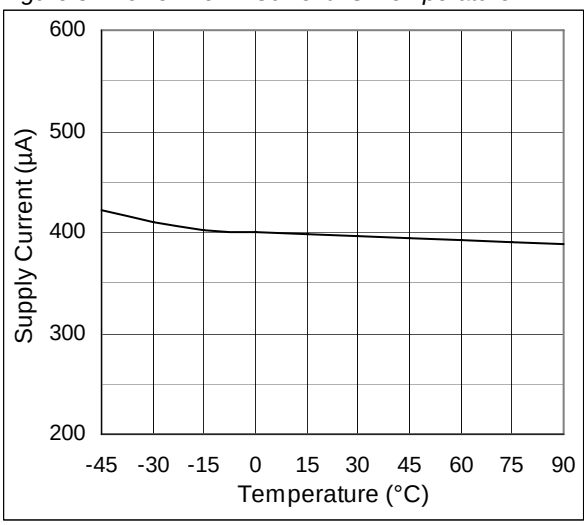
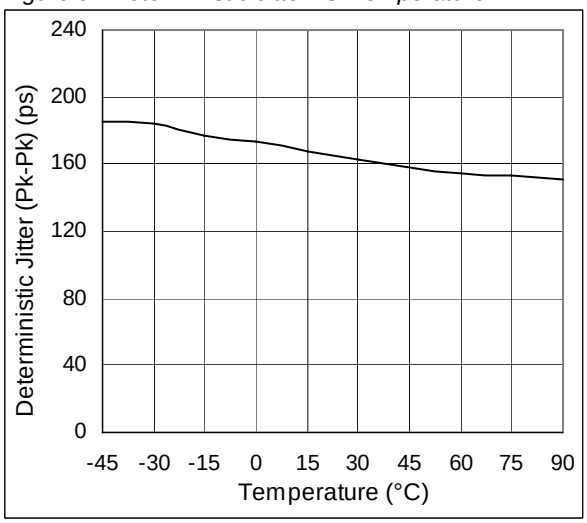


Figure 9. Deterministic Jitter vs. Temperature



8 Typical Operating Characteristics AS1161

V_{DD} = 3.6V, C_{LOAD} = 15pF, *T_{AMB} = +25ºC (unless otherwise specified);*

Figure 10. Supply Current vs Supply Voltage

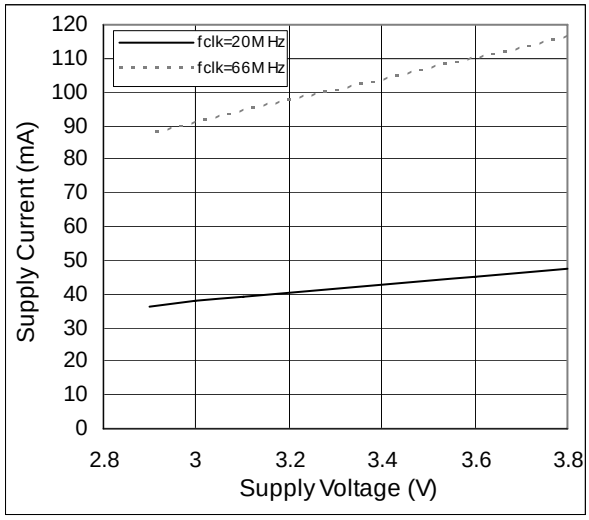


Figure 11. Power-Down Current vs Supply Voltage

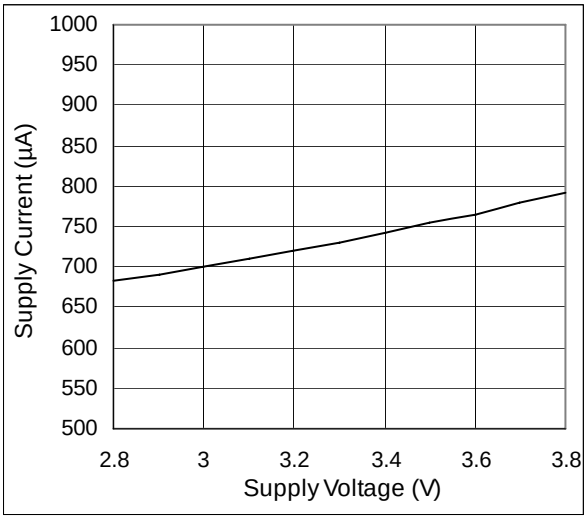


Figure 12. Supply Current vs Clock Frequency

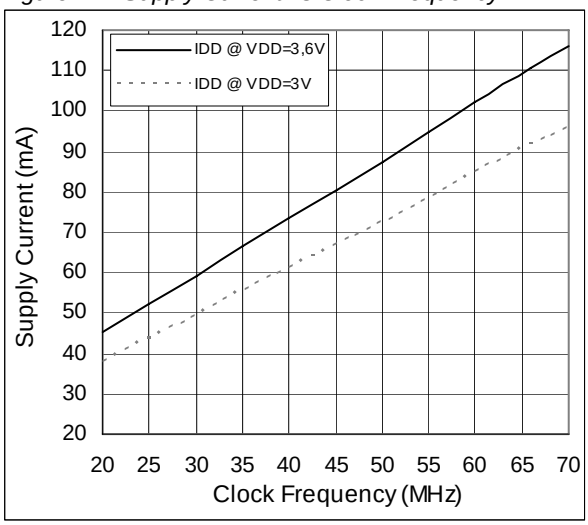


Figure 13. Supply Current vs Temperature

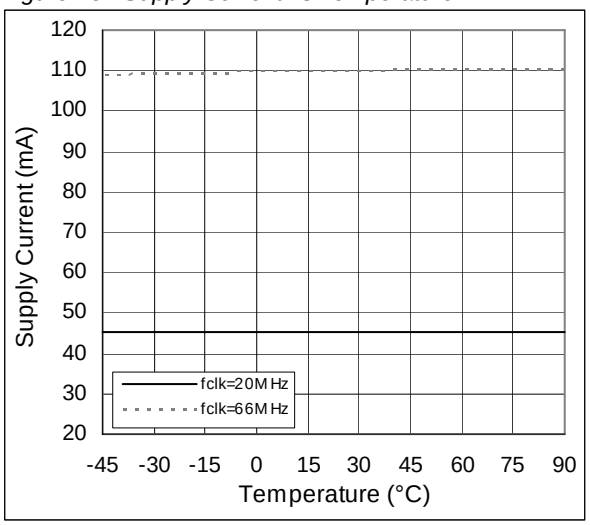
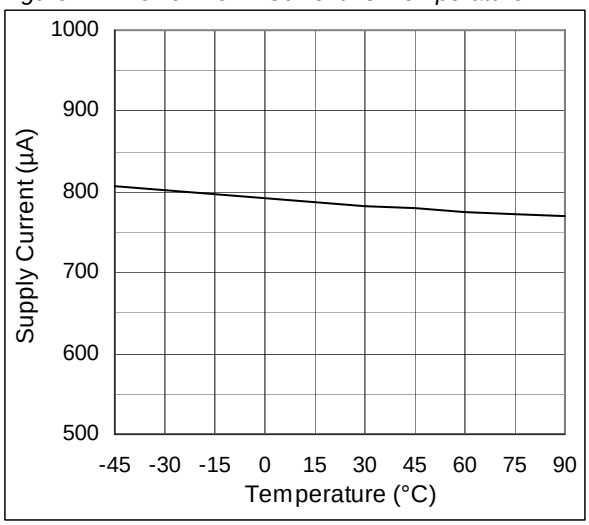


Figure 14. Power-Down Current vs. Temperature



9 Timing Diagrams

Figure 15. JTAG Timing Diagram

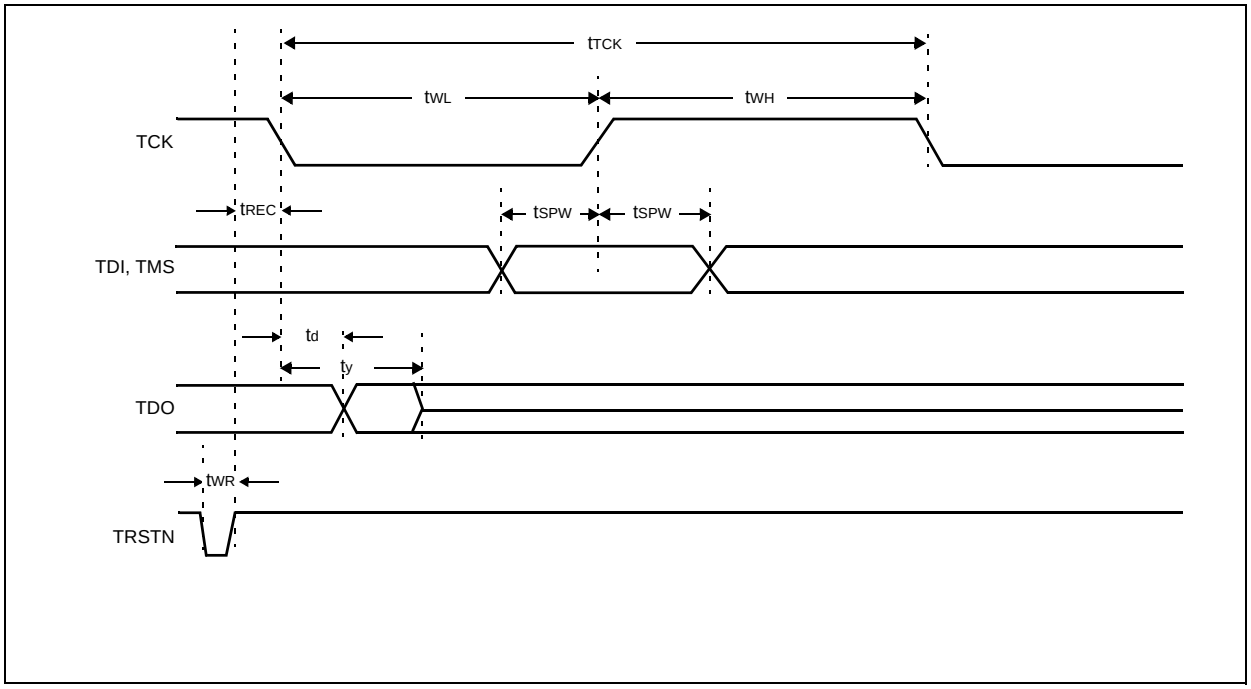


Figure 16. Worst-Case Serializer ICC Test Pattern

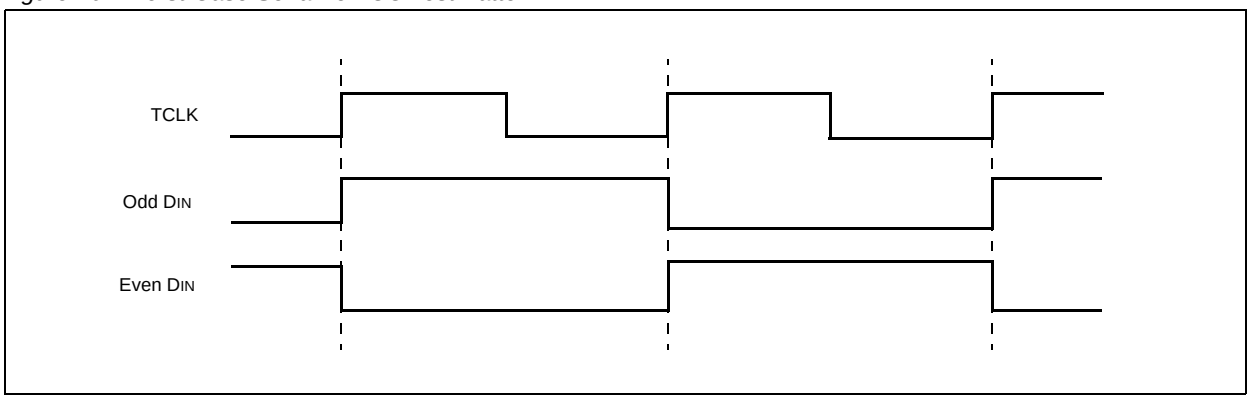


Figure 17. Worst-Case Deserializer ICC Test Pattern

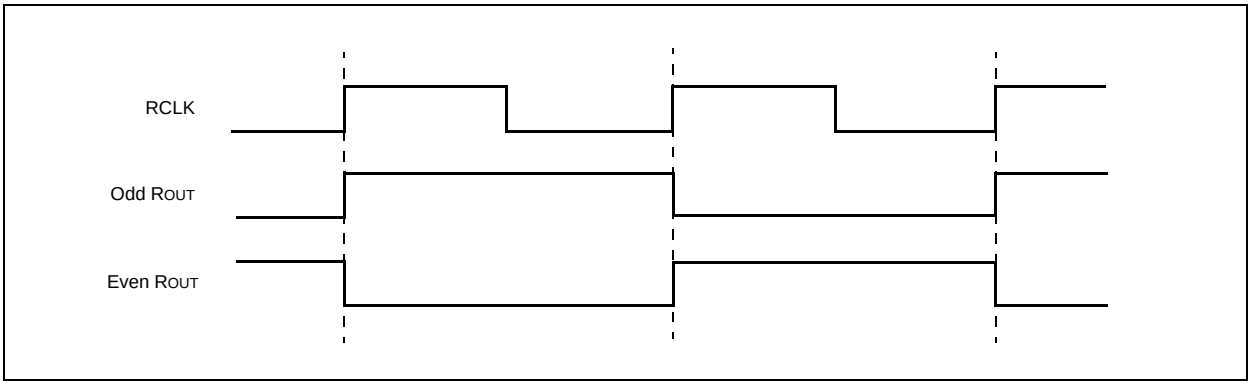


Figure 18. Serializer Bus LVDS *Output Load and Transition Times*

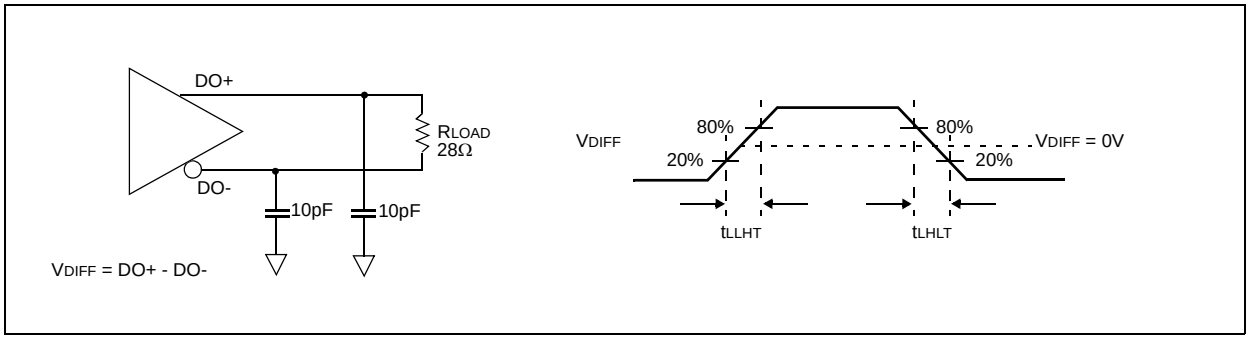


Figure 19. Deserializer CMOS/TTL Output Load and Transition Times

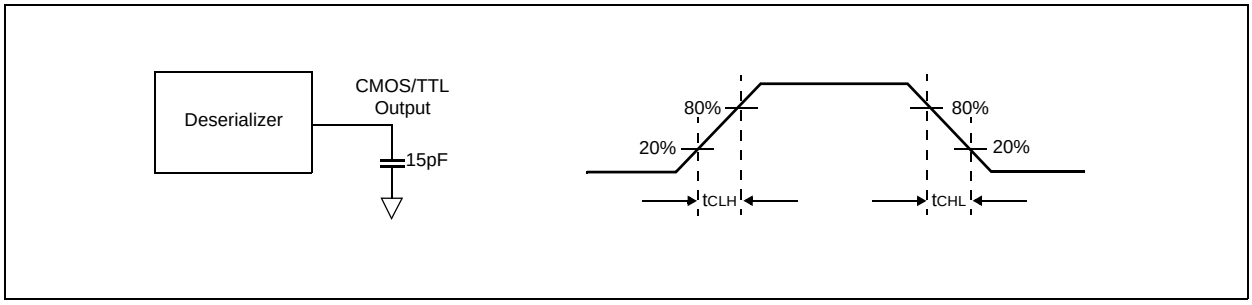


Figure 20. Serializer Input Clock Transition Time

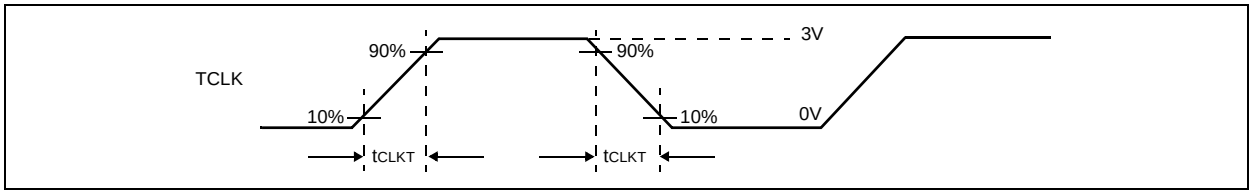


Figure 21. Serializer Setup and Hold Times

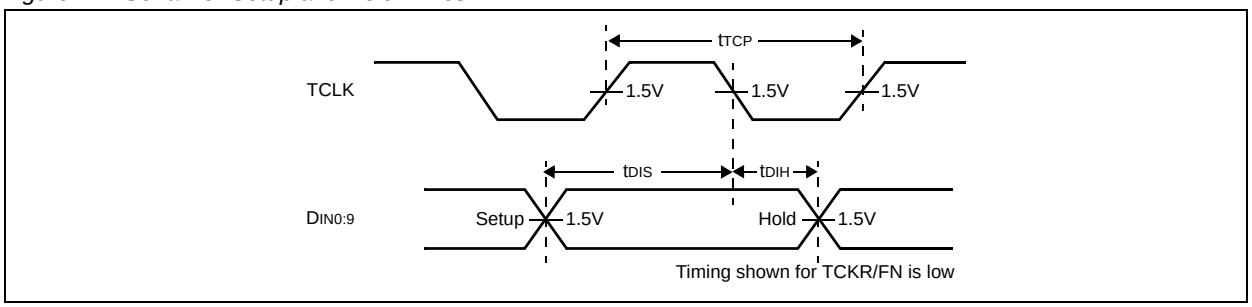


Figure 22. Serializer Tri-State Test Circuit and Timing

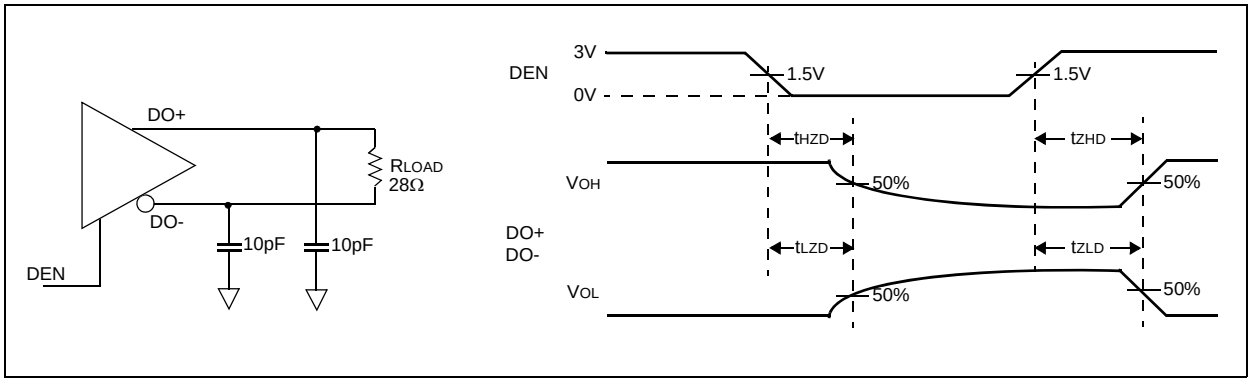


Figure 23. Serializer Power Up Timing

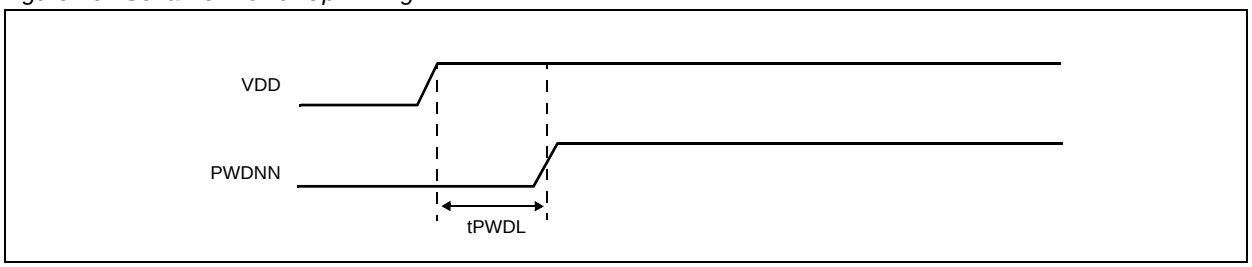


Figure 24. Serializer PLL Lock Time and PWDNN Tri-State Delays

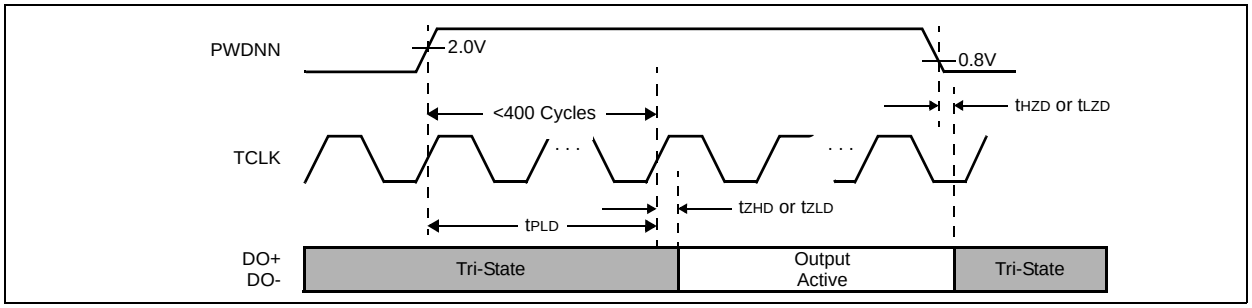


Figure 25. SYNC Timing Delays

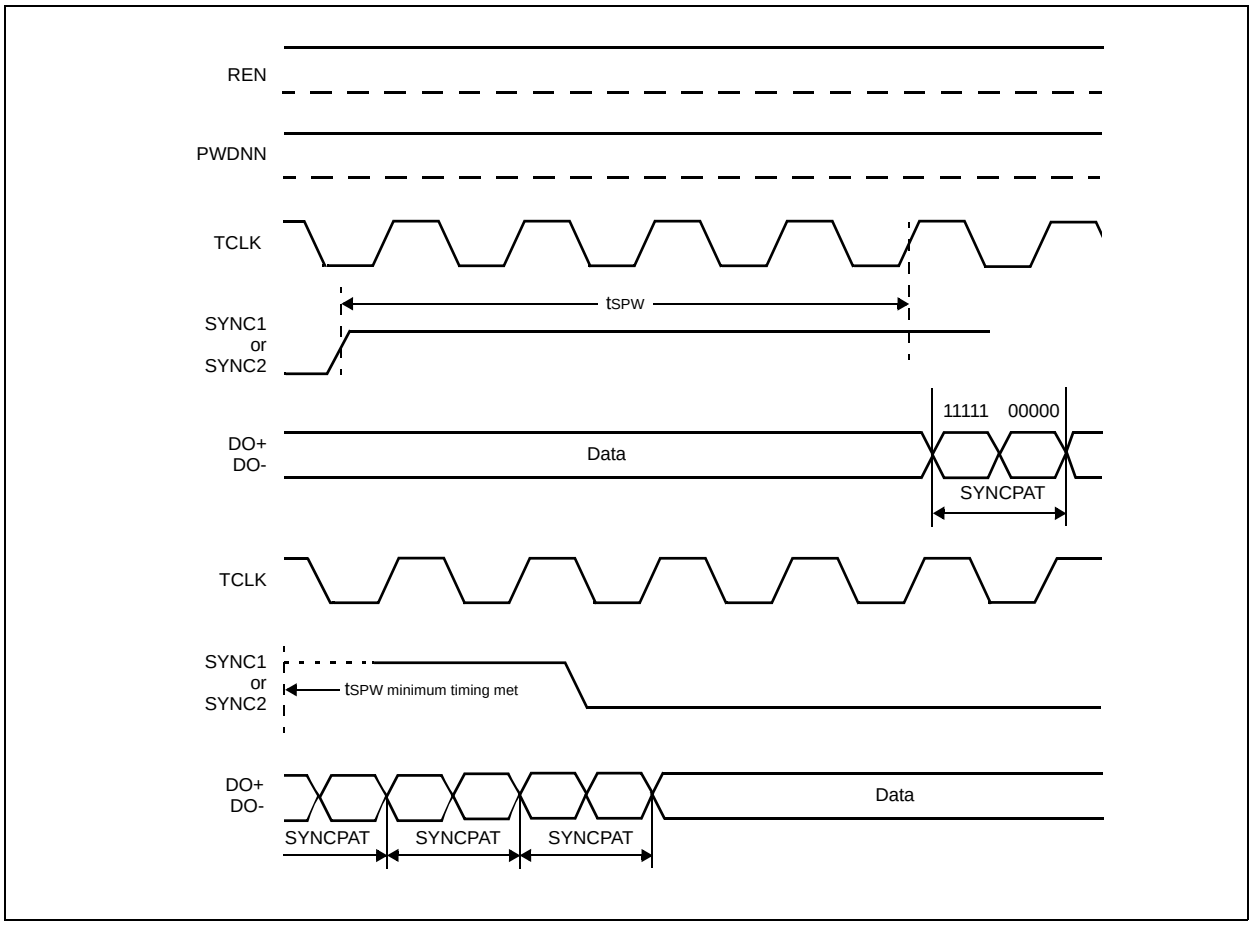


Figure 26. Serializer Delay

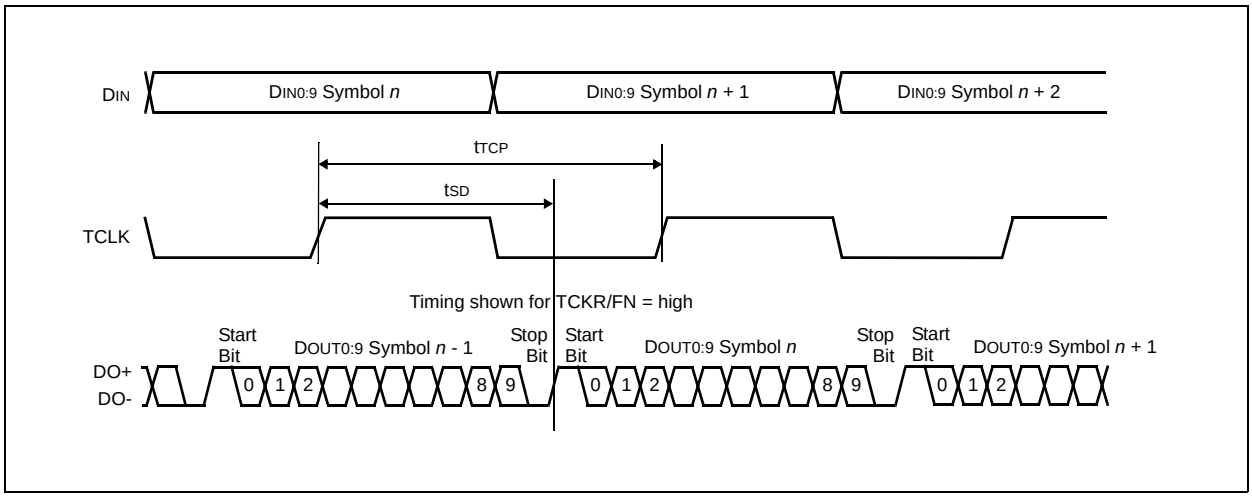


Figure 27. Deserializer Delay

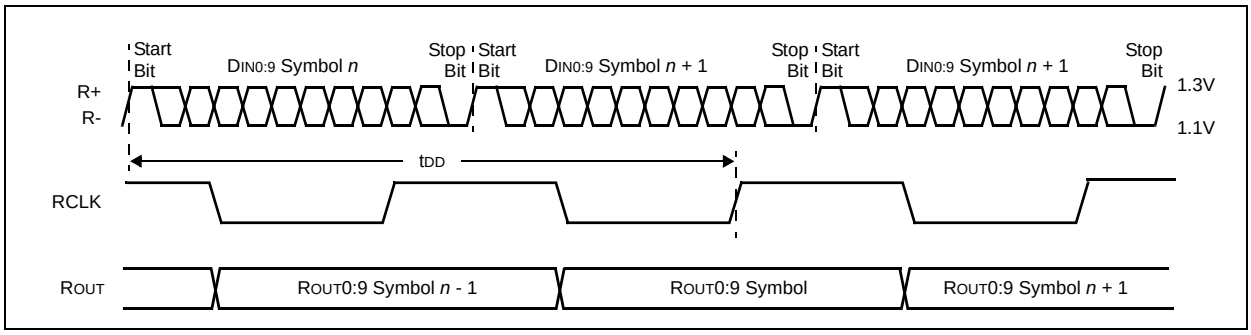


Figure 28. Deserializer Data Valid Out Times

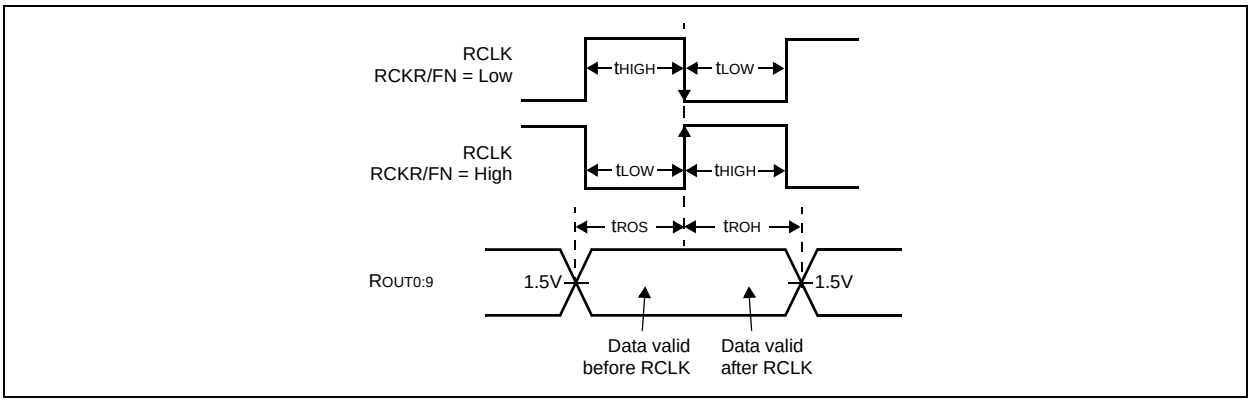


Figure 29. Deserializer Tri-State Test Circuit and Timing Diagram

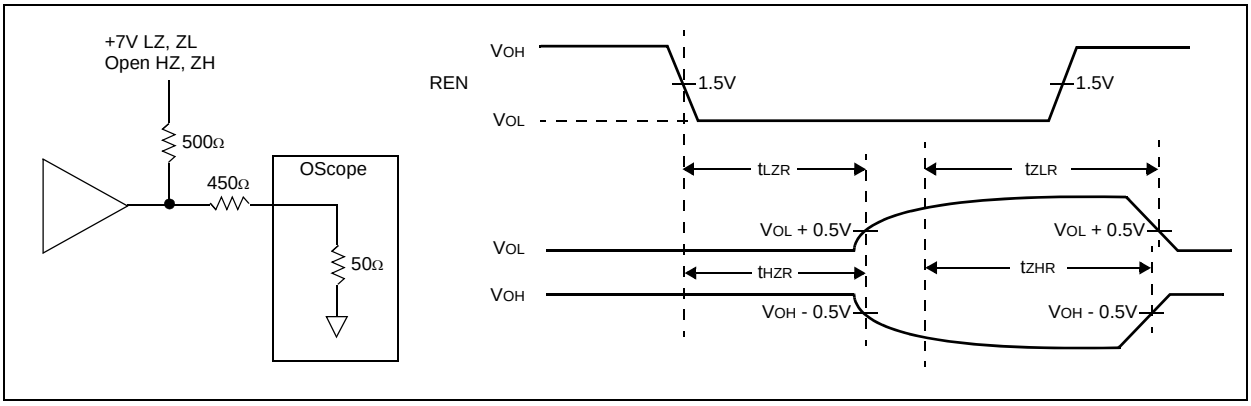


Figure 30. Deserializer PLL Lock Times and PWDNN Tri-State Delays

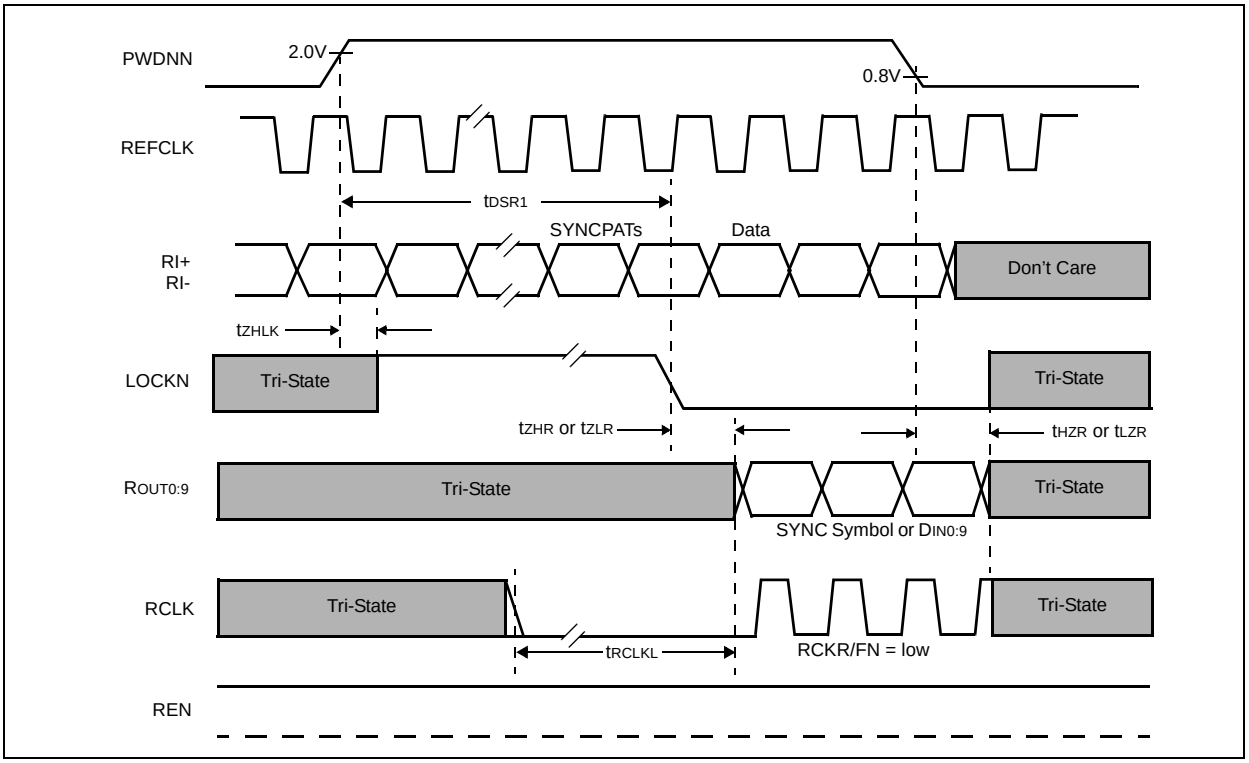


Figure 31. Deserializer PLL Lock Time from SYNCPAT

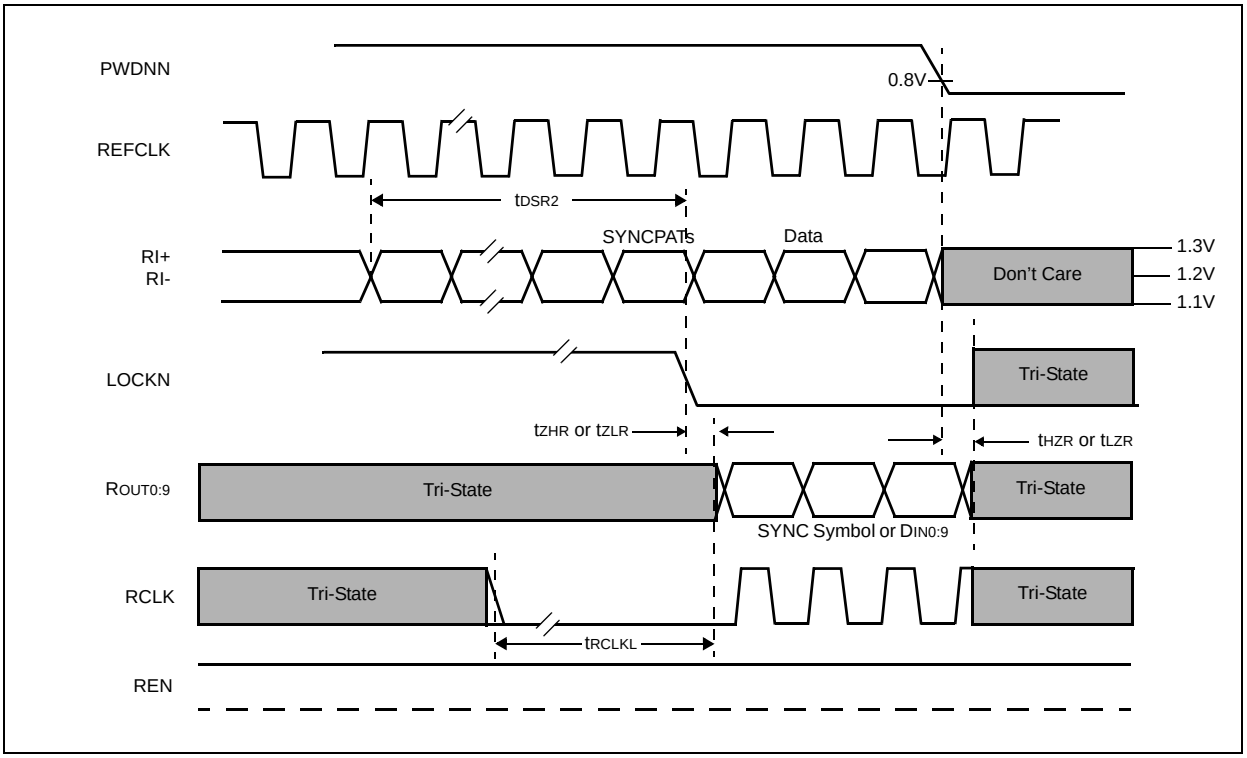


Figure 32. Definition of Deterministic Jitter (t_{DJIT})

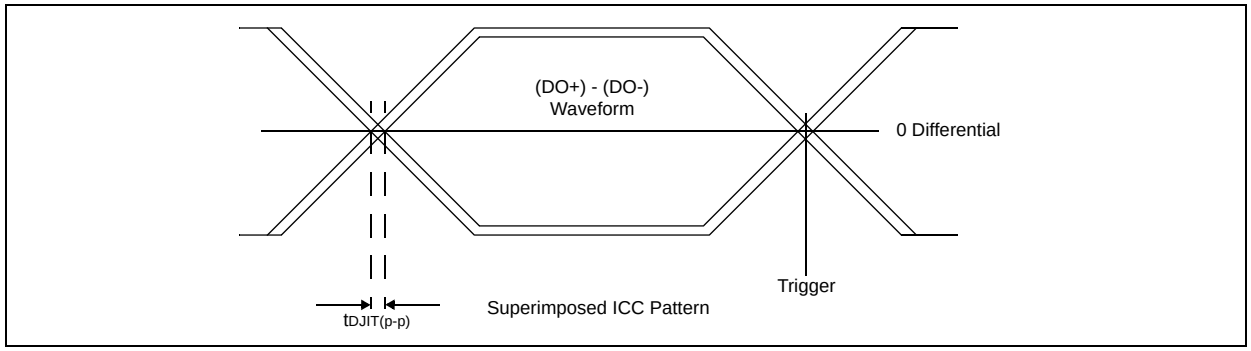
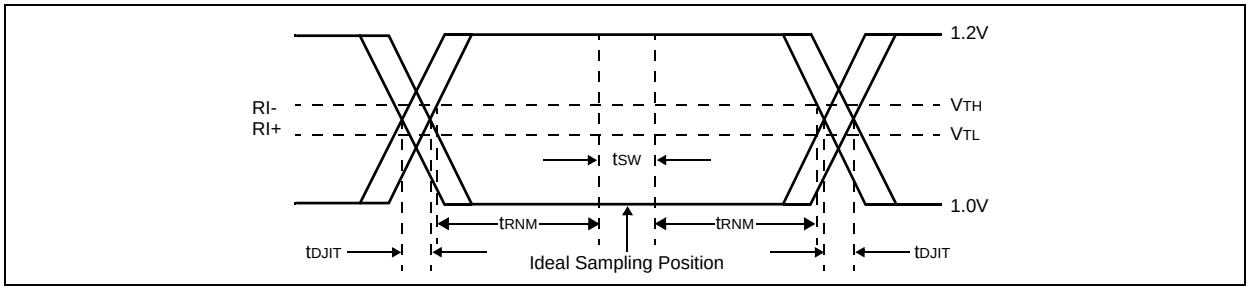


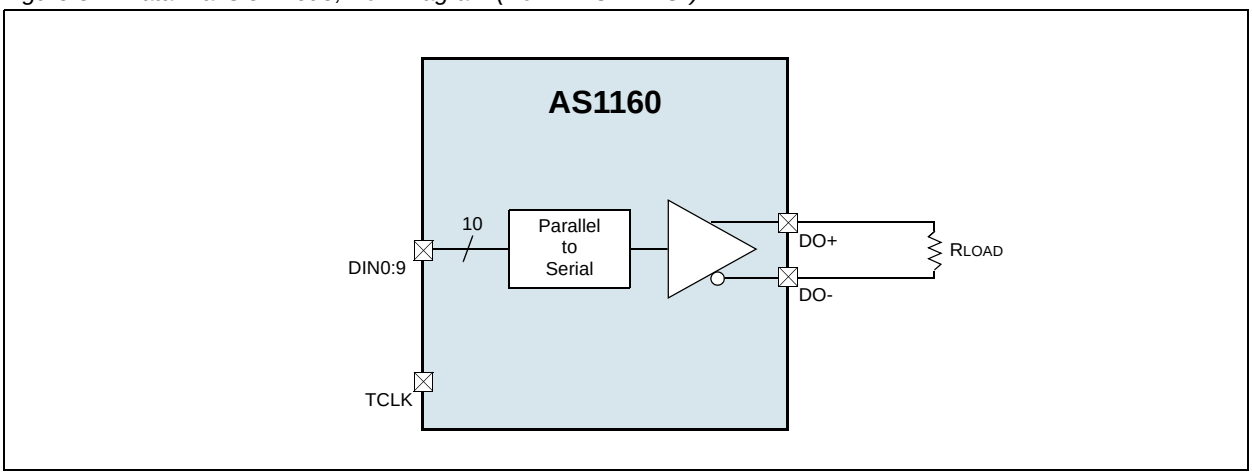
Figure 33. Receiver Bus LVDS Input Skew Margin



Where:

tSW is the setup and hold time (internal data sampling window).
tDJIT is the serializer output bit position jitter as a result of jitter on TCLK.
tRNM is the receiver noise time margin.

Figure 34. Data Transfer Mode, VOD Diagram (VOD = DO+ - DO-)



10 Detailed Description

The serializer/deserializer chipset transfers 10 parallel LVTTL data bits over a serial Bus LVDS link up to 660Mbps at clock speeds from 20MHz to 66MHz.

For the serializer, an on-board PLL serializes the input data and inserts two control bits (start & stop bit) into the data stream.

The deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The deserializer monitors the incoming clock information, determines lock status and asserts the LOCKN output high when loss of lock occurs.

Note: The chipset is also capable of driving data over unshielded twisted pair cable.

The chipset has three active states of operation:

- Initialization
- Data Transfer
- Resynchronization

The chipset also has two passive states:

- Powerdown
- Tri-State

Note: There are also test modes for JTAG access and at-speed BIST (built-in-self-test).

Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the serializer and deserializer PLLs to local clocks, which may be the same or separate. Afterwards, synchronization of the deserializer to the serializer occurs.

1. When V_{DD} is applied and reaches a stable value between +3.0V and +3.6V, the PWDNN of the serializer has to stay low for at least 50µs to ensure proper operation (see Figure 23 on page 14), the respective output enter tri-state. After PWDNN is high the PLL in the serializer begins locking to a local clock.
   When V_{DD} is applied to the deserializer, the respective outputs enter tri-state and an on-chip power-on circuitry disables internal circuitry. When V_{DD} reaches V_{DDOK} (2.5V) the PLL in the deserializer begins locking to a local clock. For the serializer, the local clock is the transmited clock (TCLK) provided by the source ASIC or other device. For the deserializer, a local clock must be applied to pin REFCLK that can be provided by any source.
   The serializer outputs remain in tri-state while the PLL locks to the TCLK. After locking to TCLK, the serializer is now ready to send data or SYNCPATs (SYNC patterns), depending on the levels of the SYNC1 and SYNC2 inputs or a data stream.
   The SYNCPAT sent by the serializer consists of six ones and six zeros switching at the input clock rate. Note that the deserializer LOCKN output will remain high while its PLL locks to the incoming data or to SYNCPATs on the input.
2. The deserializer PLL must synchronize to the serializer to complete initialization. The deserializer will lock to non-repetitive data patterns. However, the transmission of SYNCPATs enables the deserializer to lock to the serializer signal within a specified time (see Figure 24 on page 14).
   The application determines control of pins SYNC1 and SYNC2. A direct feedback loop from the LOCKN pin is mandatory (see Figure 36 on page 23). In all cases the serializer stops sending SYNCPATs after both SYNC inputs return low.
   When the deserializer detects edge transitions at the bus LVDS input, it will attempt to lock to the embedded clock information. When the deserializer locks to the bus LVDS clock, the LOCKN output will go low. When LOCKN is low, the deserializer outputs represent incoming bus LVDS data.

Data Transfer

After initialization, the serializer will accept data from inputs DIN0:DIN9. The serializer uses TCLK to latch incoming data. TCKR/FN selects which edge the serializer uses to strobe incoming data. TCKR/FN high selects the rising edge for clocking data and low selects the falling edge. If SYNC1 or SYNC2 is high for more than 5 TCLK cycles, the data at DIN0:DIN9 is ignored regardless of clock edge.

After determining which clock edge to use a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. In the serial stream the start and stop bits are used as the embedded clock bits.

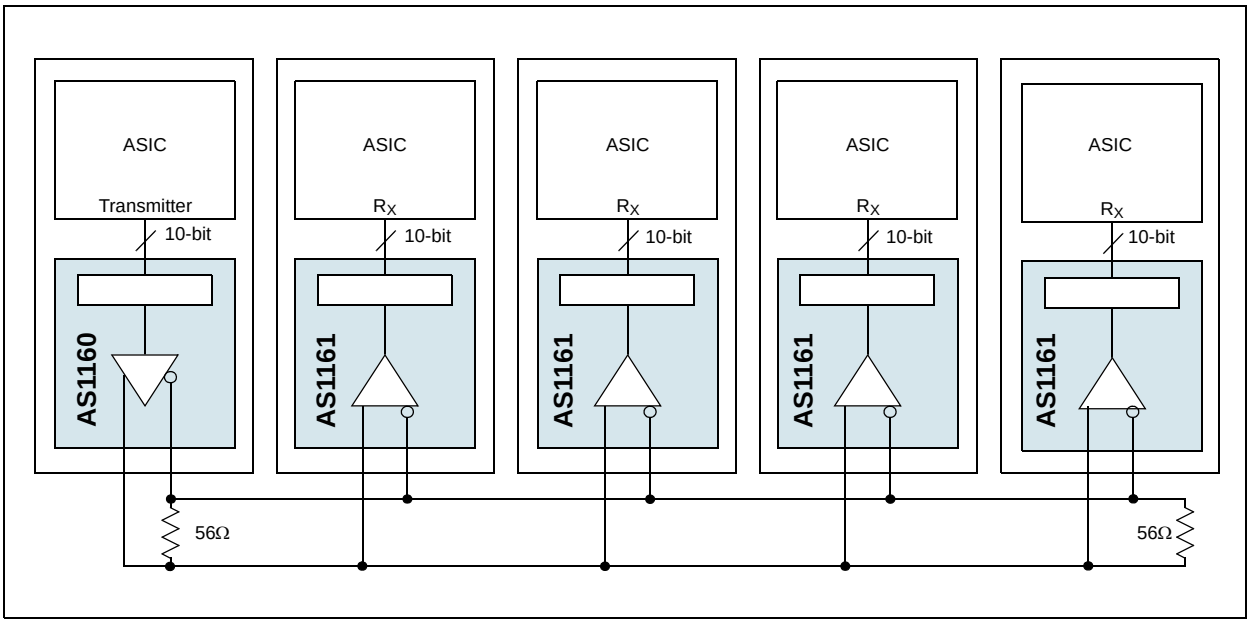
The serializer transmits serialized data and clock bits (10 + 2 bits) from the serial data output (DO+ and DO-) at 12 times the TCLK frequency. For example, if TCLK is 66MHz, the serial rate is 66 x 12 = 792 mega bits per second. Since only 10 bits are from input data, the serial payload rate is 10 times the TCLK frequency (if TCLK = 66MHz, the payload data rate is 66 x 10 = 660Mbps). The data source provides TCLK and must be in the range of 20MHz to 66MHz nominal.

The serializer outputs (DO+ and DO-) can drive a point-to-point connection (see Figure 37 on page 24) or a multidrop configuration (see Figure 35). In a multidrop configuration one serializer is connected through a backplane bus with limited multiple deserializers.

The outputs transmit data when DEN, PWDNN are high and SYNC1, SYNC2 are low.

Note: When DEN is driven low, the serializer output pins will enter tri-state.

Figure 35. Multidrop Configuration



When the deserializer synchronizes to the serializer, pin LOCKN is low. The deserializer locks to the internal clock and uses it to recover the serialized data. ROUT0:ROUT9 data is valid when LOCKN is low, otherwise ROUT0:ROUT9 is invalid.

Pins ROUT0:ROUT9 use pin RCLK as the reference to data. The polarity of the RCLK edge is controlled by the RCKR/FN input (see Figure 28 on page 16). ROUT0:ROUT9, LOCKN and RCLK outputs will drive a maximum of three CMOS input gates (15pF load) with a 66MHz clock.

Resynchronization

When the deserializer PLL locks to the embedded clock edge, the deserializer LOCKN pin asserts a low. If the deserializer loses lock, pin LOCKN output will go high and the outputs (including RCLK) will enter tri-state.

The user's system monitors the pin LOCKN to detect a loss of synchronization. Upon detection, the system can arrange to pulse the serializer SYNC1 or SYNC2 pin to resynchronize.

Multiple resynchronization approaches are possible. It is mandatory to provide a feedback loop using pin LOCKN to control the SYNC request of the serializer (SYNC1 or SYNC2). Two SYNC pins are provided for multiple control in a multi-drop application. Sending SYNCPATs for resynchronization is desirable when lock times within a specific time are critical.

Powerdown

The low-power powerdown mode can be used while no data transfer is taking place. The serializer and deserializer use the powerdown mode to reduce power consumption by:

- The deserializer enters powerdown when pins PWDNN and REN are low.
- The serializer enters powerdown when pin PWDNN is driven low.

In powerdown, the PLL stops and the outputs enter tri-state, which disables load current and reduces supply current to the µA range.

Note: To exit powerdown, drive pin PWDNN high.

Before valid data exchanges between the serializer and deserializer, the devices must re-initialized and resynchronized to each other. Initialization of the serializer takes a maximum of 400 TCLK cycles. The deserializer will initialize and assert LOCKN high until lock to the Bus LVDS clock occurs.

Tri-State

The serializer enters tri-state when pin DEN is driven low. This puts both driver output pins (DO+ and DO-) into tri-state. When DEN is driven high, the serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, PWDNN, TCKR/FN).

When pin REN is driven low, the deserializer enters tri-state. Consequently, the receiver output pins (ROUT0:ROUT9) and RCLK will enter tri-state. The LOCKN output remains active, reflecting the state of the PLL.

11 Application Information

Power Considerations

An all CMOS design of the serializer and deserializer makes them inherently low power devices. In addition, the constant current source nature of the bus LVDS outputs minimizes the slope of the speed vs. IDD curve of conventional CMOS designs.

The pins AVDD and DVDD should be bypassed with a 100nF and a 1nF ceramic capacitor in parallel. The 1nF capacitor should be closest to the pin.

Powering up the Deserializer

The AS1161 can be powered up at any time by following a proper sequence. The REFCLK input can be running before the deserializer powers up and it must be running in order for the deserializer to lock to incoming data. The deserializer outputs will remain in tri-state until the deserializer detects data transmission at its inputs and locks to the incoming data stream.

Table 11. Deserializer Truth Table

Inputs		Outputs		
PWDNN	**REN**	**LOCKN**	**ROUTx**	**RCLK**
High	High	High (not locked)	Z	Z
High	High	Low (not locked)	Active[1]	Active[1]
Low	X (dont care)	Z	Z	Z
High	Low	Active[2]	Z	Z

1. Active indicates the RCLK will be running if the deserializer is locked. The timing of RCLK with respect to ROUT0:ROUT9 is determined by RCKR/FN. ROUT0:ROUT9 and RCLK are tri-stated when LOCKN is asserted high.
2. Active indicates the LOCKN output will reflect the state of the deserializer with regard to the selected data stream.

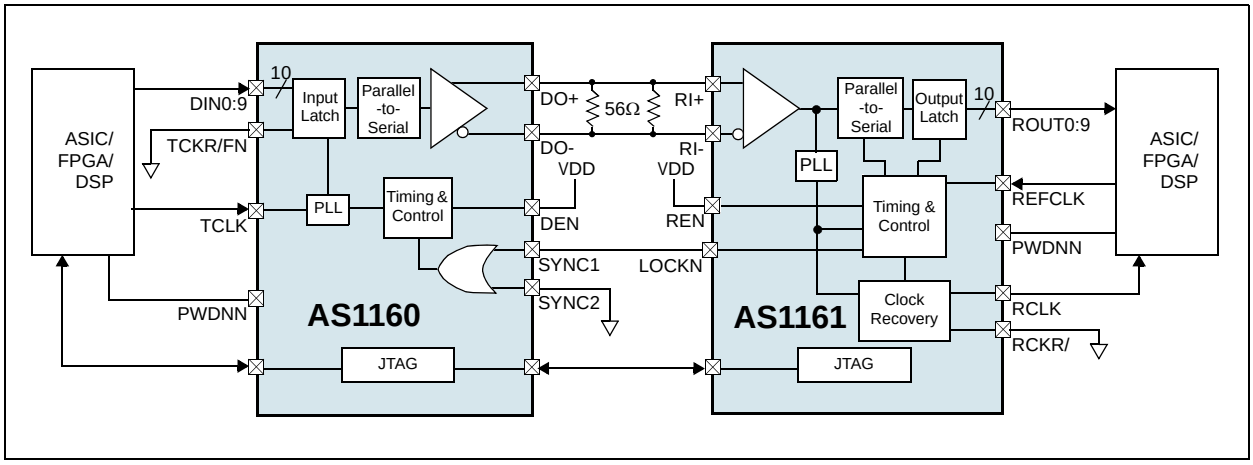
Transmitting Data

Once the serializer (AS1160) and deserializer (AS1161) are powered up, they must be phase locked to each other to transmit data. Phase locking occurs when the deserializer locks to incoming data or when the serializer sends patterns.

The serializer sends SYNCPATs whenever the SYNC1 or SYNC2 inputs are high. The LOCKN output of the deserializer remains high until it has locked to the incoming data stream. Connecting the LOCKN output of the deserializer to one of the SYNC inputs of the serializer will guarantee that enough SYNCPATs are sent to achieve deserializer lock (see Figure 36 on page 23).

As long as the deserializer LOCKN output is low, valid data is presented at the deserializer outputs (ROUT0:ROUT9), except for the specific case of loss of lock during transmission (see Lock Loss Recovery on page 23).

Figure 36. Typical Application



Noise Margin

The deserializer (AS1161) noise margin is the amount of input jitter (phase noise) that the deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

- Serializer: TCLK jitter, V_{DD} noise (noise bandwidth and out-of-band noise)
- Media: ISI (Inter Symbolic Interference), Large VCM shifts
- Deserializer: V_{DD} noise

Lock Loss Recovery

In the case where the deserializer (AS1161) loses lock during data transmission, up to 3 cycles of data that were previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 4 times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. Therefore, after the deserializer re-locks to the incoming data stream and the deserializer LOCKN pin goes low, at least three previous data cycles should be suspect for bit errors.

The deserializer can re-lock to the incoming data stream by making the serializer re-send SYNCPATs.

Hot Insertion

As all BLVDS devices the AS1161 is hot pluggable but you have to follow some rules.

Hot insertion should be performed with pins making contact in the following order:

- Ground pins
- V_{DD} pins
- I/O pins

Note: When removing the device, the pin groups should be removed in reverse order from insertion.

PCB Considerations

The serializer and deserializer should be placed as close to the PCB edge connector as possible. In multiple deserializer applications, the distance from the deserializer to the slot connector appears as a stub to the serializer driving the backplane traces. Longer stubs lower the impedance of the bus, increase the load on the serializer and lower the threshold margin at the deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the serializer bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.

For bus LVDS applications the LVTTL, LVCMOS and bus LVDS signals should be separated from each other to prevent coupling into the bus lines. This can be achieved by using a four-layer PCB where the power, ground and input/output signals are separated.

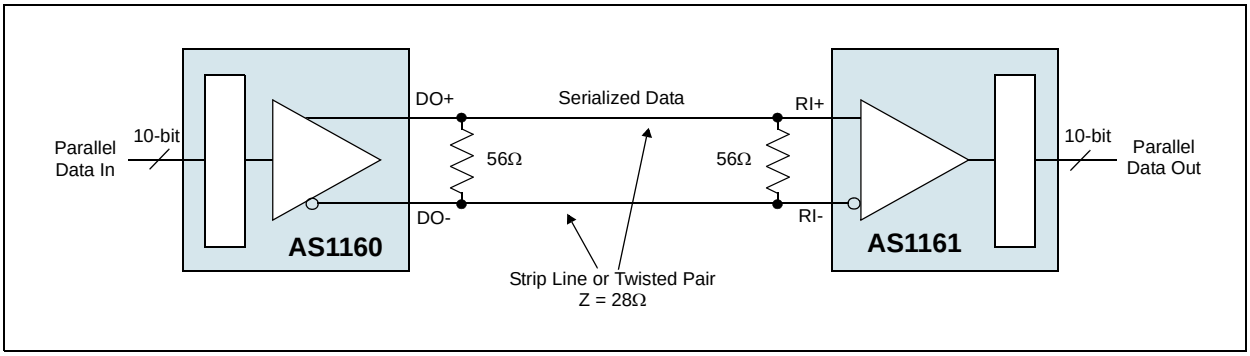
Transmission Media

The transmission line characteristics affect the performance of the AS1160/AS1161. It's recommended to use controlled-impedance media and to terminate at both ends of the transmission line (see Figure 37). Twisted pair cables should be used due to their superior signal quality and the less EMI generation. Noise which is picked up as common mode in the twisted pair is rejected by the differential receiver.

It's important to eliminate reflections and to run the differential traces as close together as possible to ensure that the noise is coupled as common mode. Also take care of matching the electrical length of the traces to prevent a degradation of the magnetic field cancellation. To avoid an external magnetic field, the differential output signals should also be placed as close together as possible.

The potential of offsetting the ground levels of the serializer vs. the deserializer must be considered. The bus LVDS provides a +1.2V common mode range at the receiver inputs.

Figure 37. Double-Terminated Point-to-Point



The serializer/deserializer chipset can be used in many different topologies. Such as multidrop configurations (see Figure 35 on page 20), through a PCB trace or through twisted pair cable (see Figure 37).

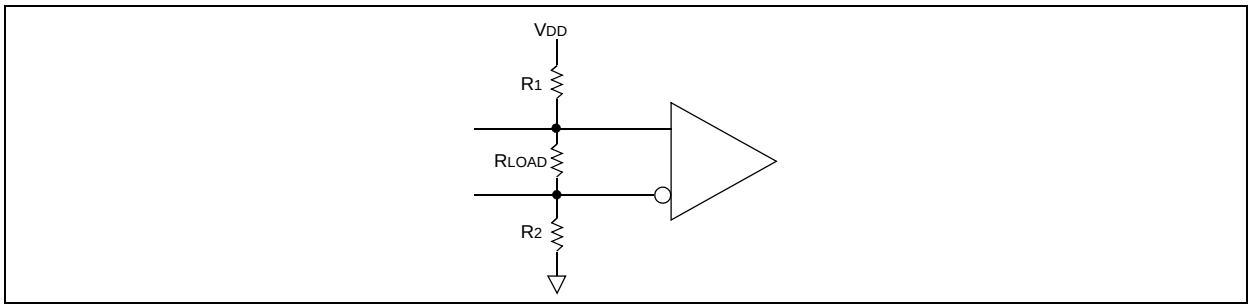
In point-to-point configurations, it's possible to terminated the transmission line only once at the receiver end. With only one termination the reflections and the differential signal swing are larger compared to a double termination.

Failsafe Biasing

The AS1161 has an input threshold sensitivity of ±75mV, which allows a greater differential noise margin.

However, in cases where the receiver input is not being actively driven, the increased sensitivity of the AS1161 can pickup noise as a signal and cause unintentional locking (e.g., when the input cable is left floating).

Figure 38. Failsafe Biasing Setup



External resistors can be added to the receiver circuit to prevent noise pickup as shown in Figure 38. In such circuits, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. The pull-up and pull-down resistors (R_1 and R_2 in Figure 38) provide a current path through the termination resistor (R_{LOAD}) which biases the receiver inputs when they are not connected to an active driver.

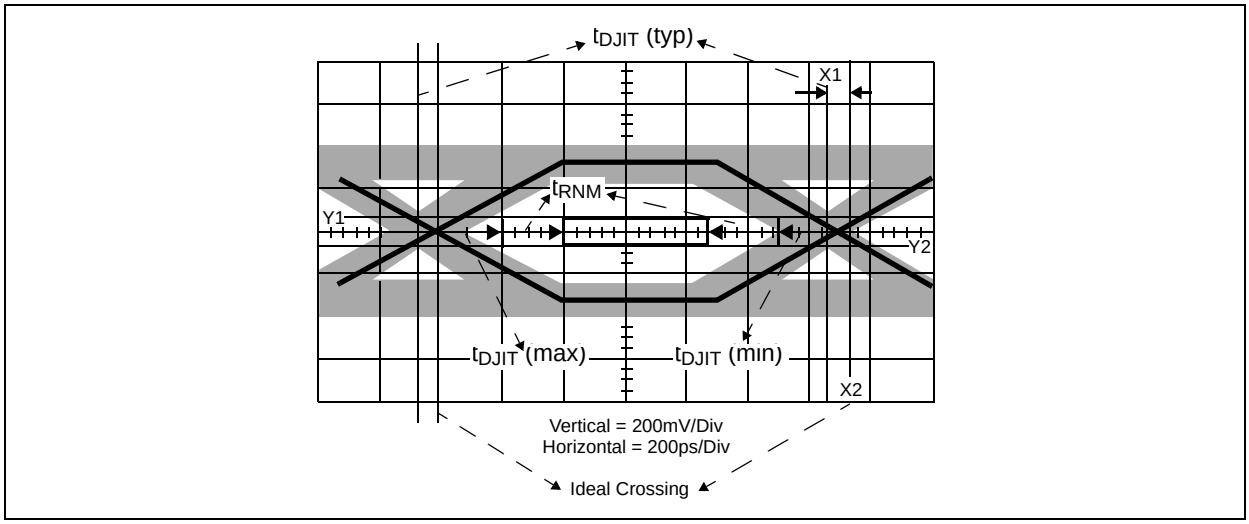
Note: The value of the pull-up and pull-down resistors should be chosen so that sufficient current is drawn to provide a +15mV drop across the termination resistor.

Signal Integrity

For a validation of the signal qualitiy in an application or in a simulation, the parameters t_{DJIT} and t_{RNM} can be used to generate an eye pattern mask.

t_{DJIT} measures the transmitter's ability to place data bits in the ideal position to be sampled by the receiver. The typical t_{DJIT} parameter of 50ps @ 66MHz indicates that the crossing point of the Tx data is 50ps before the ideal crossing point. The $t_{DJITMIN}$ and $t_{DJITMAX}$ parameters specify the earliest and latest time that a crossing will occur relative to the ideal position.

Figure 39. Eye Pattern Mask Generation and Signal Quality Validation



First of all, t_{RNM} is calculated by measuring how much of the bit the receiver needs to ensure correct sampling. This calculated amount is subtracted from the ideal bit and what's left of it is available for external sources of noise and is called t_{RNM}. It is the offset from t_{DJIT} for the test mask within the eye opening.

The vertical limits of the mask are determined by the AS1161 receiver input threshold of ±75mV.

JTAG Test Modes

Instructions supported by the AS1160/AS1161 and its respective operational binary codes are shown in Table 12.

Note: Boundary Scan Description Language (BSDL) model files for the AS1160 and the AS1161 are available on the internet.

Table 12. Instruction Codes

Instruction	Code
SAMPLE/PRELOAD	0101
BYPASS	1111
EXTEST	0001
IDCODE	1010
RUNBIST	1110

SAMPLE/PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification that supports two functions. The digital I/Os of the device can be sampled at the boundary scan test data register without interfering with the normal operation of the device. SAMPLE/PRELOAD also allows the device to shift data into the boundary scantest data register through TDI.

BYPASS

When the BYPASS instruction is latched into the instruction register, TDI connects to TDO through the 1-bit bypass test data register. This allows data to pass from TDI to TDO without affecting the device's normal operation.

EXTEST

Implemented at LVDS levels as a go/no-go test (e.g. missing cables).

IDCODE

The AS1160/AS1161 ID code is provided to the TDO output.

Table 13. 32bit ID Code

	MSB			LSB
Device	**Version (4bits)**	**Device ID (16bits)**	**Manufacturer ID (11bits)**	**Fixed Value (1bit)**
AS1160	0100	0001000101100000	01011011010	1
AS1161	0100	0001000101100001	01011011010	1

RUNBIST

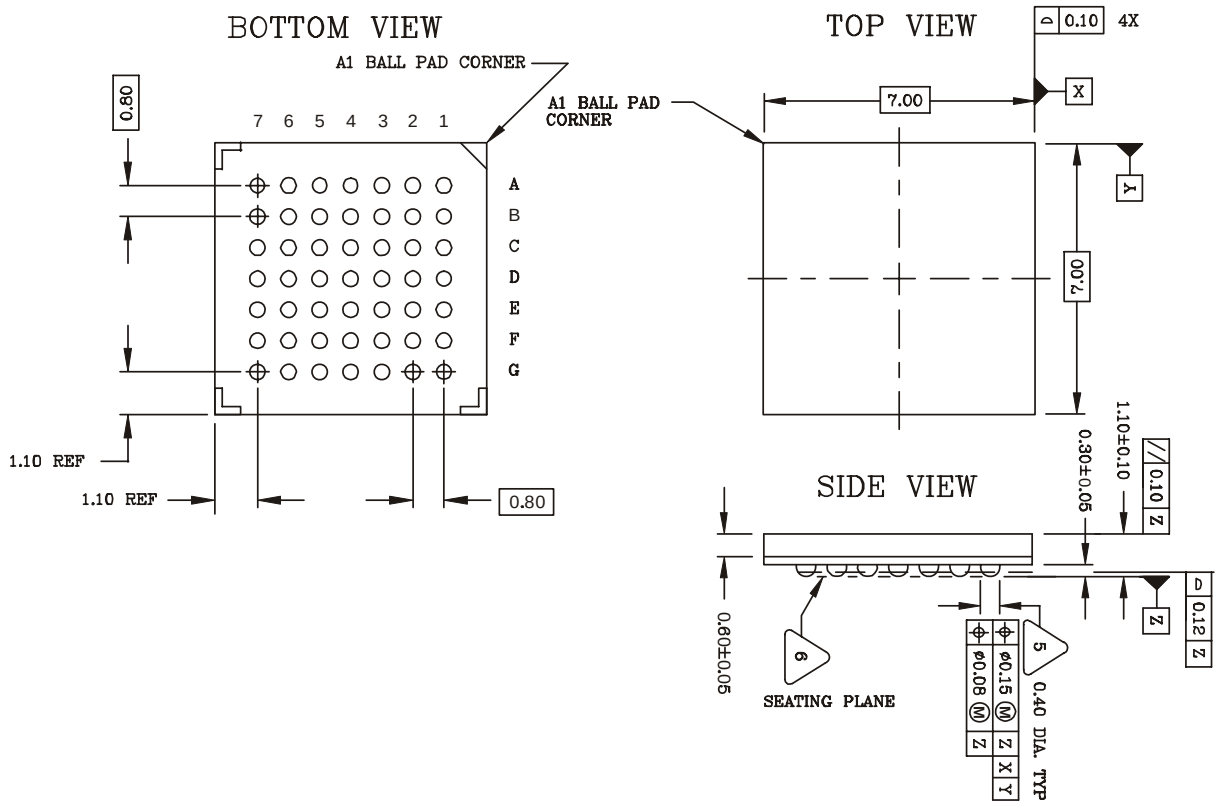
An at-system-speed interconnect test instruction. It is executed in approximately 33mS (@ 66MHz system speed). There are two bits in the RX BIST data register for notification of PASS/FAIL and TEST_COMPLETE. Pass indicates that the BER (bit-error-rate) is better than 10^{-7}.

If both the AS1160 and the AS1161 have loaded the RUNBIST instruction into their instruction registers, both devices must move into the RTI state within 4K system clocks (at a SCLK of 66Mhz and TCK of 1MHz this allows for 66 TCK cycles). This is only an issue when both devices are not on the same scan chain or LSP, although, it can be a problem with some multi-drop devices.

12 Package Drawings and Markings

The device is available in an CTBGA 49-bumps package.

Figure 40. CTBGA 49-bumps Package



13 Ordering Information

The devices are available as the standard products shown in Table 14.

Table 14. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS1160-BCTT	Serializer	Tape and Reel	CTBGA 49-bumps
AS1161-BCTT	Deserializer	Tape and Reel	CTBGA 49-bumps

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

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