

AS1152 Quad LVDS Driver

Data Sheet

1 General Description

The AS1152 is a Quad Flow-Through LVDS (Low-Voltage Differential Signaling) Line Driver which accepts and converts LVTTTL/LVCMOS input levels into LVDS output signals. The device is perfect for low-power low-noise applications requiring high signaling rates and reduced EMI emissions.

The device is guaranteed to transmit data at speeds up to 500Mbps (250MHz) over controlled impedance media of approximately 100Ω. Supported transmission media are PCB traces, backplanes, and cables.

The AS1152 is capable of setting all four outputs to a high-impedance state through two Enable Inputs (EN and ENn – internally pulled down to GND), dropping the device to an ultra-low-power state of 16mW (typical) during high impedance. The Enable Inputs are common to all four drivers.

Outputs conform to the *ANSI TIA/EIA-644 LVDS* standards. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVTTTL/LVCMOS inputs and LVDS outputs.

The AS1152 operates from a single +3.3V supply and is specified for operation from -40 to +85°C.

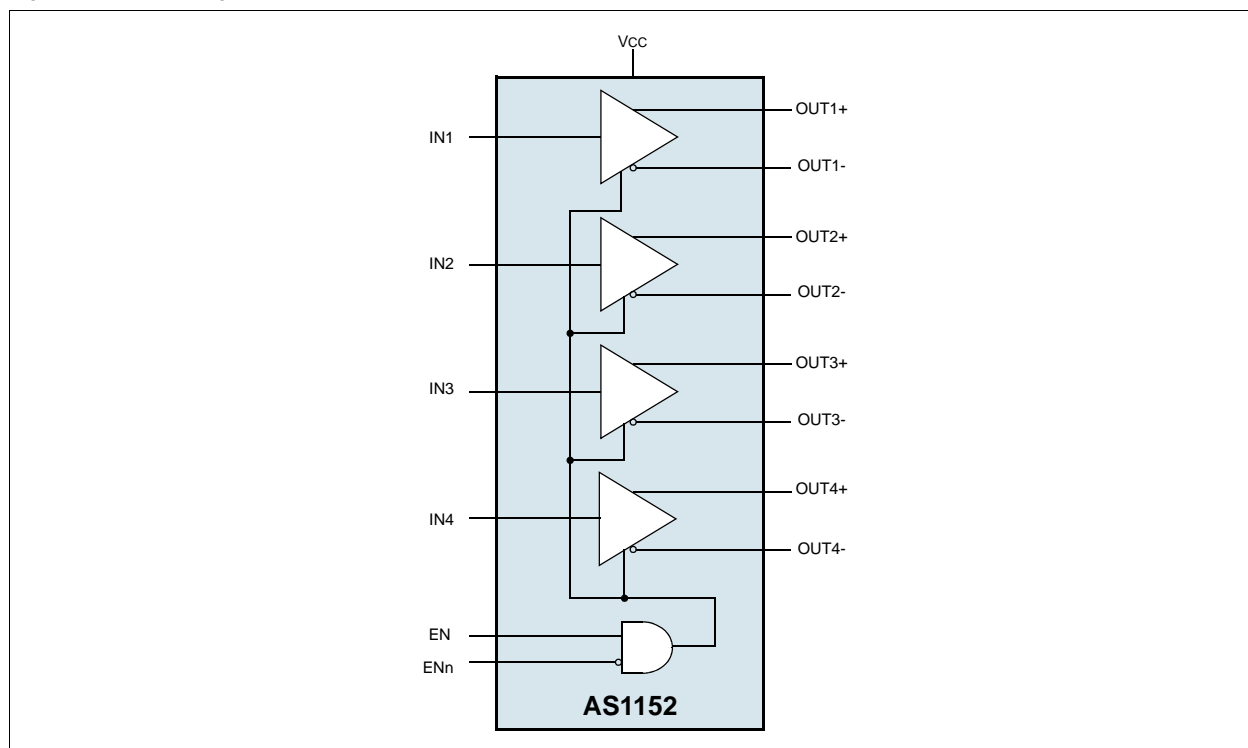
2 Key Features

- Flow-Through Pinout
- Guaranteed 500Mbps Data Rate (paired with AS1150)
- 350ps Pulse Skew (Max)
- Conforms to *ANSI TIA/EIA-644* LVDS Standards
- Single +3.3V Supply
- Operating Temperature Range: -40 to +85°C
- 16-Pin TSSOP Package

3 Applications

Digital Copiers, Laser Printers, Cellular Phone Base Stations, Add/Drop Muxes, Digital Cross-Connects, DSLAMs, Network Switches/Routers, Backplane Interconnect, Clock Distribution Computers, Intelligent Instruments, Controllers, Critical Microprocessors and Microcontrollers, Power Monitoring, and Portable/Battery-Powered Equipment.

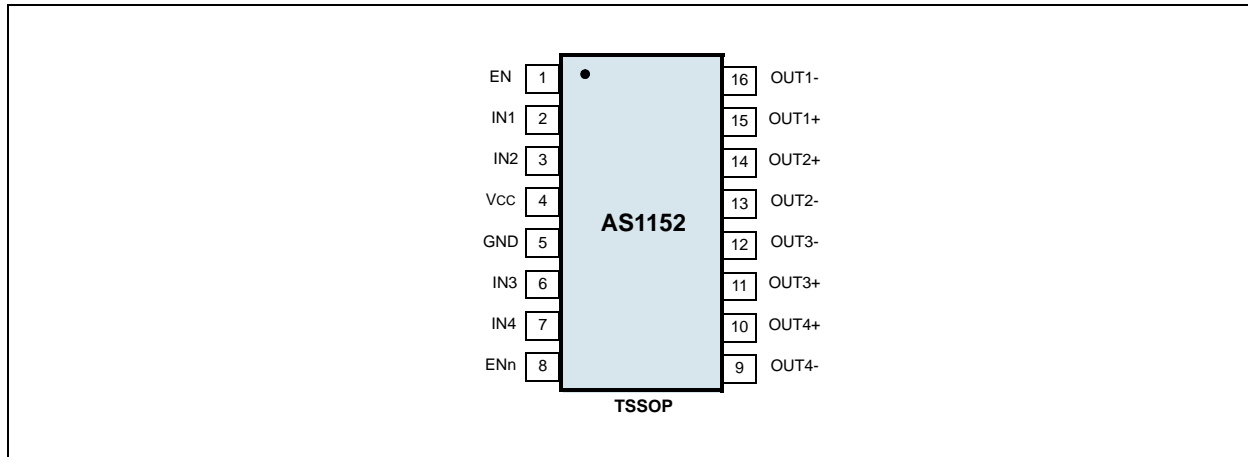
Figure 1. Block Diagram



4 Pinout

Pin Assignments

Figure 2. AS1152 Pin Assignments (Top View)



Pin Descriptions

Table 1. AS1152 Pin Descriptions

Pin Number	Pin Name	Description
1	EN	Driver Enable Input. Internally pulled down to GND. When EN = high and ENn = low or open, the driver outputs are active. For other combinations of EN and ENn, the outputs are disabled and in high impedance.
2	IN1	LVTTL/LVCMOS Driver Input
3	IN2	LVTTL/LVCMOS Driver Input
4	Vcc	Power Supply Input. Bypass Vcc to GND with 0.1μF and 0.001μF ceramic capacitors.
5	GND	Ground
6	IN3	LVTTL/LVCMOS Driver Input
7	IN4	LVTTL/LVCMOS Driver Input
8	ENn	Driver Enable Input. Internally pulled down to GND. When EN = high and ENn = low or open, the driver outputs are active. For other combinations of EN and ENn, the outputs are disabled and in high impedance.
9	OUT4-	Inverting LVDS Driver Output
10	OUT4+	Noninverting LVDS Driver Output
11	OUT3+	Noninverting LVDS Driver Output
12	OUT3-	Inverting LVDS Driver Output
13	OUT2-	Inverting LVDS Driver Output
14	OUT2+	Noninverting LVDS Driver Output
15	OUT1+	Noninverting LVDS Driver Output
16	OUT1-	Inverting LVDS Driver Output

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Limits	Units	Notes
V _{CC} to GND	-0.3 to +5.0	V	
IN _x , EN, EN _n to GND	-0.3 to (V _{CC} + 0.3)	V	
OUT _{x+} , OUT _{x-} to GND	-0.3 to +5	V	
Short Circuit Duration (OUT _{x+} , OUT _{x-})	Continuous		
Continuous Power Dissipation (T _A = +70°C)	755	mW	Derate 9.4mW/°C Above +70°C
Storage Temperature Range	-65 to +150	°C	
Maximum Junction Temperature	+150	°C	
Operating Temperature Range	-40 to +85	°C	
Package Body Temperature	260	°C	The reflow peak soldering temperature (body temperature) specified is in compliance with IPC/JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".
ESD Protection	±4	kV	Human Body Model, IN _x , OUT _{x+} , OUT _{x-}

6 Electrical Characteristics

DC Electrical Characteristics

($V_{CC} = +3.0$ to $+3.6V$, $T_A = -40$ to $+85^\circ C$, $R_L = 100\Omega$, $f \leq 150MHz$)

Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, Unless Otherwise Noted.)^{1, 2}

Table 3. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVDS Output (OUTx+, OUTx-)						
Differential Output Voltage	VOD	Figure 20 on page 12	250	370	450	mV
Change in Magnitude of VOD Between Complementary Output States	ΔVOD	Figure 20 on page 12		1	35	mV
Offset Voltage	VOS	Figure 20 on page 12	1.125	1.25	1.375	V
Change in Magnitude of Vos Between Complementary Output States	ΔVOS	Figure 20 on page 12		4	25	mV
Output High Voltage	VOH				1.6	V
Output Low Voltage	VOL		0.90			V
Differential Output Short-Circuit Current ³	IOSD	Enabled, VOD = 0			-9	mA
Output Short-Circuit Current	IOS	OUTx+ = 0 at INx = VCC or OUTx- = 0 at INx = 0, enabled		-3.8	-9	mA
Output High-Impedance Current	IOZ	EN = low and ENn = high, OUTx+ = 0 or VCC, OUTx- = 0 or VCC, $R_L = \infty$	-10		10	μA
Power-Off Output Current	IOFF	$V_{CC} = 0$ or open, OUTx+ = 0 or 3.6V, OUTx- = 0 or 3.6V, $R_L = \infty$	-20		20	μA
Inputs (INx, EN, ENn)						
High-Level Input Voltage	VIH		2.0		VCC	V
Low-Level Input Voltage	VIL		GND		0.8	V
Input Current	IIN	INx, EN, ENn = 0 or VCC	-20		20	μA
Supply Current						
No-Load Supply Current	ICC	$R_L = \infty$, INx = VCC or 0 for all channels		4	6	mA
Loaded Supply Current	ICCL	$R_L = 100\Omega$, INx = VCC or 0 for all channels		18	25	mA
Disabled Supply Current	ICCZ	Disabled, INx = VCC or 0 for all channels, EN = 0, ENn = VCC		3.5	5.5	mA

Notes:

1. Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at $T_A = +25^\circ C$.
2. Currents into the device are positive, and current out of the device is negative. All voltages are referenced to ground except VOD.
3. Guaranteed by correlation data.

Switching Characteristics

($V_{CC} = +3.0$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, $f \leq 150MHz$, $T_A = -40$ to $+85^\circ C$)

Typical values are at $V_{CC} = +3.3V$, $T_A = +25^\circ C$, Unless Otherwise Noted.) 1, 2, 3

Table 4. Switching Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Propagation Delay, High-to-Low	tPHLD	Figure 18 on page 11 and Figure 19 on page 11	1.1		1.7	ns
Differential Propagation Delay, Low-to-High	tPLHD	Figure 18 on page 11 and Figure 19 on page 11	1.1		1.7	ns
Differential Pulse Skew ⁴	tsKD1	Figure 18 on page 11 and Figure 19 on page 11		0.04	0.35	ns
Differential Channel-to-Channel Skew ⁵	tsKD2	Figure 18 on page 11 and Figure 19 on page 11		0.07	0.60	ns
Differential Part-to-Part Skew ⁶	tsKD3	Figure 18 on page 11 and Figure 19 on page 11		0.13	0.8	ns
Differential Part-to-Part Skew ⁷	tsKD4	Figure 18 on page 11 and Figure 19 on page 11		0.43	1.0	ns
Rise Time	tTLH	Figure 18 on page 11 and Figure 19 on page 11	0.2	0.39	2.6	ns
Fall Time	tTHL	Figure 18 on page 11 and Figure 19 on page 11	0.2	0.39	2.6	ns
Disable Time, High-to-Z	tPHZ	Figure 21 on page 12 and Figure 22 on page 12		3	4	ns
Disable Time, Low-to-Z	tPLZ	Figure 21 on page 12 and Figure 22 on page 12		3	4	ns
Enable Time, Z-to-High	tPZH	Figure 21 on page 12 and Figure 22 on page 12		2	3	ns
Enable Time, Z-to-Low	tPZL	Figure 21 on page 12 and Figure 22 on page 12		2	3	ns
Maximum Operating Frequency ^{8, 9}	fMAX		250			MHz

Notes:

- Parameters are guaranteed by design and characterization.
- CL includes probe and jig capacitance.
- Signal generator conditions for dynamic tests: $V_{OL} = 0$, $V_{OH} = 3V$, $f = 100MHz$, 50% duty cycle, $R_O = 50\Omega$, $t_R \leq 1ns$, $t_F \leq 1ns$ (0 to 100%).
- tsKD1 is the magnitude difference of differential propagation delay. $tsKD1 = |tPHLD - tPLHD|$.
- tsKD2 is the magnitude difference of tPHLD or tPLHD of one channel to the tPHLD or tPLHD of another channel on the same device.
- tsKD3 is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within $5^\circ C$ of each other.
- tsKD4 is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.
- fMAX signal generator conditions: $V_{OL} = 0$, $V_{OH} = 3V$, 50% duty cycle, $R_O = 50\Omega$, $t_R \leq 1ns$, $t_F \leq 1ns$ (0 to 100%).
- Conforms to ANSI TIA/EIA 644 LVDS Standards $\leq 150MHz$. Maximum operating frequency of 250MHz is possible using an AS1150 receiver.

7 Typical Operating Characteristics

$V_{CC} = +3.3V$, $V_{CM} = +1.2V$, $|V_{D}| = 0.2V$, $C_{LOAD} = 15pF$, $T_{amb} = +25^{\circ}C$, unless otherwise noted

Figure 3. Output High Voltage vs. V_{CC}

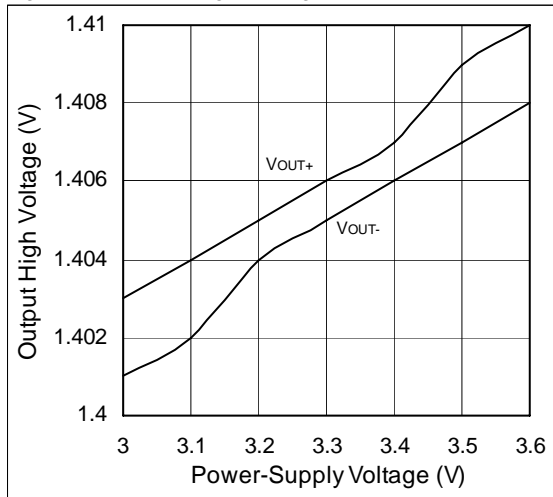


Figure 4. Output Low Voltage vs. V_{CC}

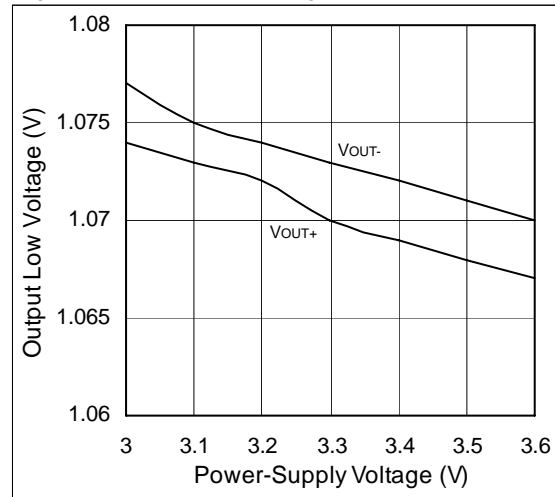


Figure 5. Output Short-Circuit Current vs. V_{CC} ; $V_{IN} = V_{CC}$ or GND

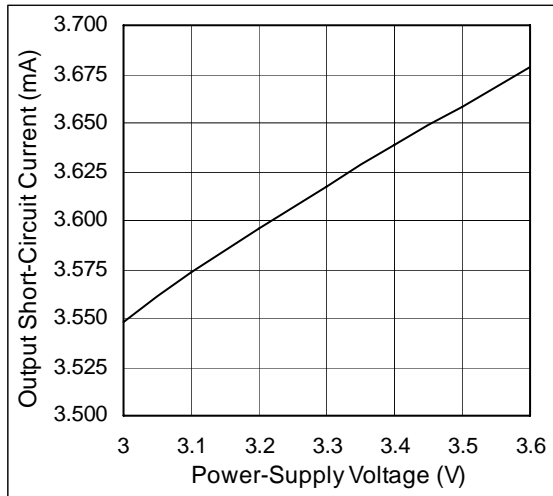


Figure 6. Output High-Impedance State Current vs. V_{CC} ; $V_{IN} = V_{CC}$ or GND

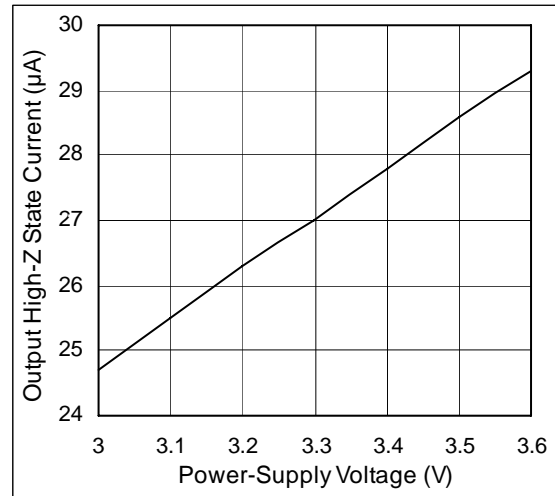


Figure 7. Differential Output Voltage vs. Vcc

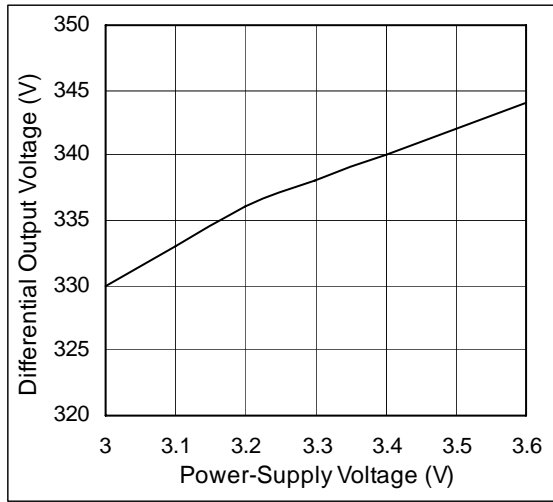


Figure 8. Differential Output Voltage vs. Load Resistor

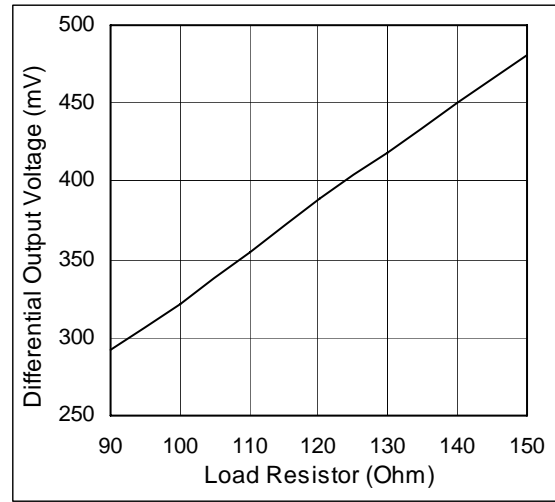


Figure 9. Offset Voltage vs. Vcc

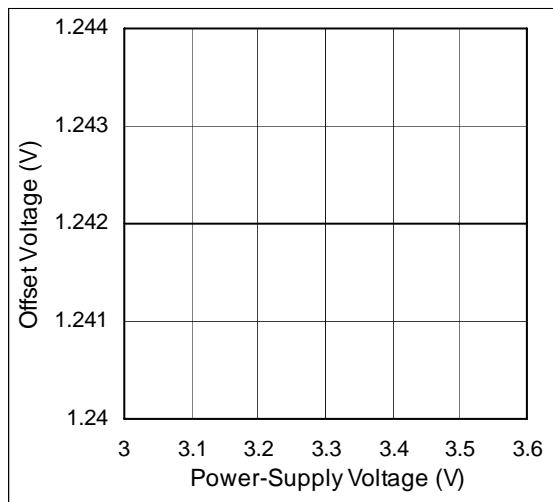


Figure 10. Power Supply Current vs. Frequency; VIN = 0 to 3V

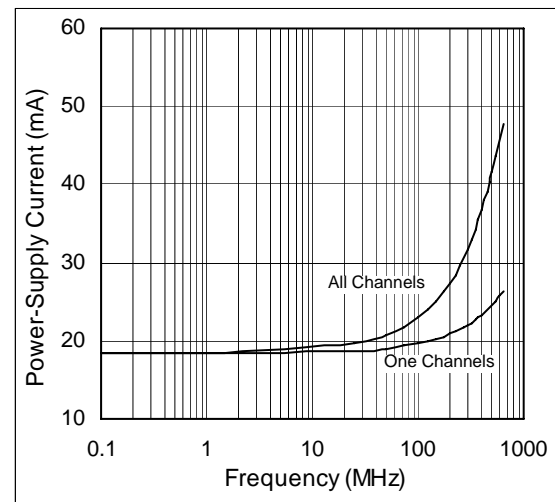


Figure 11. Icc vs. Vcc; Freq = 1MHz

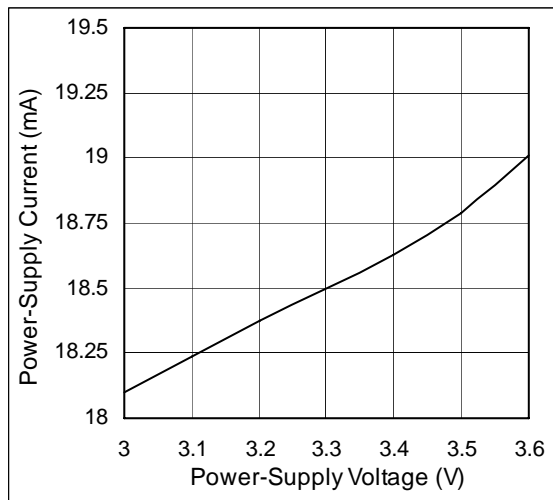


Figure 12. Icc vs. Temperature; Freq = 1MHz

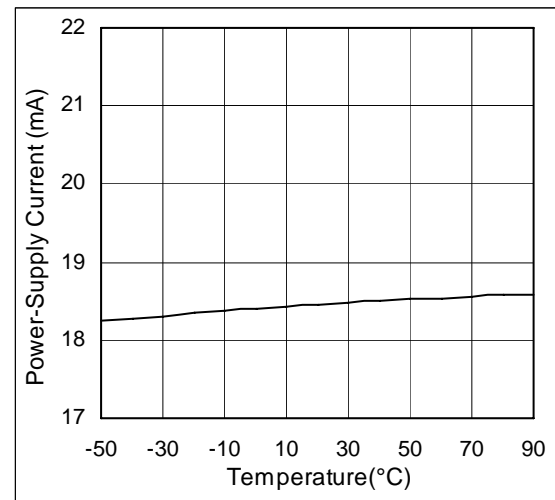


Figure 13. Differential Propagation Delay vs. Vcc; Freq = 1MHz

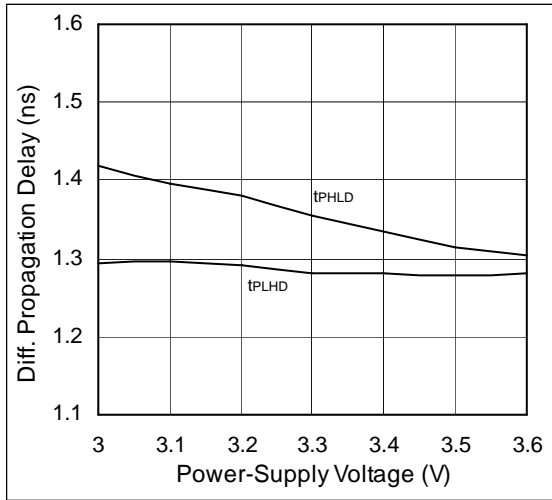


Figure 14. Differential Propagation Delay vs. Temperature; Freq = 1MHz

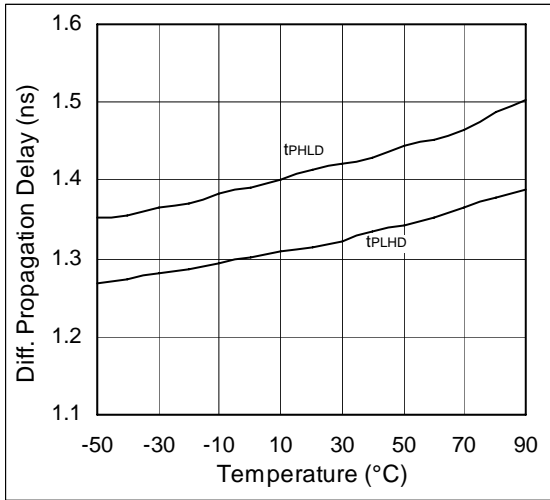


Figure 15. Differential Skew vs. Vcc; Freq = 1MHz

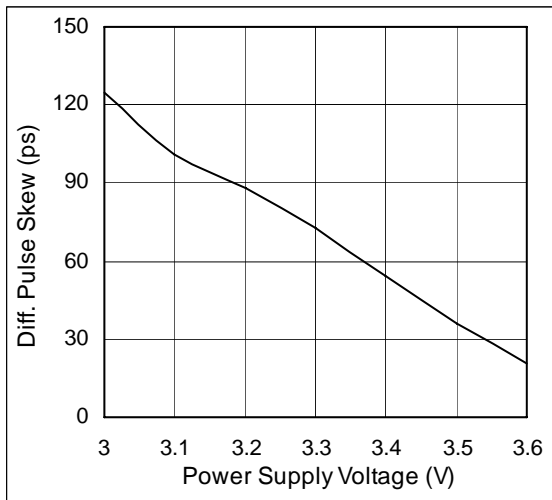
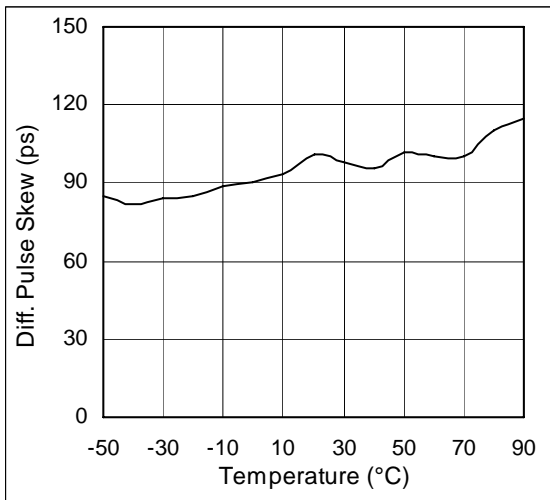


Figure 16. Differential Skew vs. Temperature; Freq = 1MHz



8 Detailed Description

LVDS Interface

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the *ANSI/TIA/EIA-644* and *IEEE 1596.3* standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The AS1152 is an 500Mbps quad differential LVDS driver that is designed for high-speed, point-to-point, low-power applications. This device accepts LVTTTL/LVCMOS input levels and translates them to LVDS output signals.

The AS1152 generates a 2.5mA to 4.5mA output current using a current-steering configuration. This current steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited, and enter a high-impedance state when the device is not powered or is disabled.

The current-steering architecture of the AS1152 requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor at the input of an LVDS receiver (AS1150, AS1151). Logic states are determined by the direction of current flow through the termination resistor.

With a typical 3.7mA output current, the AS1152 produces an output voltage of 370mV when driving a 100Ω load.

Note: The AS1152 is conform to the ANSI TIA/EIA 644 LVDS Standards when operating ≤ 150 MHz. Paired with the AS1150 the datarate can be increased to 500Mbps. While operating faster than 150MHz, the rise and fall time, as well as the setup and hold time are not conform to the ANSI TIA/EIA 644 LVDS Standards.

Termination

Because the AS1152 is a current-steering device, no output voltage will be generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels depend upon the value of the termination resistor.

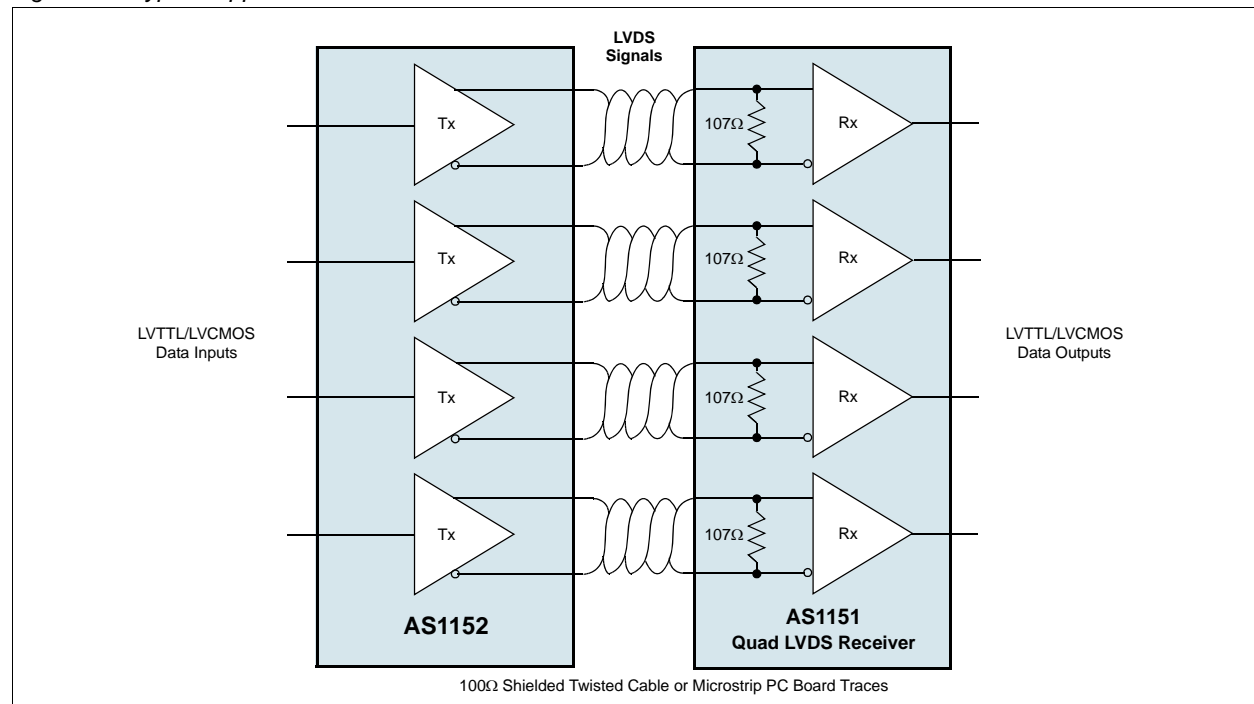
The AS1152 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90 and 132Ω, depending on the characteristic impedance of the transmission medium.

9 Applications

Table 5. Function Table

Enable Pins		Input		Output
EN	ENn	INx+	INx-	OUTx
H	L or Open	L	L	H
H	L or Open	H	H	L
Other Combinations of Enable Pin Settings		Don't Care	Z	Z

Figure 17. Typical Application Circuit



Power-Supply Bypassing

To bypass V_{CC} , use high-frequency surface-mount ceramic $0.1\mu\text{F}$ and $0.001\mu\text{F}$ capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to pin V_{CC} .

Differential Traces

Input trace characteristics can adversely affect the performance of the AS1152.

- Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor is also matched to this characteristic impedance.
- Eliminate reflections and ensure that noise couples as common mode by running the differential traces near each other.
- Reduce skew by using matched trace lengths. Tight skew control is required to minimize emissions and proper data recovery of the devices.
- Route each channel's differential signals very close to each other for optimal cancellation of their respective external magnetic fields. Use a constant distance between the differential traces to avoid irregularities in differential impedance.
- Avoid 90° turns (use two 45° turns).
- Minimize the number of vias to further prevent impedance irregularities.

Cables and Connectors

Supported transmission media include printed circuit board traces, backplanes, and cables.

- Use cables and connectors with matched differential impedance (typically 100Ω) to minimize impedance mismatches.
- Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.
- Avoid the use of unbalanced cables such as ribbon cable or simple coaxial cable.

Board Layout

The device should be placed as close to the interface connector as possible to minimize LVDS trace length.

- Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.
- Use a four-layer PCB that provides separate power, ground, LVDS signals, and input signals.
- Isolate the input LVDS signals from each other and the output LVCMOS/LVTTL signals from each other to prevent coupling.
- Separate the input LVDS signals from the output signals planes with the power and ground planes for best results.

Figure 18. Driver Propagation Delay and Transition Time Waveforms

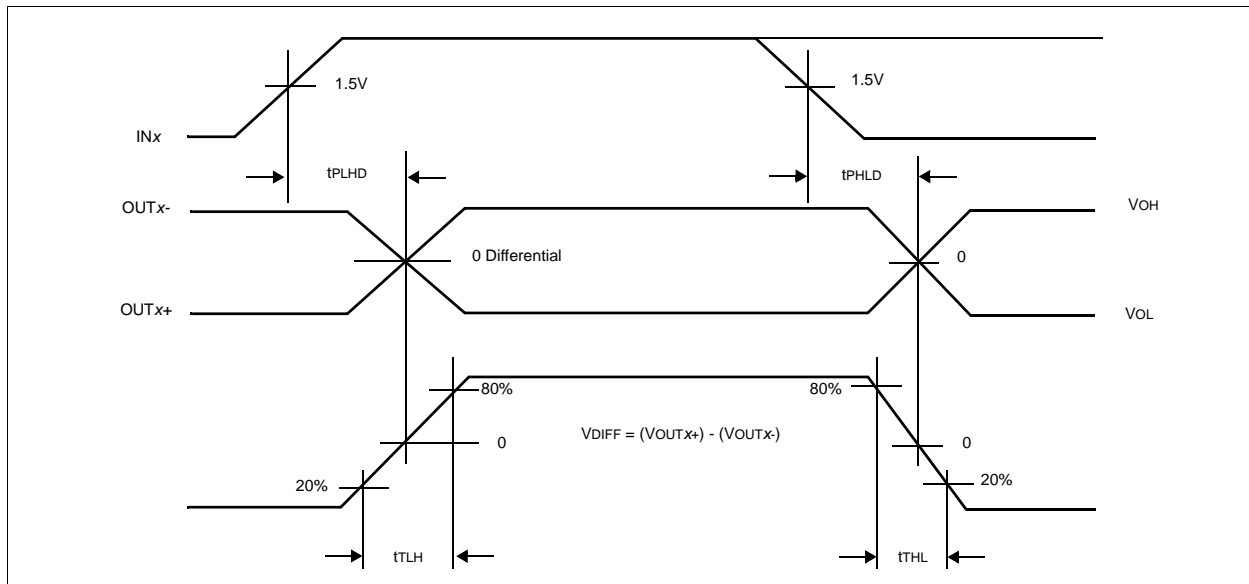


Figure 19. Driver Propagation Delay and Transition Time Test Circuit

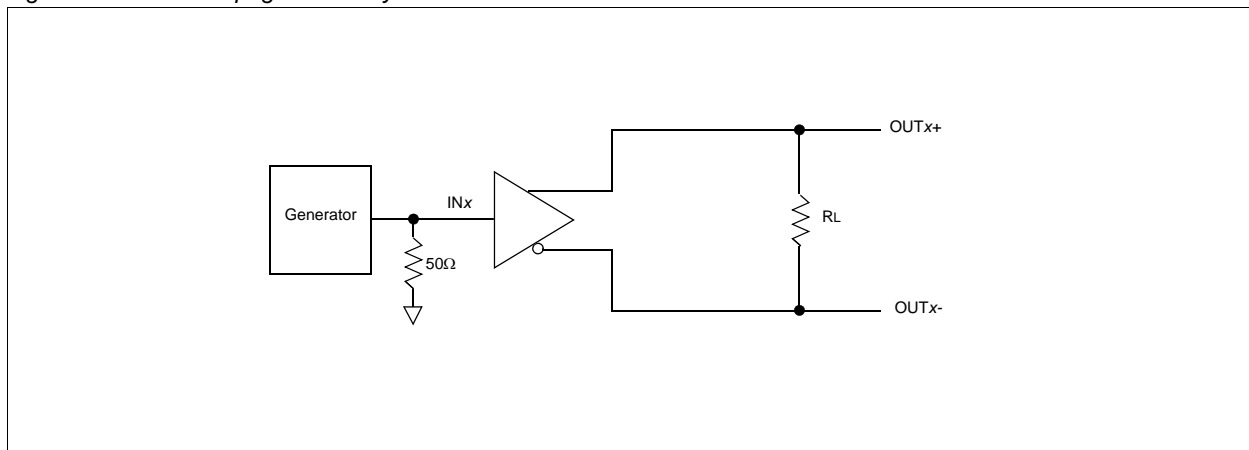


Figure 20. Driver V_{OD} and V_{OS} Test Circuit

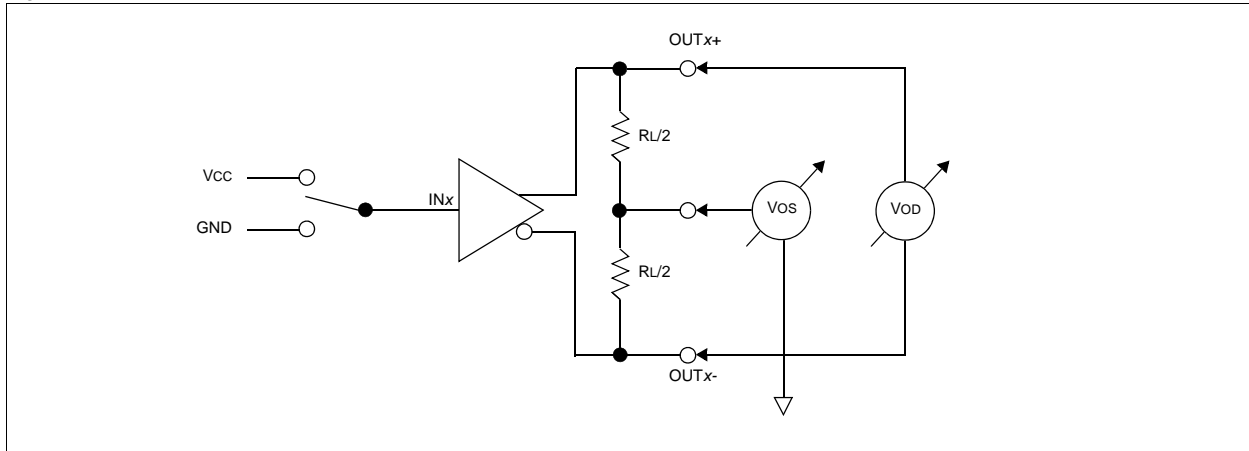


Figure 21. Driver High Impedance Delay Waveforms

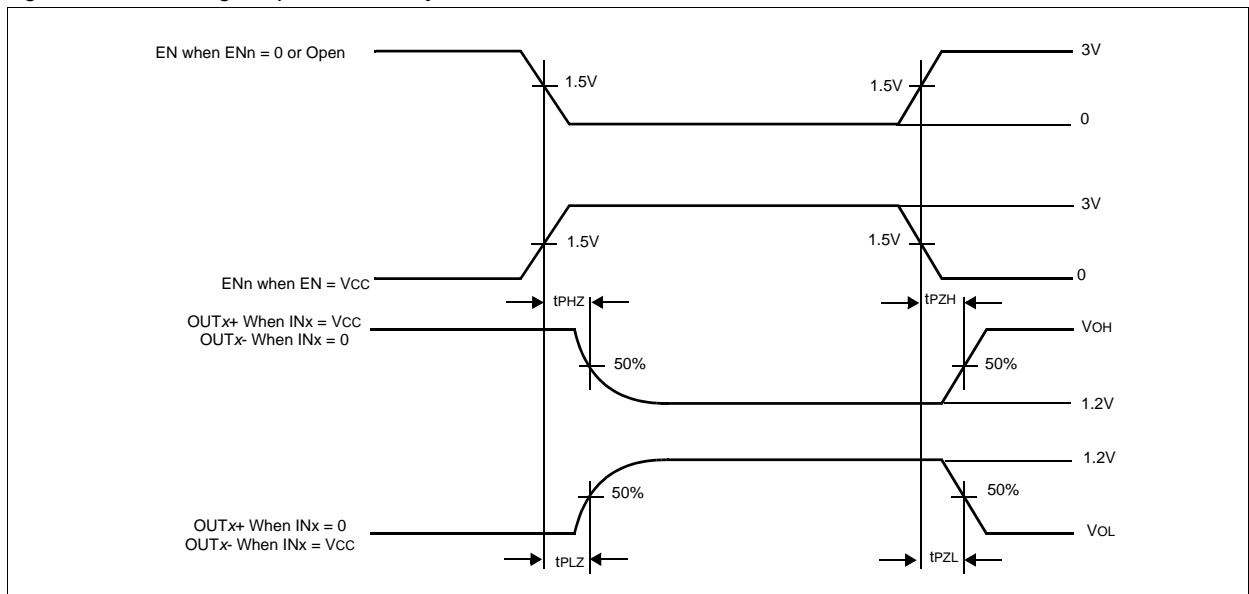
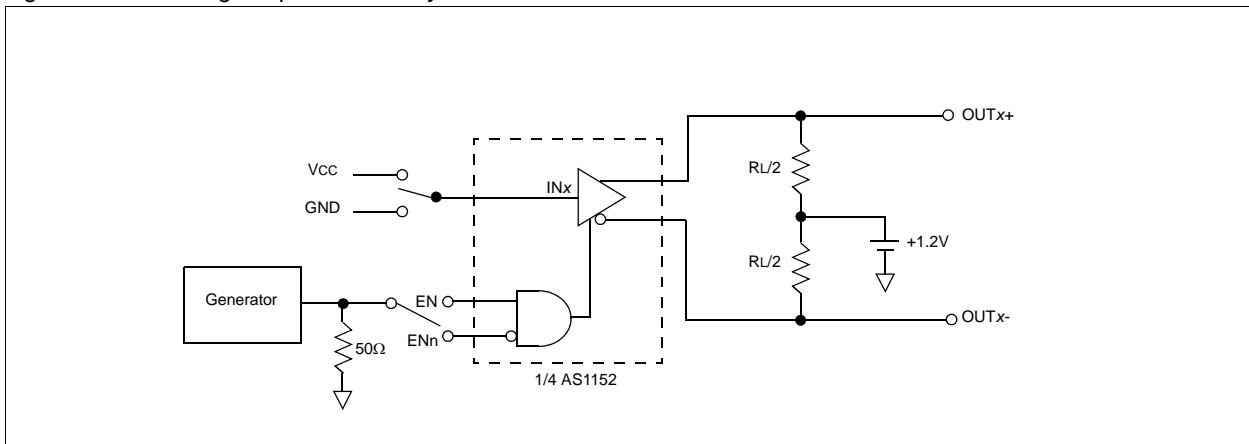
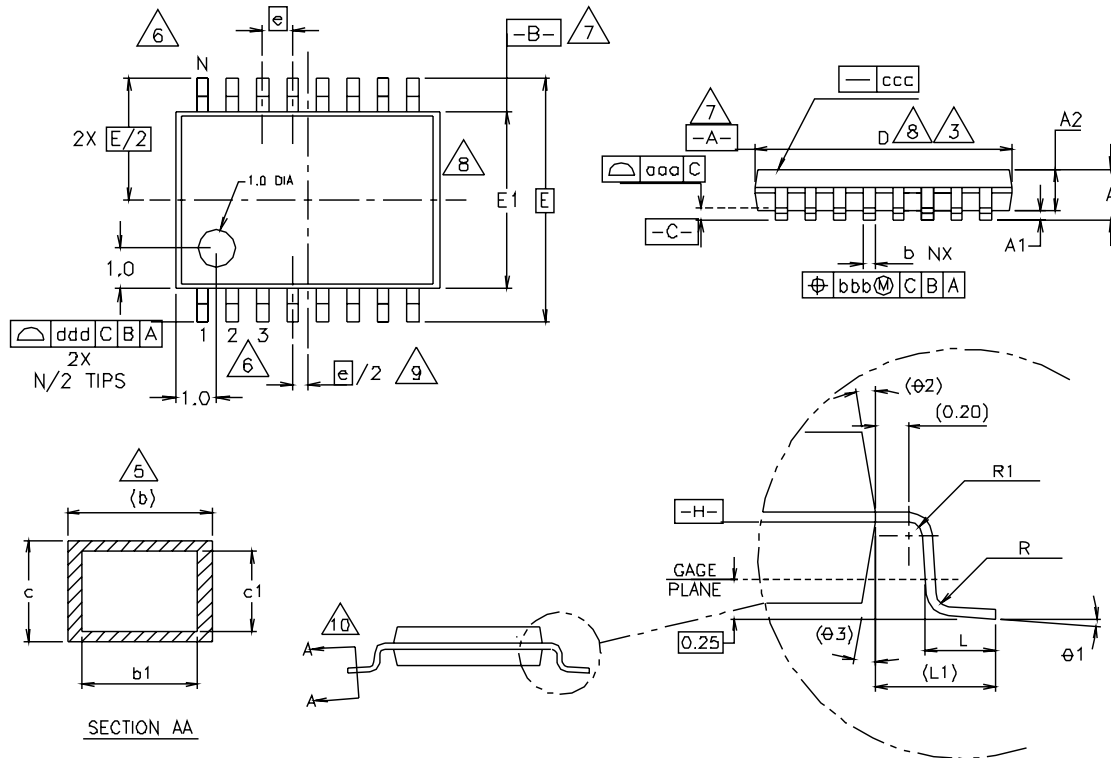


Figure 22. Driver High-Impedance Delay Test Circuit



10 Package Drawings and Markings

Figure 23. 16-pin TSSOP Package



Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensioning and tolerancing per ASME Y14.5M – 1994.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
6. Terminal numbers are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 are to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

Symbol	Min	Typ	Max	Notes
A	-	-	1.10	1,2
A1	0.05	-	0.15	1,2
A2	0.85	0.90	0.95	1,2
L	0.50	0.60	0.75	1,2
R	0.09	-	-	1,2
R1	0.09	-	-	1,2
b	0.19	-	0.30	1,2,5
b1	0.19	0.22	0.25	1,2
c	0.09	-	0.20	1,2
c1	0.09	-	0.16	1,2
theta 1	0°	-	8°	1,2
L1	1.0REF			1,2
aaa	0.10			1,2
bbb	0.10			1,2
ccc	0.05			1,2
ddd	0.20			1,2
e	0.65BSC			1,2
theta 2	12°REF			1,2
theta 3	12°REF			1,2
Variations				
D	4.90	5.00	5.10	1,2,3,8
E1	4.30	4.40	4.50	1,2,4,8
E	6.4BSC			1,2
e	0.65BSC			1,2
N	16			1,2,6

11 Ordering Information

Part Number	Description	Package Type	Delivery Form
AS1152	Quad low-voltage differential signaling driver	16-pin TSSOP	Tube
AS1152-T	Quad low-voltage differential signaling driver	16-pin TSSOP	Tape and Reel

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