BLF8G20LS-140V; BLF8G20LS-140GV

Power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 1805 MHz to 1990 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1805 to 1880	900	28	35	18.5	32	–30 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; 5 MHz carrier spacing.

1.2 Features and benefits

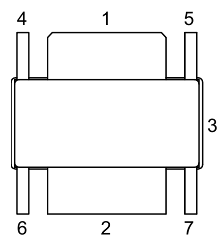
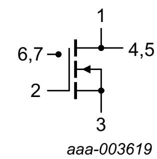
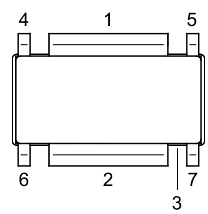
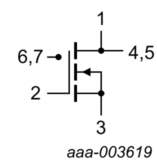
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth (150 MHz typical)
- Designed for broadband operation (1805 MHz to 1990 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1990 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G20LS-140V (SOT1244B)			
1	drain		
2	gate		
3	source [1]		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		
BLF8G20LS-140GV (SOT1244C)			
1	drain		
2	gate		
3	source [1]		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G20LS-140V	-	earless flanged ceramic package; 6 leads	SOT1244B
BLF8G20LS-140GV	-	earless flanged ceramic package; 6 leads	SOT1244C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 35 W	0.4	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.5	1.8	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 900 mA	1.6	2	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	33	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	-	13.35	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	-	0.08	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; 3GPP test model 1 with 64 DPCH; PAR = 8.4 dB at 0.01 % probability on the CCDF; f_1 = 1807.5 MHz; f_2 = 1812.5 MHz; f_3 = 1872.5 MHz; f_4 = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C; unless otherwise specified; in a water cooled AB test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 35 W	17.3	18.5	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 35 W	28	32	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 35 W	-	–17	–10	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 35 W	-	–30	–25	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G20LS-140V and BLF8G20LS-140GV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 900 mA; P_L = 140 W (CW); f = 1800 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data; I_{Dq} = 900 mA; V_{DS} = 28 V.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)
BLF8G20LS-140V		
1805	1.71 – 3.75j	1.5 – 3.7j
1840	2.01 – 4.01j	1.4 – 3.8j
1880	2.35 – 4.08j	1.5 – 3.8j
1930	2.62 – 4.45j	1.6 – 3.9j
1960	3.13 – 4.87j	1.4 – 3.8j
1990	3.93 – 4.54j	1.3 – 3.9j
BLF8G20LS-140GV		
1805	1.71 – 5.75j	1.5 – 5.7j
1840	2.01 – 6.01j	1.4 – 5.8j
1880	2.35 – 6.08j	1.5 – 5.8j
1930	1.62 – 6.45j	1.6 – 5.9j
1960	3.13 – 6.87j	1.4 – 5.8j
1990	3.93 – 6.54j	1.3 – 5.9j

[1] Z_S and Z_L defined in Figure 1.

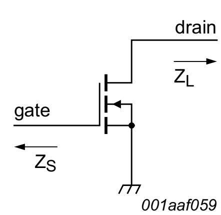
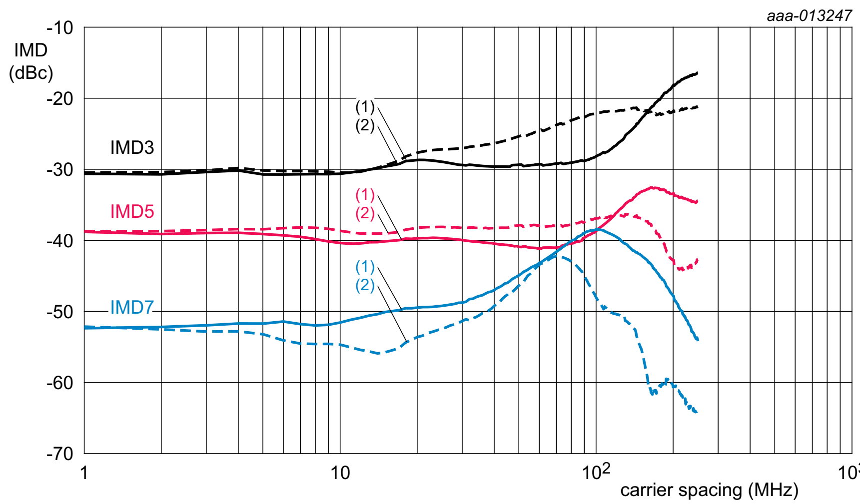


Fig 1. Definition of transistor impedance

7.3 VBW in a class-AB operation

The BLF8G20LS-140V and BLF8G20LS-140GV show 150 MHz (typical) video bandwidth (IMD third-order intermodulation inflection point) in a class-AB test circuit in the 1805 MHz to 1880 MHz band at V_{DS} = 28 V and I_{Dq} = 900 mA.



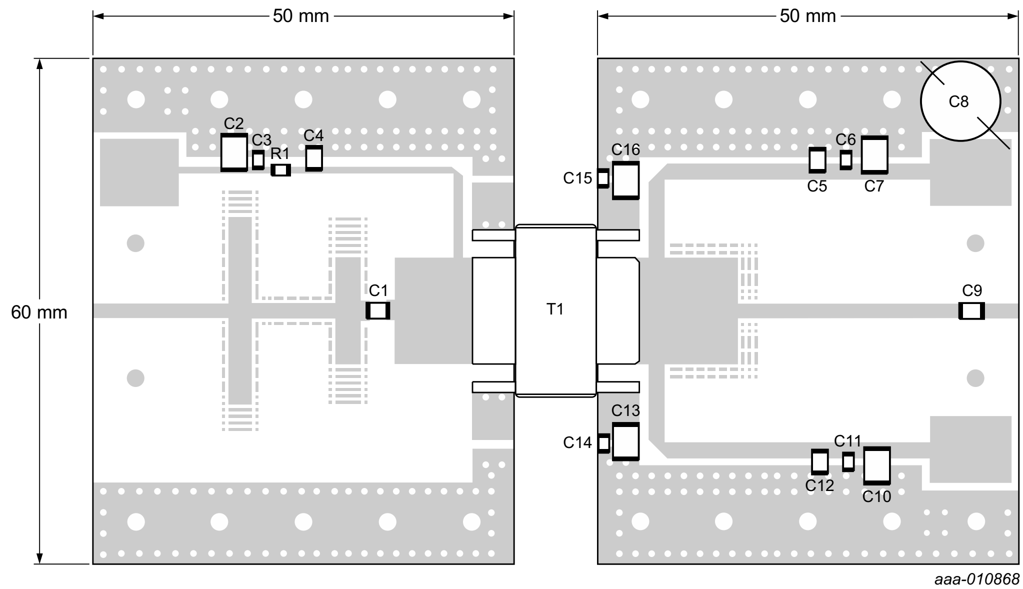
V_{DS} = 28 V; I_{Dq} = 900 mA; R_1 = 10 Ω.

(1) low

(2) high

Fig 2. VBW capacity in class-AB test circuit

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B with a thickness of 0.76 mm. See Table 9 for a list of components.

Fig 3. Component layout

Table 9. List of components

See Figure 3 for component layout.

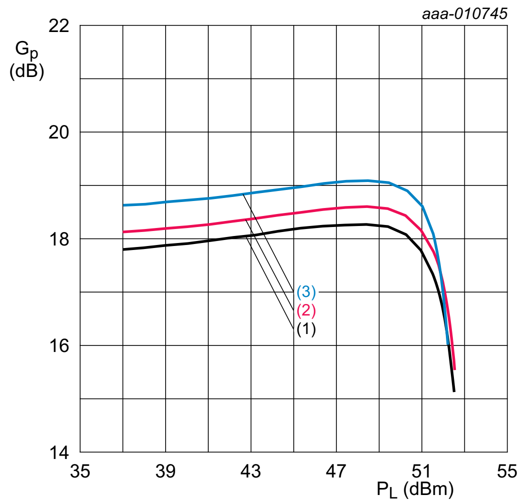
Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	1.2 pF	[1]	ATC 800B
C2	multilayer ceramic chip capacitor	1 μF	[2]	Murata
C3	multilayer ceramic chip capacitor	100 nF	[2]	Murata
C4, C9	multilayer ceramic chip capacitor	12 pF	[1]	ATC 800B
C5, C12	multilayer ceramic chip capacitor	20 pF	[1]	ATC 800B
C6, C11	multilayer ceramic chip capacitor	220 nF	[2]	Murata
C7, C10, C13, C16	multilayer ceramic chip capacitor	4.7 μF, 50 V	[2]	Murata
C8	electrolytic capacitor	> 470 μF, 63 V		
C14, C15	multilayer ceramic chip capacitor	-		not mounted
R1	chip resistor	4.7 Ω, 1 % tolerance		SMD 0805
T1	transistor	-		Ampleon BLF8G20LS-140V

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Murata or capacitor of same quality.

7.5 Graphical data

7.5.1 Pulsed CW



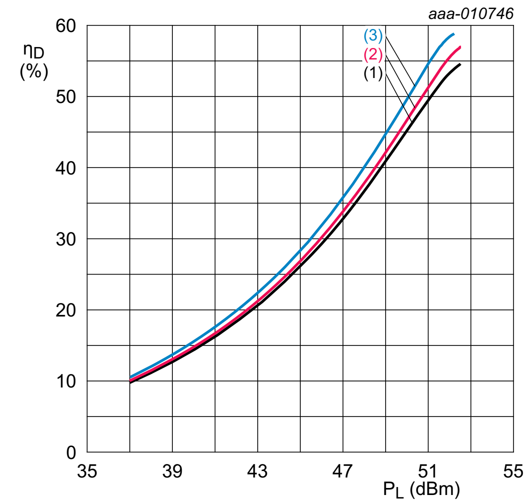
V_{DS} = 28 V; I_{Dq} = 900 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1805 MHz

(2) f = 1840 MHz

(3) f = 1880 MHz

Fig 4. Power gain as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 900 mA; t_p = 100 μs; δ = 10 %.

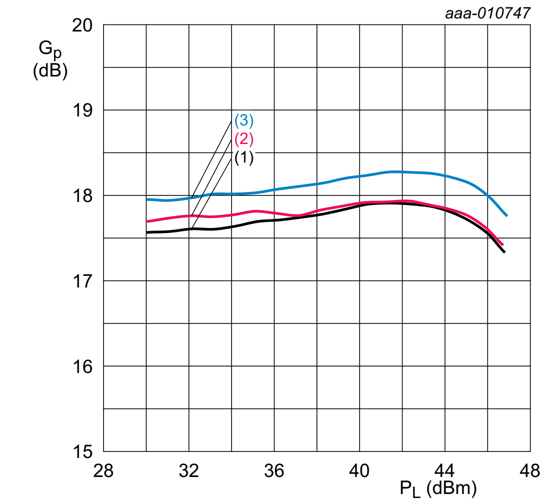
(1) f = 1805 MHz

(2) f = 1840 MHz

(3) f = 1880 MHz

Fig 5. Drain efficiency as a function of out power; typical values

7.5.2 IS-95



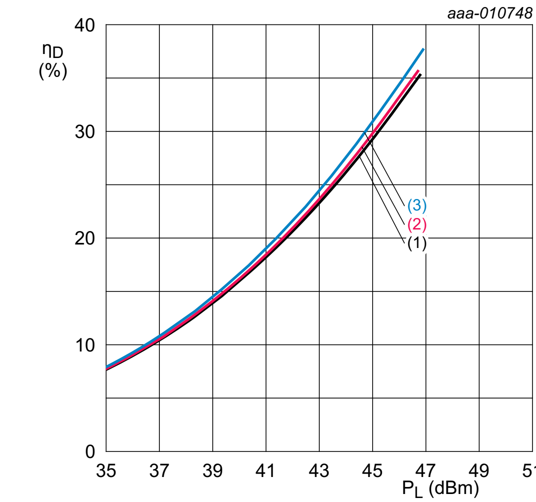
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 6. Power gain as a function of output power; typical values



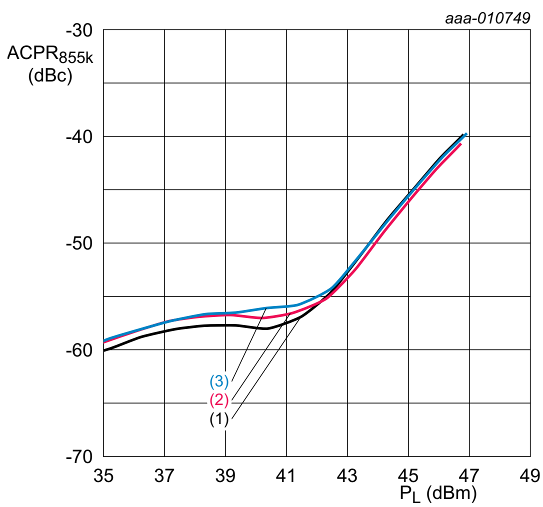
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 7. Drain efficiency as a function of output power; typical values



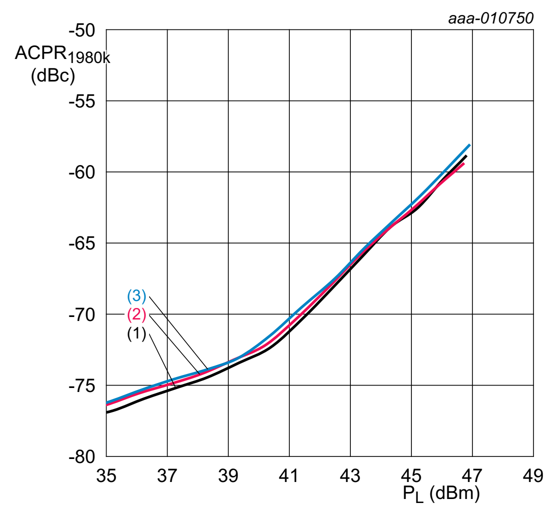
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 8. Adjacent channel power ratio (885 kHz) as a function of output power; typical values



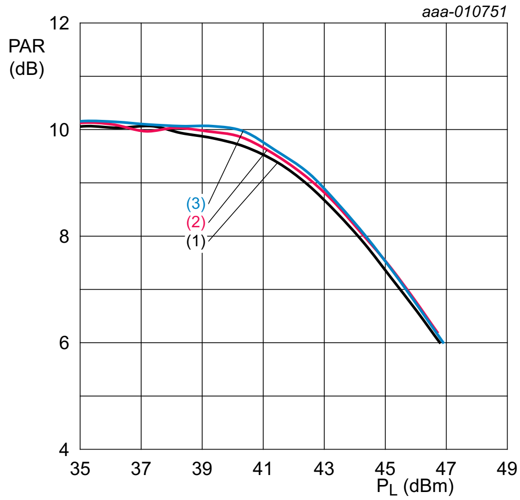
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 9. Adjacent channel power ratio (1980 kHz) as a function of output power; typical values



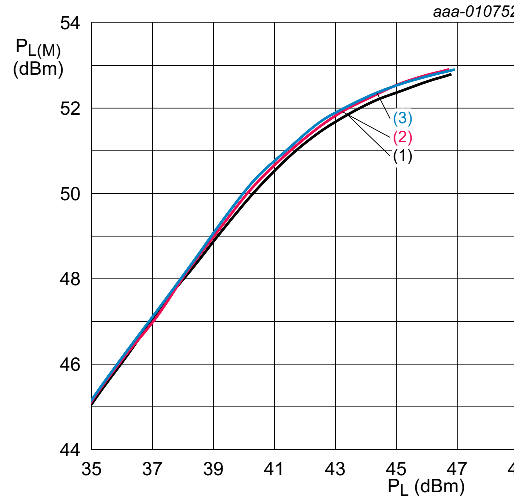
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 10. Peak-to-average ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 900 mA.

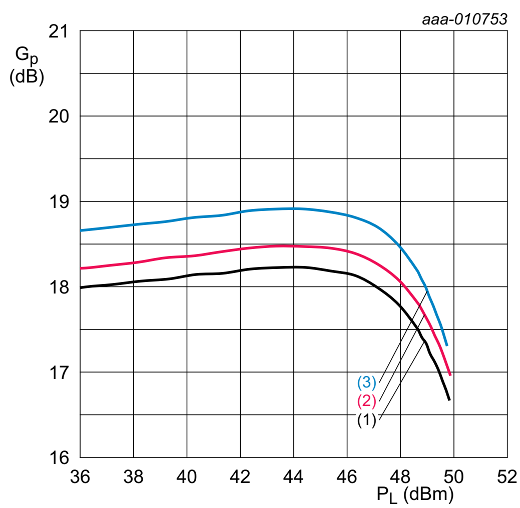
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 11. Peak output power as a function of output power; typical values

7.5.3 1-Carrier W-CDMA



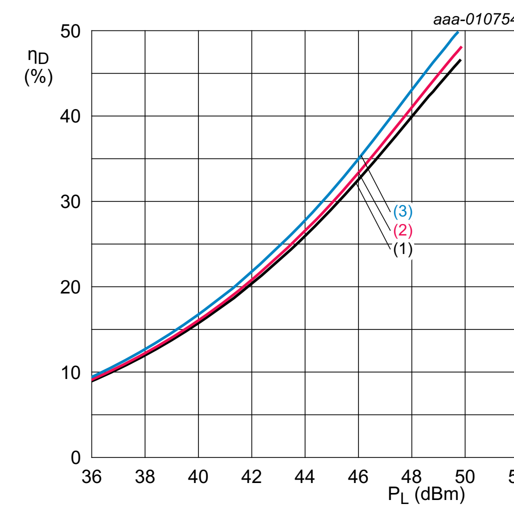
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 12. Power gain as a function of output power; typical values



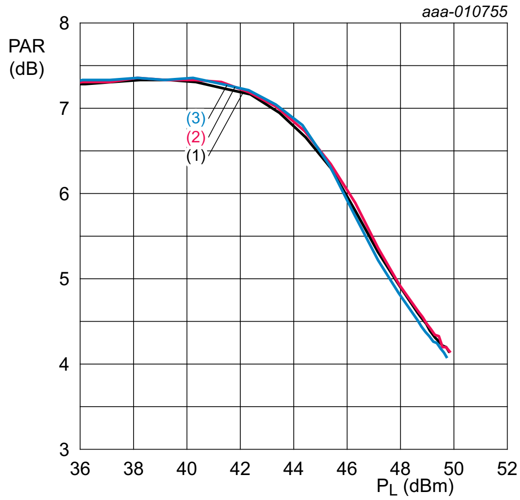
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 13. Drain efficiency as a function of output power; typical values



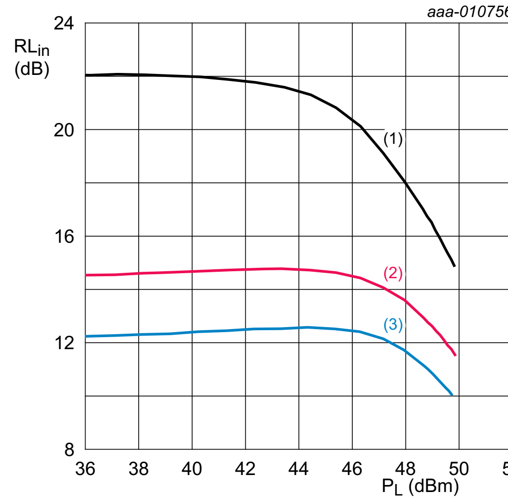
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 14. Peak-to-average ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 900 mA.

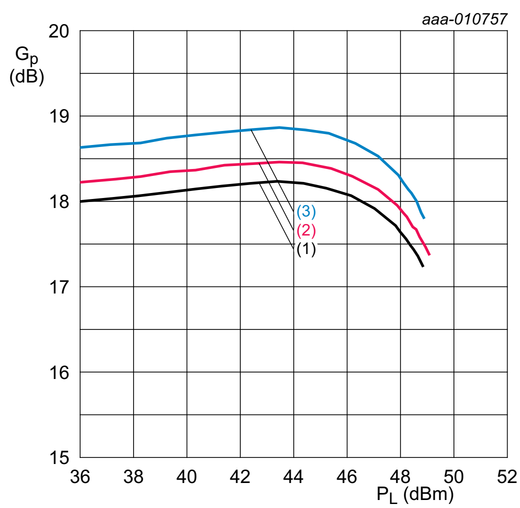
(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 15. Input return loss as a function of output power; typical values

7.5.4 2-Carrier W-CDMA



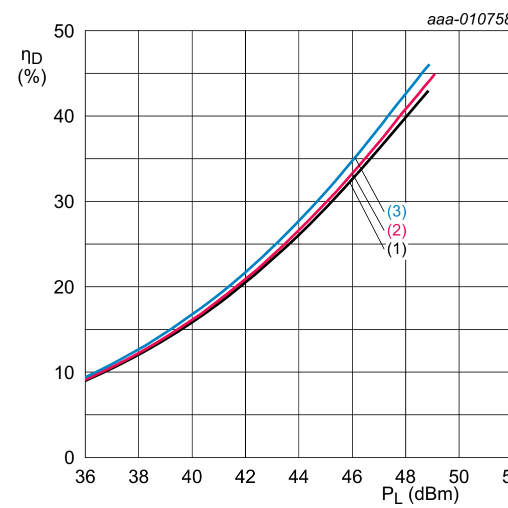
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 16. Power gain as a function of output power; typical values



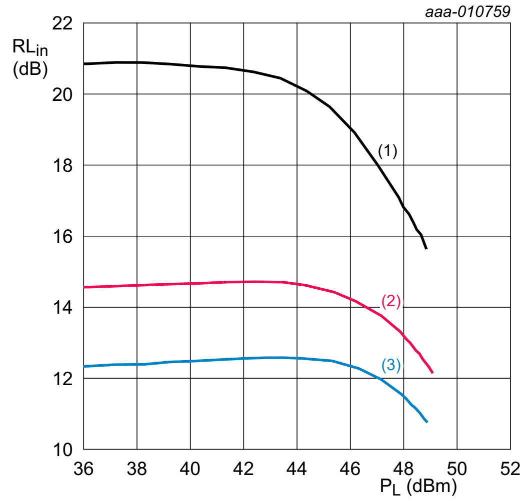
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 17. Drain efficiency as a function of output power; typical values



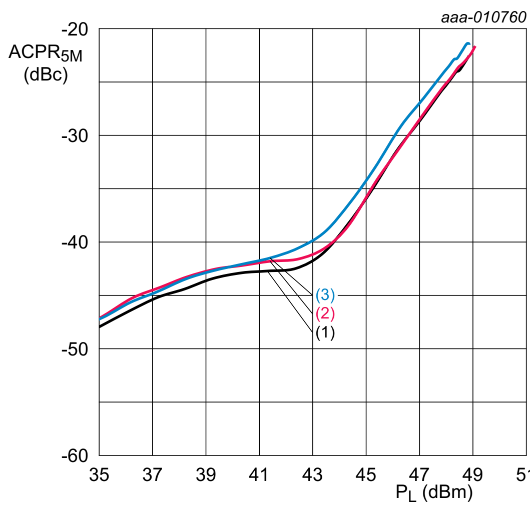
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 18. Input return loss as a function of output power; typical values



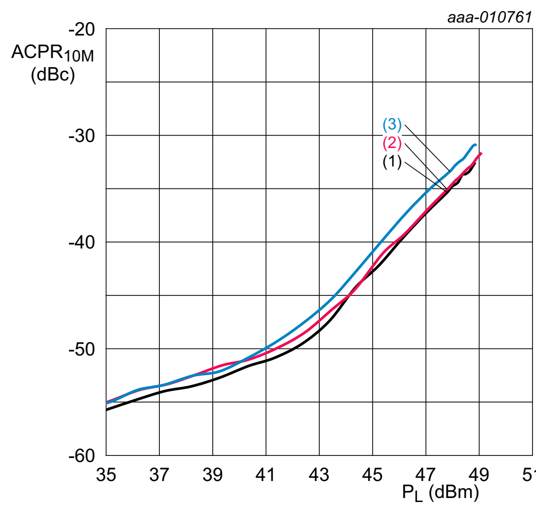
V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 19. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 900 mA.

(1) f = 1810 MHz

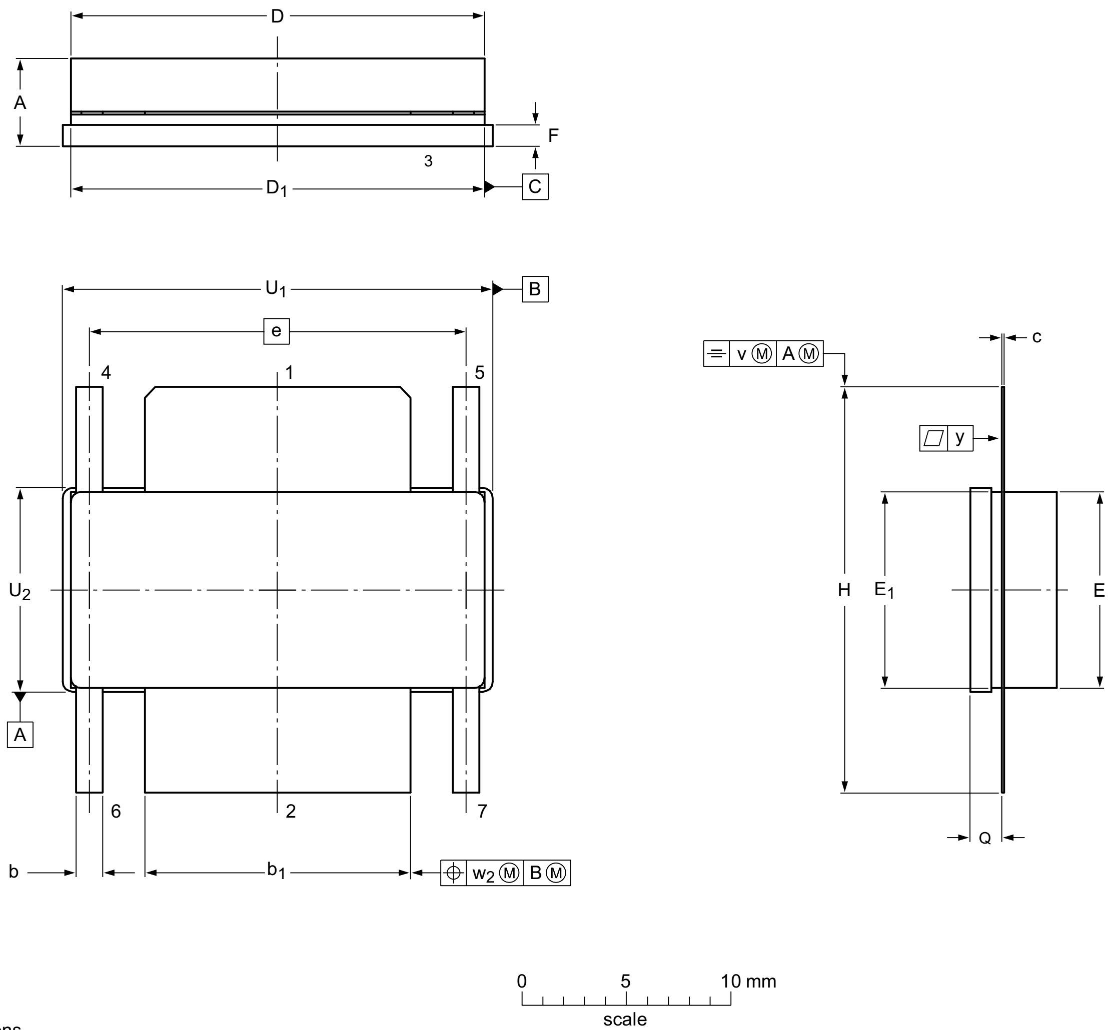
(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 20. Adjacent channel power ratio (10 MHz) as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 6 leads **SOT1244B**



Dimensions

Unit(1)		A	b	b_1	c	D	D_1	e	E	E_1	F	H	Q(2)	U_1	U_2	v	w_2	y
mm	max	4.75	1.41	12.83	0.18	20.02	19.96		9.53	9.53	1.14	19.94	1.70	20.70	9.91	0.25	0.25	0.25
	nom							18.03										
	min	3.45	1.14	12.57	0.10	19.61	19.66		9.27	9.27	0.89	18.92	1.45	20.45	9.65			
inches	max	0.187	0.055	0.505	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.067	0.815	0.39	0.01	0.01	0.01
	nom							0.710										
	min	0.136	0.045	0.495	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.057	0.805	0.38			

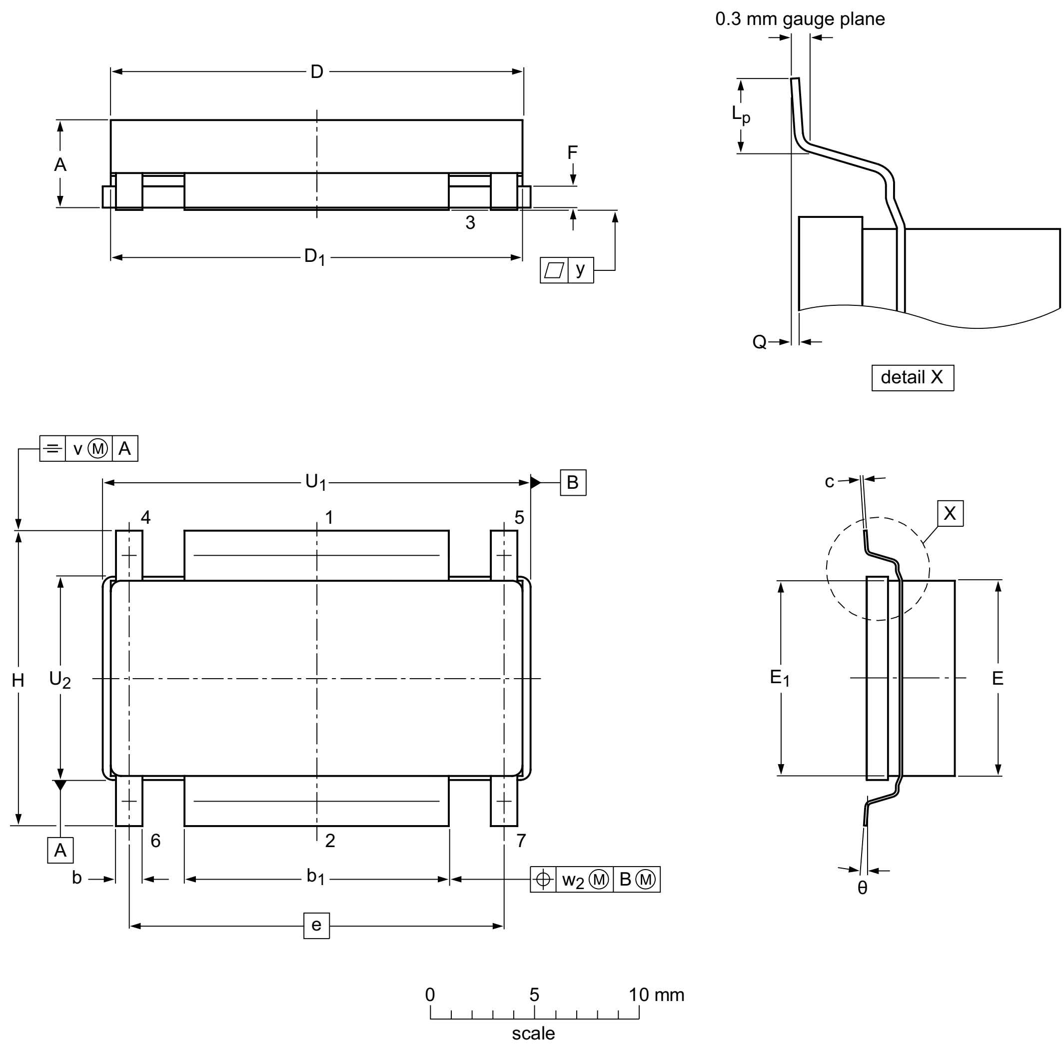
Note
1. Millimeter dimensions are derived from the original inch dimensions.
2. Dimension is measured 0.030 inch (0.76 mm) from body.

sot1244b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1244B						~~12-04-18~~ 12-05-07

Fig 21. Package outline SOT1244B

Earless flanged ceramic package; 6 leads **SOT1244C**



Dimensions

Unit(1)		A	b	b_1	c	D	D_1	e	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	θ
mm	max	4.75	1.41	12.83	0.18	20.02	19.96		9.53	9.53	1.14	14.3	1.38	0.195	20.70	9.91	0.25	0.25	0.15	7°
	nom							18.03												
	min	3.45	1.14	12.57	0.10	19.61	19.66		9.27	9.27	0.89	14.1	0.98	0.055	20.45	9.65				0°
inches	max	0.187	0.055	0.505	0.007	0.788	0.786		0.375	0.375	0.045	0.563	0.055	0.008	0.815	0.39	0.01	0.01	0.006	7°
	nom							0.710												
	min	0.136	0.045	0.495	0.004	0.772	0.774		0.365	0.365	0.035	0.555	0.039	0.002	0.805	0.38				0°

Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot1244c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1244C						~~12-05-10~~ 12-05-30

Fig 22. Package outline SOT1244C

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G20LS-140V_20LS-140GV#3	20150901	Product data sheet		BLF8G20LS-140V _20LS-140GV v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF8G20LS-140V_20LS-140GV v.2	20141007	Product data sheet	-	BLF8G20LS-140V _20LS-140GV v.1
BLF8G20LS-140V_20LS-140GV v.1	20140207	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

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13. Contact information

For more information, please visit: http://www.ampleon.com

For sales office addresses, please visit: http://www.ampleon.com/sales

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