

AOL1424
N-Channel Enhancement Mode Field Effect Transistor
General Description

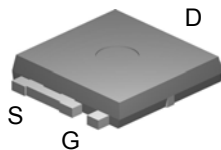
The AOL1424 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V, while retaining a 20V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a load switch.

- RoHS Compliant
- Halogen and Antimony Free Green Device*

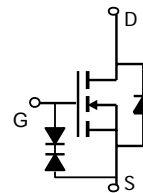
Features

- $V_{DS} (V) = 30V$
- $I_D = 70A (V_{GS} = 10V)$
- $R_{DS(ON)} < 6.5m\Omega (V_{GS} = 10V)$
- $R_{DS(ON)} < 9.8m\Omega (V_{GS} = 4.5V)$
- ESD Protected
- UIS Tested
- $R_g, C_{iss}, C_{oss}, C_{rss}$ Tested

Ultra SO-8™ Top View



Bottom tab
connected to
drain


Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^B	$T_C=25^\circ C$	70	A
	$T_C=100^\circ C$	50	
Pulsed Drain Current ^C	I_{DM}	120	
Continuous Drain Current ^A	$T_A=25^\circ C$	15	A
	$T_A=70^\circ C$	12	
Avalanche Current ^H	I_{AR}	30	A
Repetitive avalanche energy $L=0.3mH$ ^H	E_{AR}	135	mJ
Power Dissipation ^B	$T_C=25^\circ C$	50	W
	$T_C=100^\circ C$	25	
Power Dissipation ^A	$T_A=25^\circ C$	2.2	W
	$T_A=70^\circ C$	1.5	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	24	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	45	55
Maximum Junction-to-Case ^D	$R_{\theta JC}$	2.5	3.0	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±16V			10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.4	1.8	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	120			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		5.3 7.4	6.5 8.9	mΩ
		V _{GS} =4.5V, I _D =20A		7.8	9.8	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		67		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1.0	V
I _S	Maximum Body-Diode Continuous Current				70	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1803	2170	pF
C _{oss}	Output Capacitance			387		pF
C _{riss}	Reverse Transfer Capacitance			238		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.3	2	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		36	48	nC
Q _g (4.5V)	Total Gate Charge			19		nC
Q _{gs}	Gate Source Charge			3.9		nC
Q _{gd}	Gate Drain Charge			8.7		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		7.6		ns
t _r	Turn-On Rise Time			6.4		ns
t _{D(off)}	Turn-Off DelayTime			27		ns
t _f	Turn-Off Fall Time			8.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=100A/μs		27	33	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=100A/μs		17		nC

A: The value of R_{θJA} is measured with the device in a still air environment with T_A =25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on T_{J(MAX)}=150°C, using steady state junction-to-ambient thermal resistance.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

H: EAR and IAR ratings are based on low frequency and duty cycles such that T_{J(start)}=25C for each pulse.

* This device is guaranteed green after date code 8P11 (June 1ST 2008)

Rev6: March 2009

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

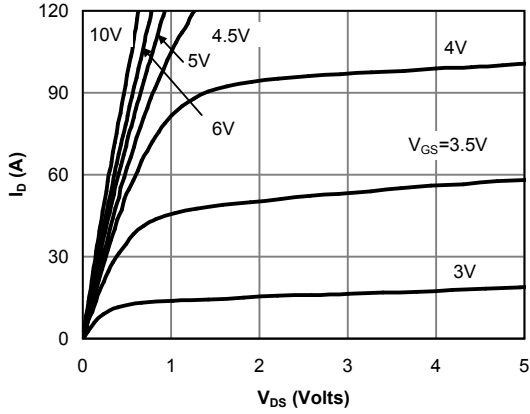


Figure 1: On-Region Characteristics

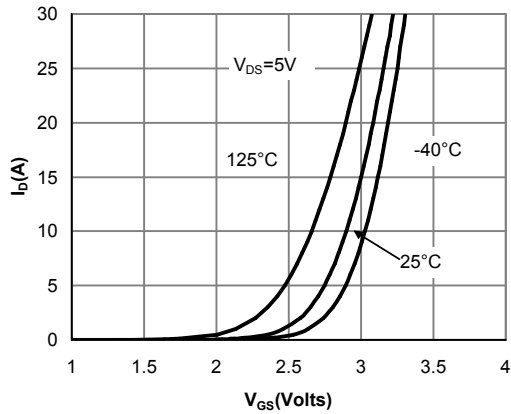


Figure 2: Transfer Characteristics

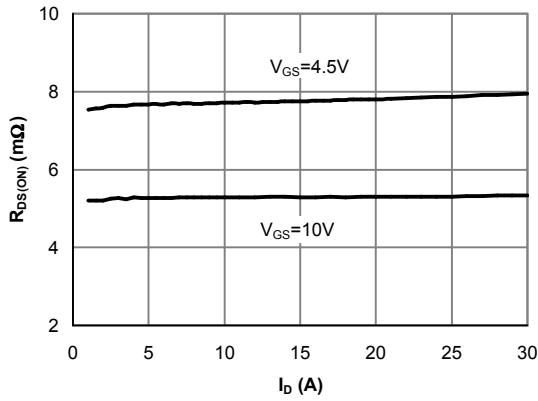


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

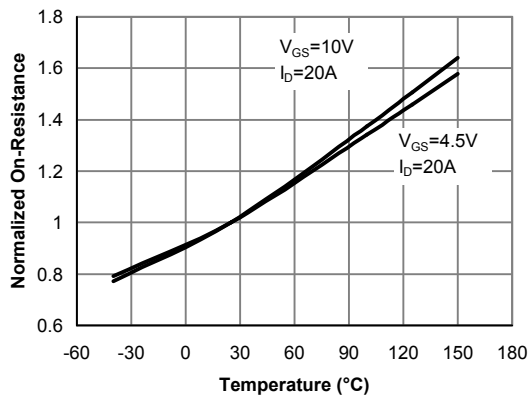


Figure 4: On-Resistance vs. Junction Temperature

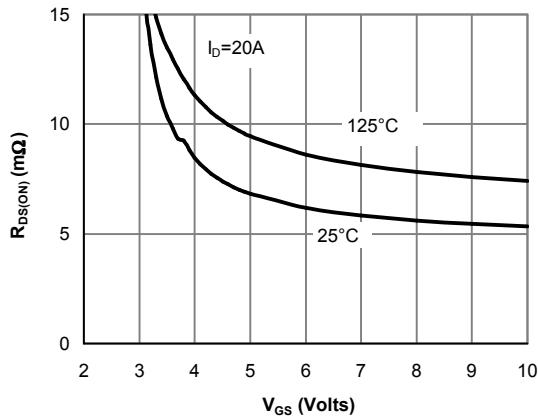


Figure 5: On-Resistance vs. Gate-Source Voltage

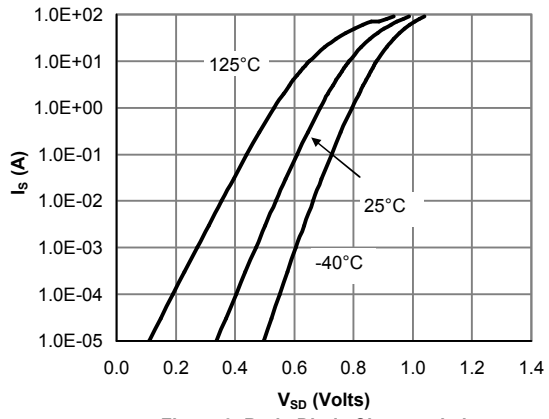


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

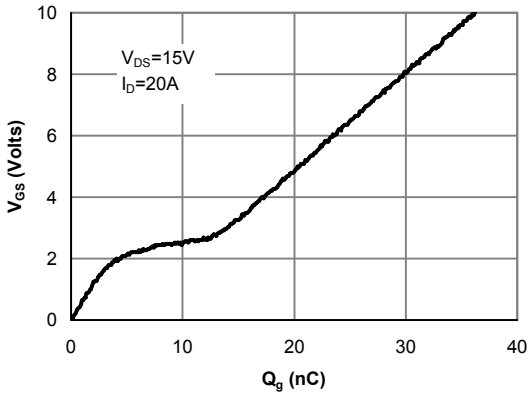


Figure 7: Gate-Charge Characteristics

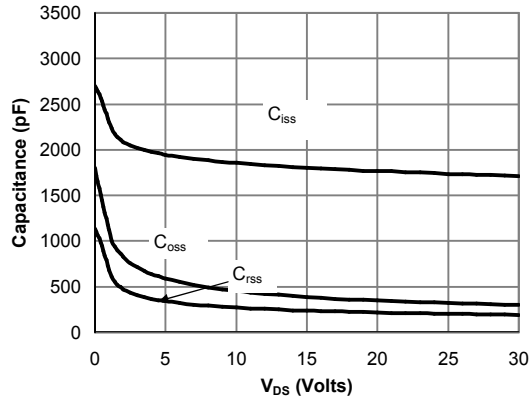


Figure 8: Capacitance Characteristics

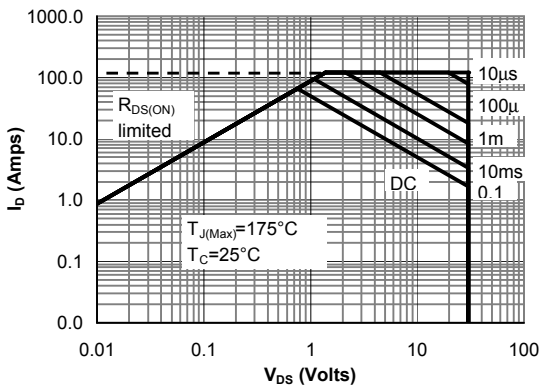


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

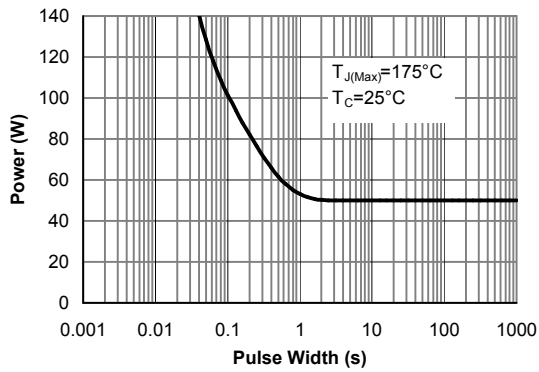


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

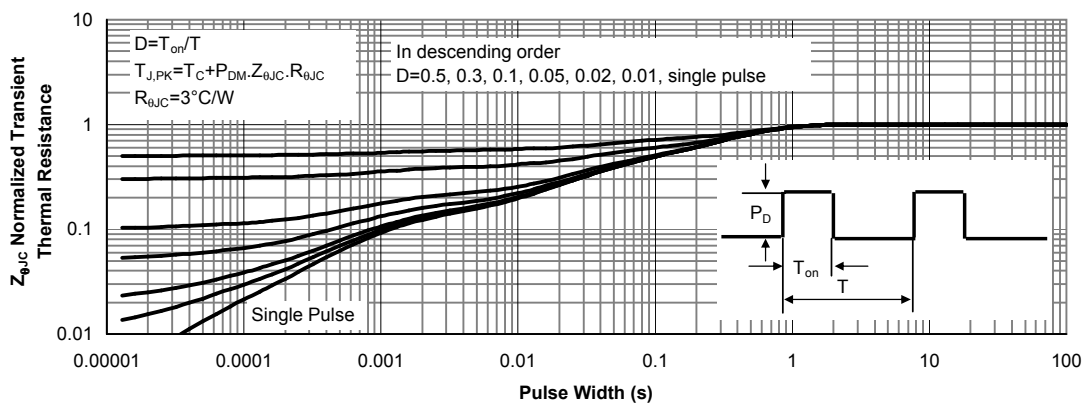


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

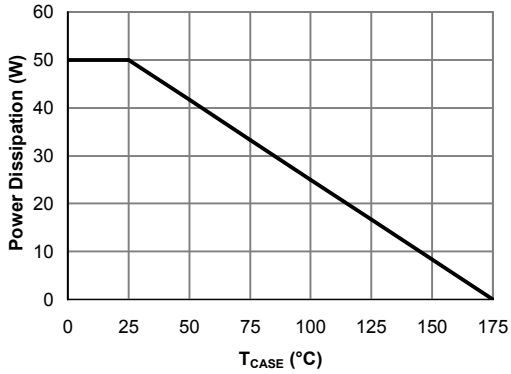


Figure 12: Power De-rating (Note B)

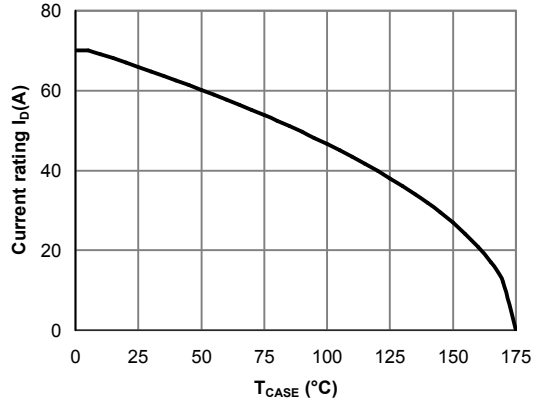


Figure 13: Current De-rating (Note B)

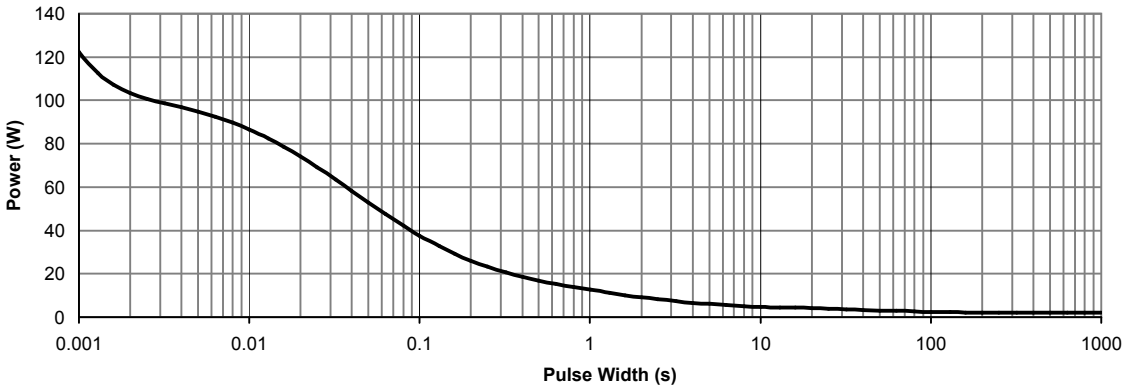


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

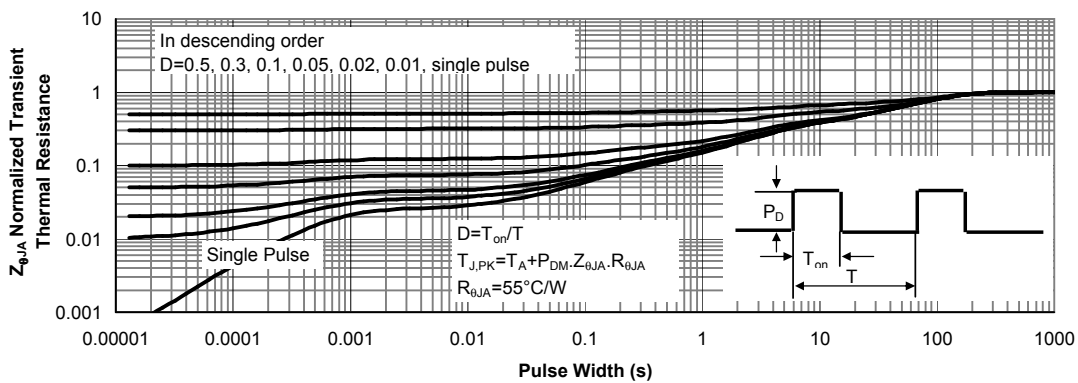
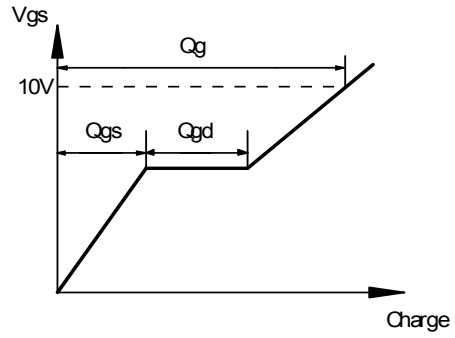
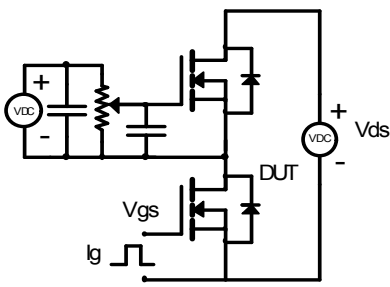
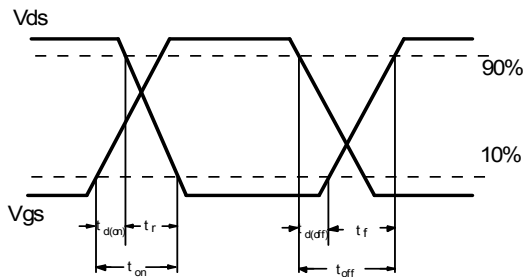
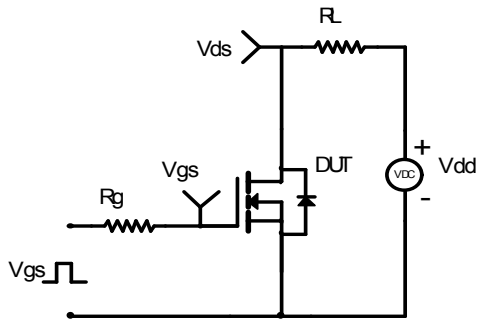


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

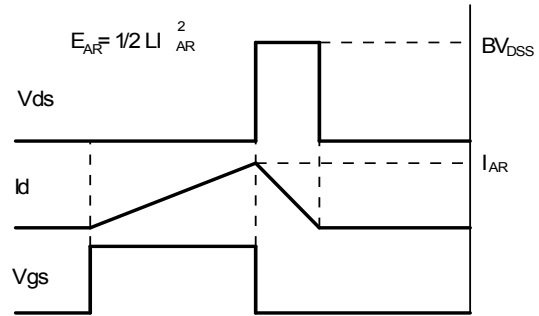
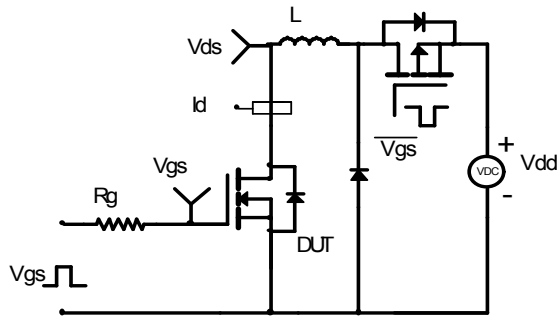
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

