

General Description

- Latest Trench Power MOSFET technology
- Very Low RDS(on) at 4.5VGS
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

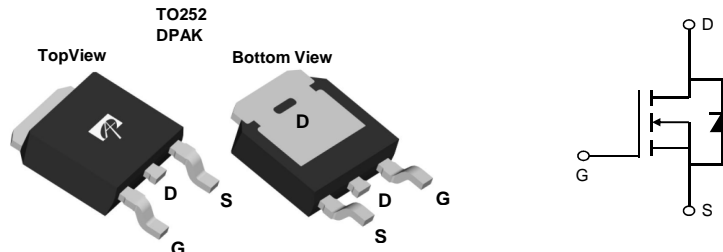
Application

- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

V _{DS}	25V
I _D (at V _{GS} =10V)	46A
R _{DS(ON)} (at V _{GS} =10V)	< 5mΩ
R _{DS(ON)} (at V _{GS} = 4.5V)	< 10mΩ

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	25	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ^G	I _D	T _C =25°C	46
		T _C =100°C	36
Pulsed Drain Current ^C	I _{DM}	170	A
Continuous Drain Current	I _{DSM}	T _A =25°C	18
		T _A =70°C	14
Avalanche Current ^C	I _{AS}	29	A
Avalanche energy L=0.1mH ^C	E _{AS}	42	mJ
V _{DS} Spike	V _{SPIKE}	33	V
Power Dissipation ^B	P _D	T _C =25°C	50
		T _C =100°C	25
Power Dissipation ^A	P _{DSM}	T _A =25°C	2.5
		T _A =70°C	1.6
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	R _{θJA}	16	20	°C/W
Maximum Junction-to-Ambient ^{A,D}		Steady-State	41	50
Maximum Junction-to-Case	R _{θJC}	2.5	3	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	25			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =25V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.6	2	2.4	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		4 5.4	5 6.8	mΩ
		V _{GS} =4.5V, I _D =20A		7.1	10	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		83		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				46	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			1333		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		512		pF
C _{rss}	Reverse Transfer Capacitance			42		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.8	1.7	2.6	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		18.3	33	nC
Q _{g(4.5V)}	Total Gate Charge			8.5	17	nC
Q _{gs}	Gate Source Charge			4.8		nC
Q _{gd}	Gate Drain Charge			2.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		7.5		ns
t _r	Turn-On Rise Time			4.8		ns
t _{D(off)}	Turn-Off DelayTime			23.3		ns
t _f	Turn-Off Fall Time			4.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		14.1		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		16.2		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=175° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

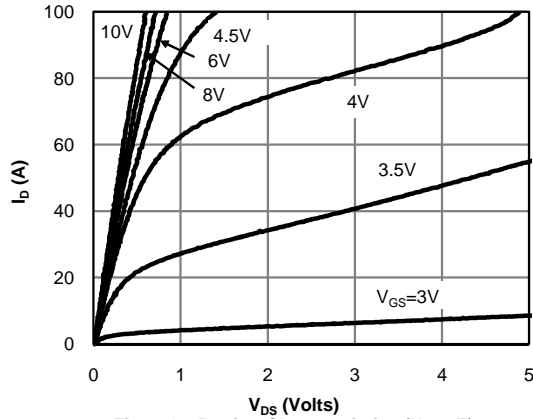


Figure 1: On-Region Characteristics (Note E)

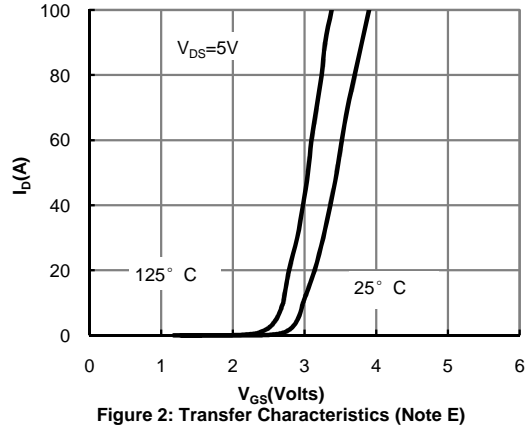


Figure 2: Transfer Characteristics (Note E)

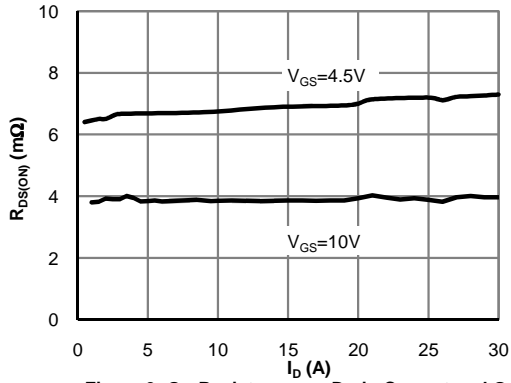


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

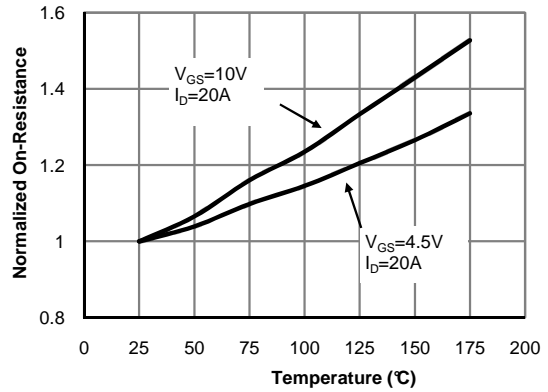


Figure 4: On-Resistance vs. Junction Temperature (Note E)

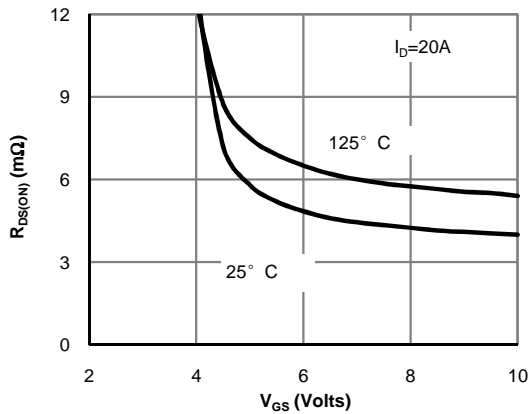


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

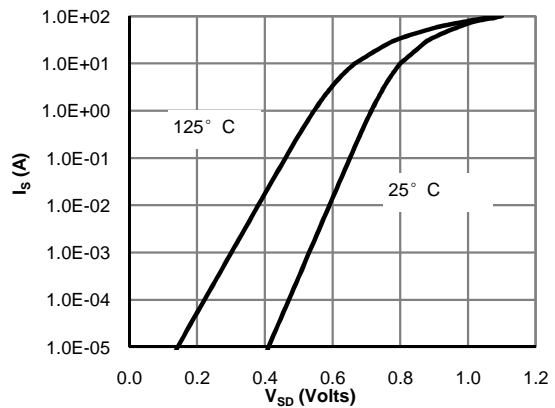


Figure 6: Body-Diode Characteristics (Note E)

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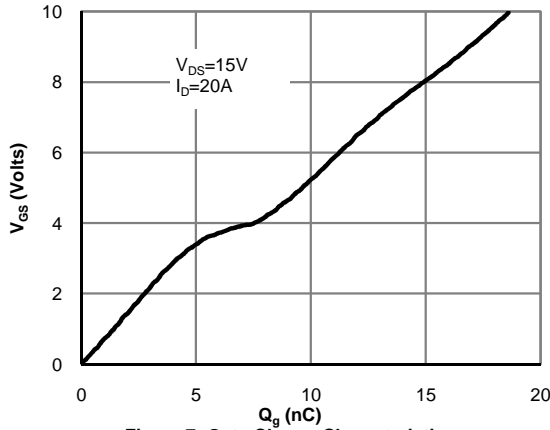


Figure 7: Gate-Charge Characteristics

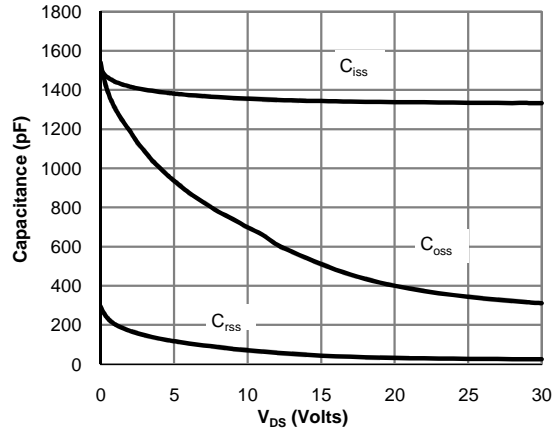


Figure 8: Capacitance Characteristics

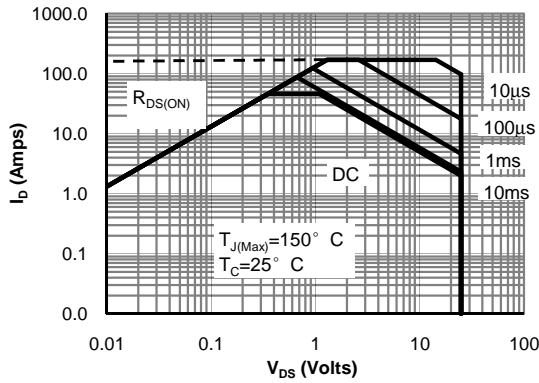


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

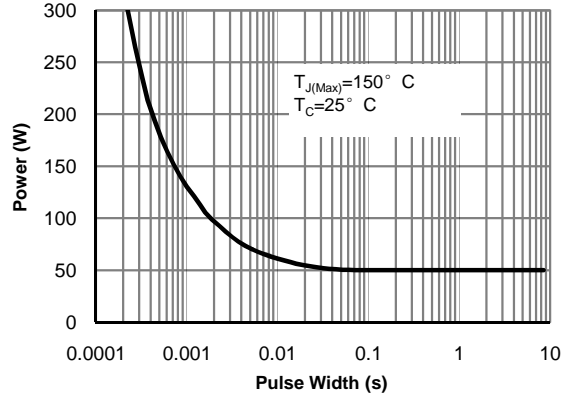


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

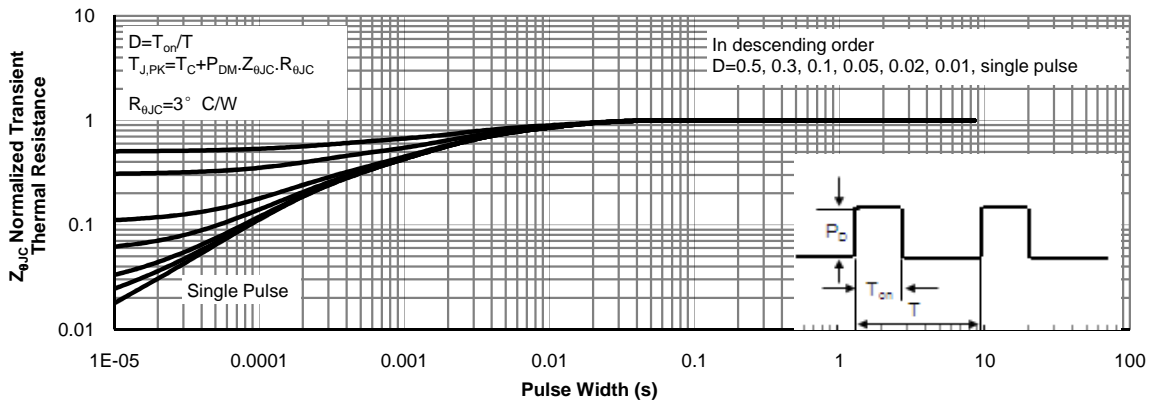


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

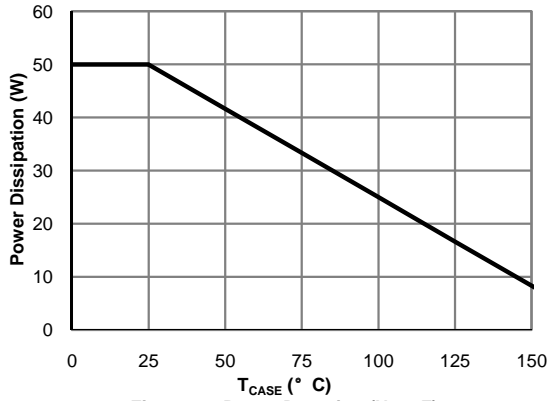


Figure 12: Power De-rating (Note F)

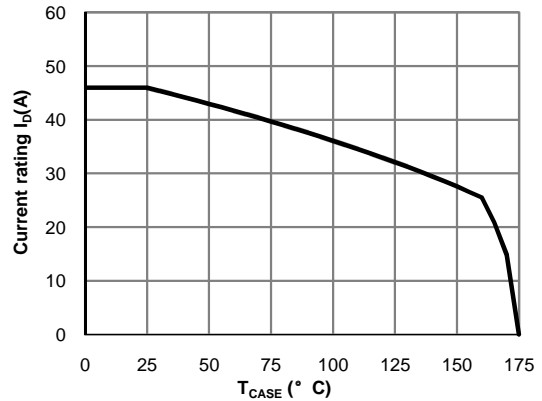


Figure 13: Current De-rating (Note F)

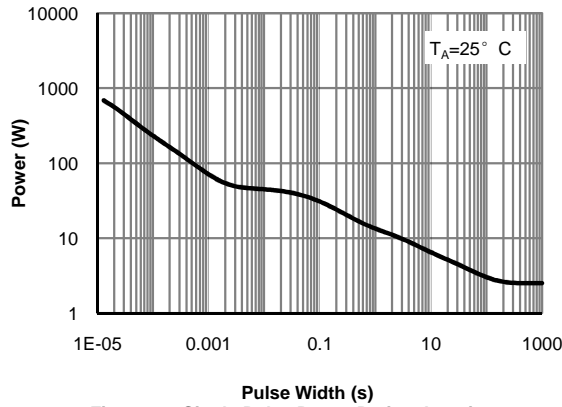


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

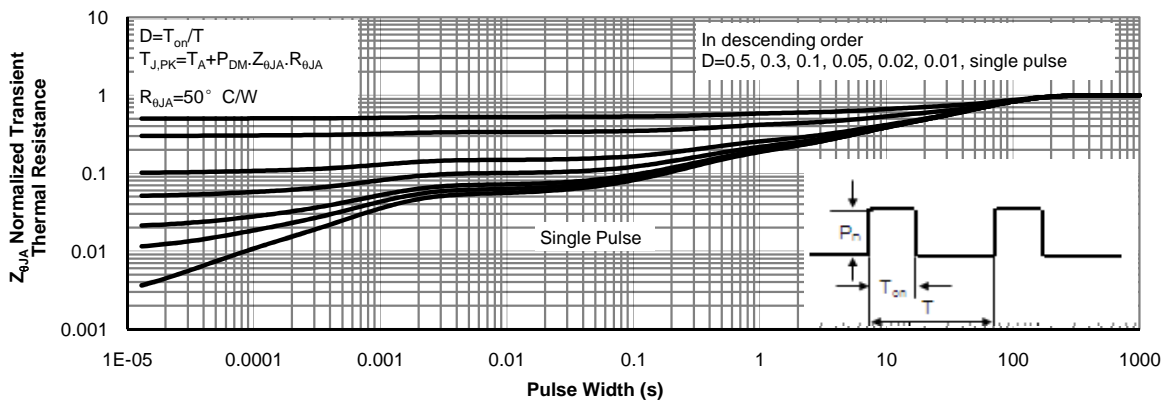


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

