

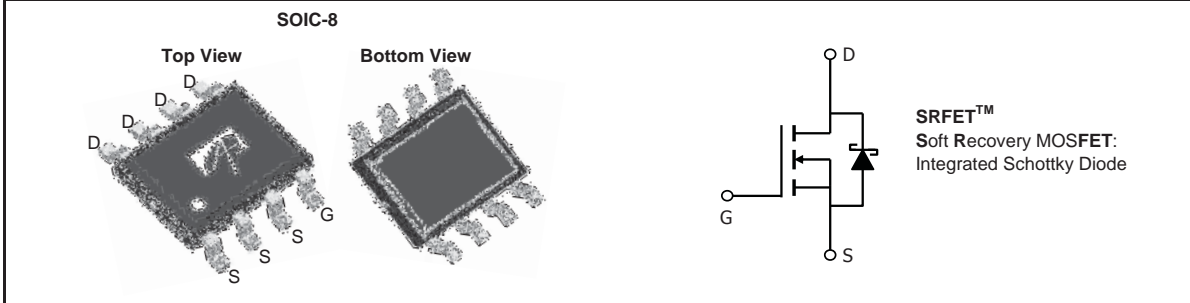
#### General Description

SRFET™ AO4728 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent  $R_{DS(ON)}$ , and low gate charge. This device is ideally suited for use as a low side switch in CPU core power conversion.

#### Product Summary

$V_{DS}$  (V) = 30V  
 $I_D$  = 20A ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 4.3m\Omega$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 6m\Omega$  ( $V_{GS} = 4.5V$ )

100% UIS Tested  
 100% Rg Tested



#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	20
		$T_C=70^\circ\text{C}$	17
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	146	A
Avalanche Current <sup>C</sup>	$I_{AR}$	40	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	80	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	3.1
		$T_C=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	31	40	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	59	75
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =125°C			0.1 20	mA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			0.1	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.2	1.8	2.2	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	146			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		3.6 5.5	4.3 6.6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =18A		4.8	6	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		87		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.4	0.7	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				6	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz	2975	3719	4463	pF
C <sub>oss</sub>	Output Capacitance		485	693	900	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		204	340	476	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.28	0.56	0.84	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A	48	60	72	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		20	25	30	nC
Q <sub>gs</sub>	Gate Source Charge		12	15	18	nC
Q <sub>gd</sub>	Gate Drain Charge		6	10	14	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		9.2		ns
t <sub>r</sub>	Turn-On Rise Time			10.7		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			40		ns
t <sub>f</sub>	Turn-Off Fall Time			12.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, di/dt=500A/μs	10	13	16	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, di/dt=500A/μs	21	26.5	32	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

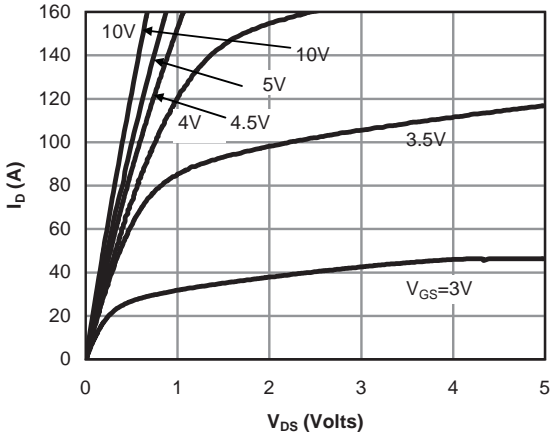


Fig 1: On-Region Characteristics (Note E)

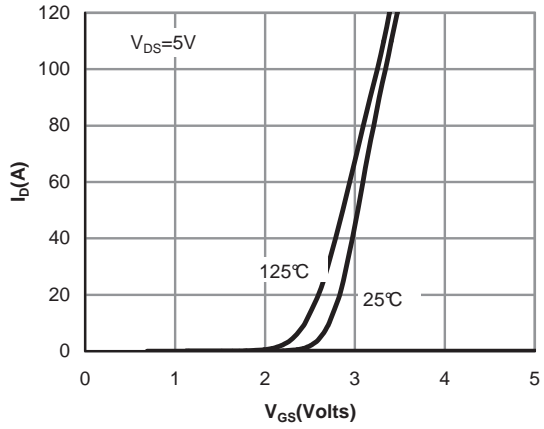


Figure 2: Transfer Characteristics (Note E)

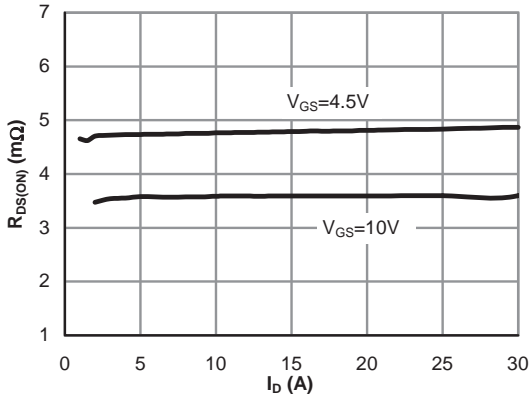


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

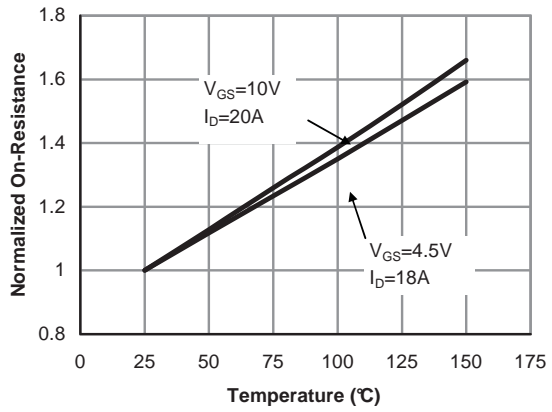


Figure 4: On-Resistance vs. Junction Temperature (Note E)

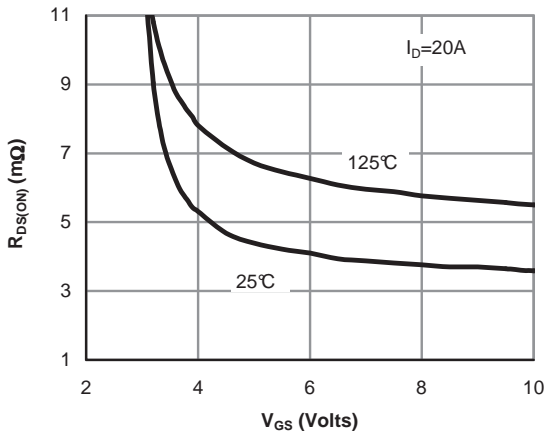


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

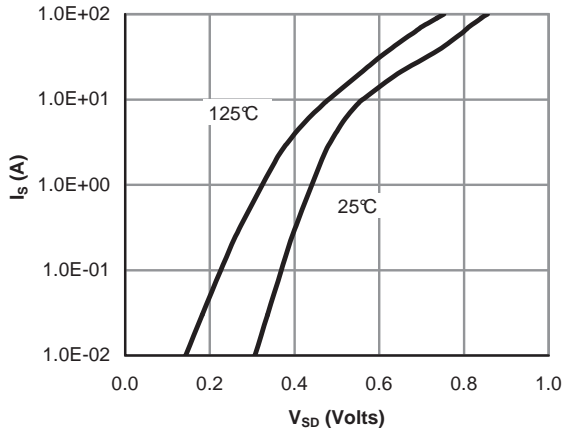


Figure 6: Body-Diode Characteristics (Note E)

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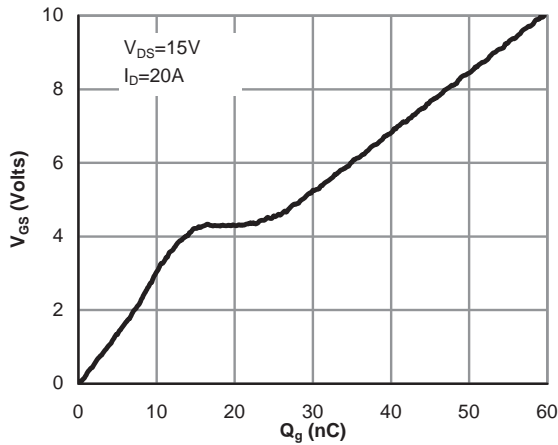


Figure 7: Gate-Charge Characteristics

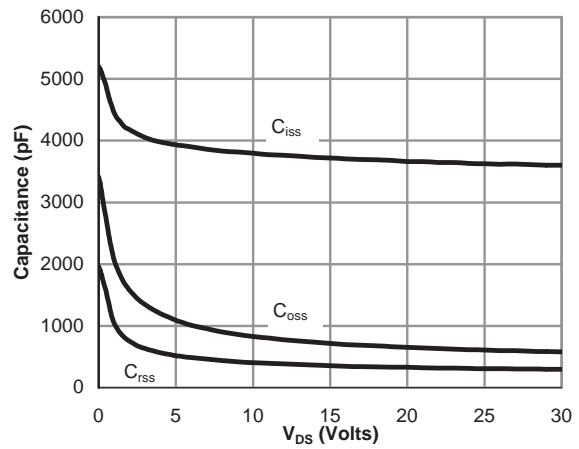


Figure 8: Capacitance Characteristics

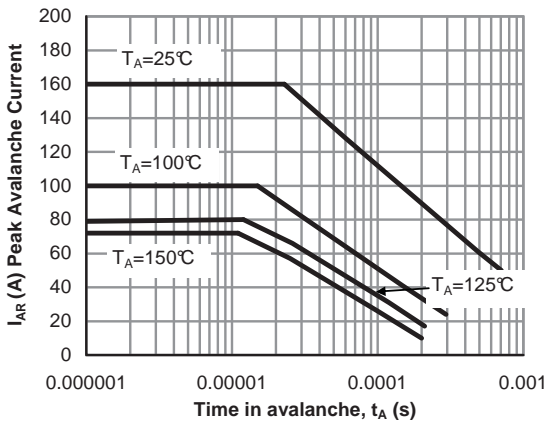


Figure 9: Single Pulse Avalanche capability (Note C)

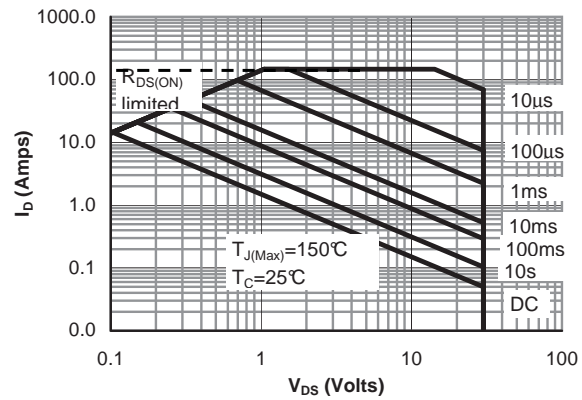


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

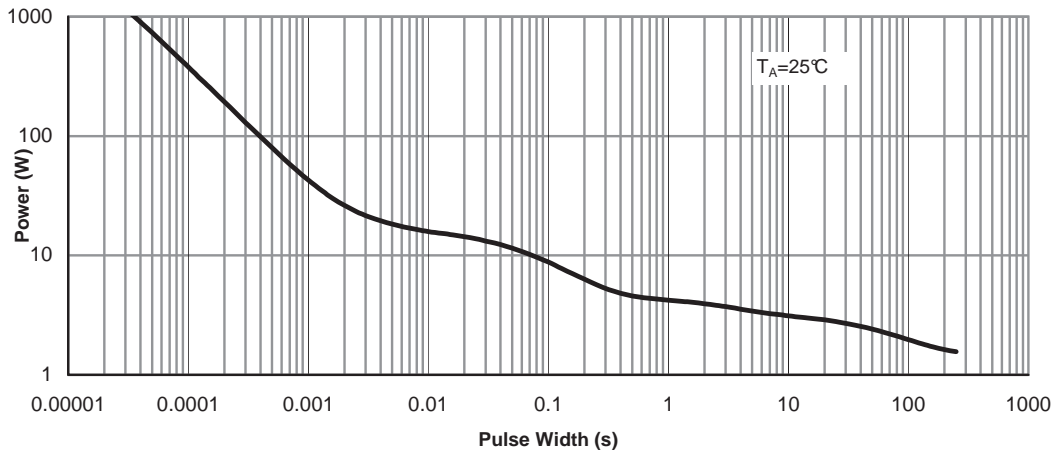


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

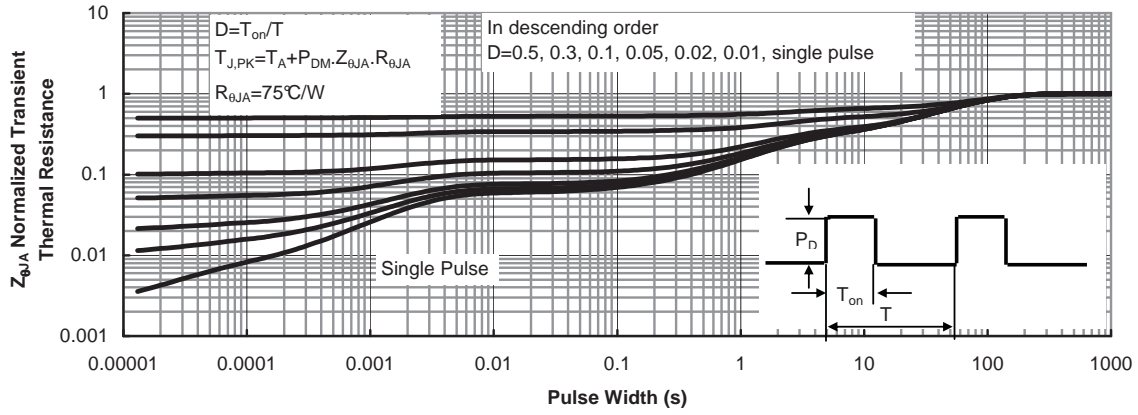


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

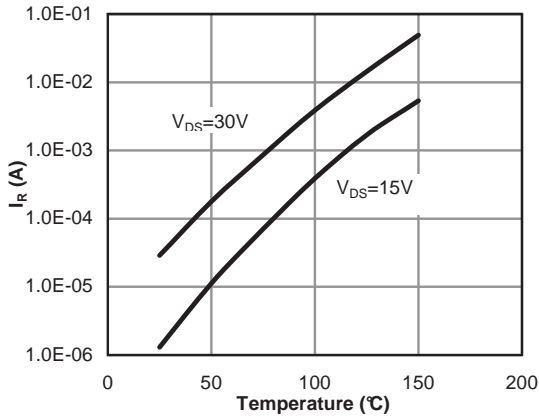


Figure 13: Diode Reverse Leakage Current vs. Junction Temperature

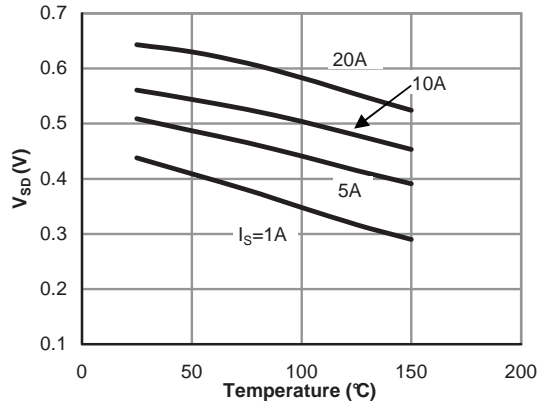


Figure 14: Diode Forward Voltage vs. Junction Temperature

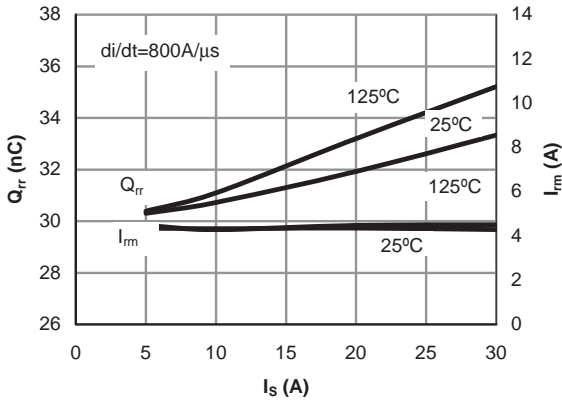


Figure 15: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

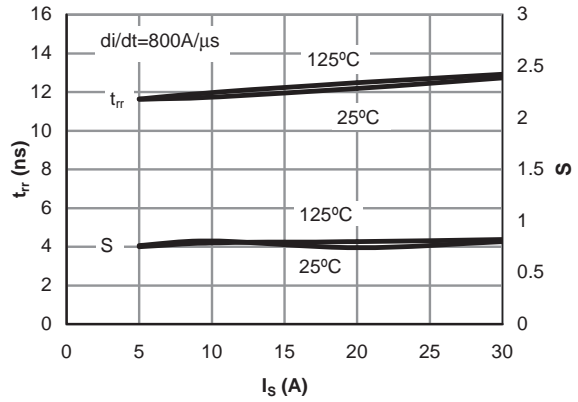


Figure 16: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

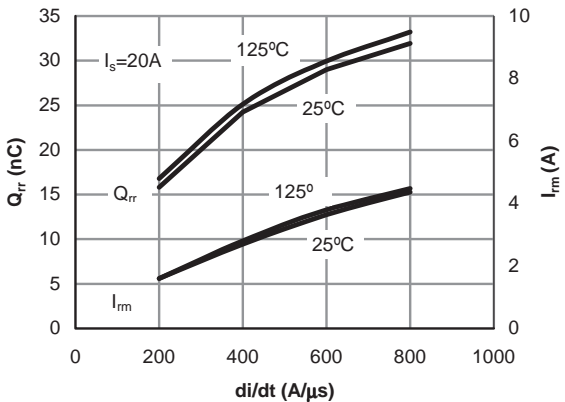


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. di/dt

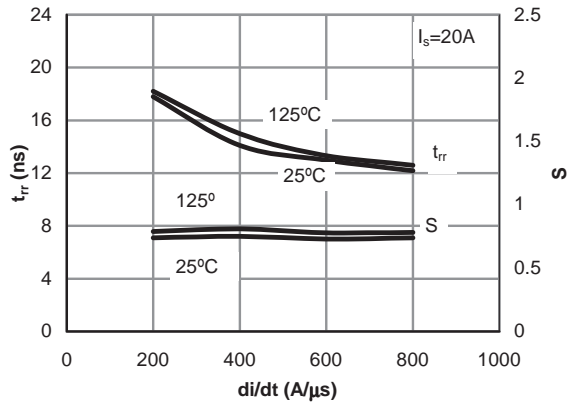
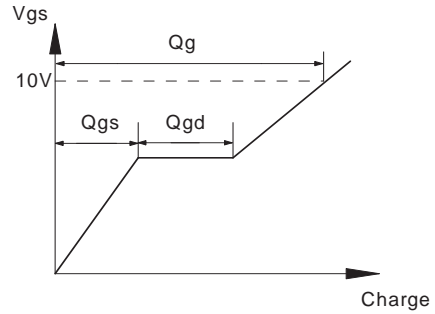
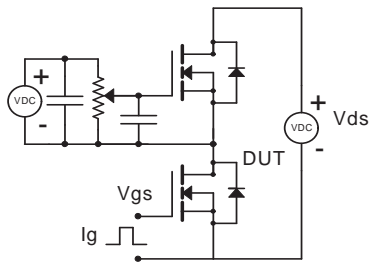
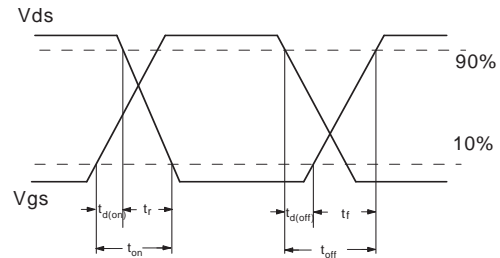
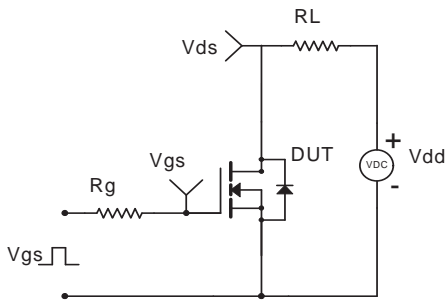


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. di/dt

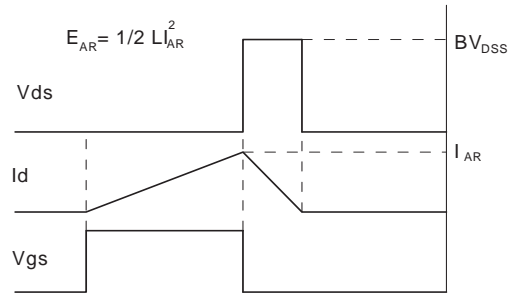
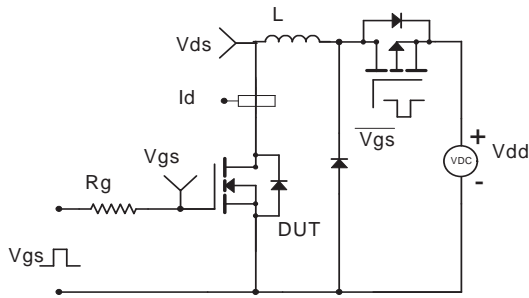
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

