

Complementary Enhancement Mode Field Effect Transistor

General Description

The AO4619 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in inverter and other applications.

Product Summary

N-Channel

V_{DS} (V) = 30V
 $I_D = 7.4A$ ($V_{GS}=10V$)
 $R_{DS(ON)}$
 $< 24m\Omega$ ($V_{GS}=10V$)
 $< 36m\Omega$ ($V_{GS}=4.5V$)

P-Channel

-30V
 $-5.2A$ ($V_{GS} = -10V$)
 $R_{DS(ON)}$
 $< 46m\Omega$ ($V_{GS} = -10V$)
 $< 72m\Omega$ ($V_{GS} = -4.5V$)

100% UIS Tested

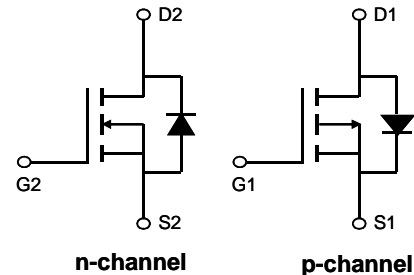
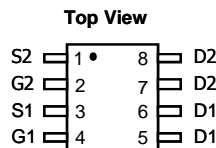
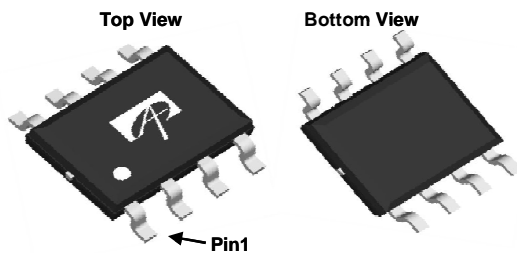
100% Rg Tested

100% UIS Tested

100% Rg Tested



SOIC-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^F	I_D	$T_A=25^\circ\text{C}$	7.4	-5.2
		$T_A=70^\circ\text{C}$	6	-4.2
Pulsed Drain Current ^B	I_{DM}	64	-25	A
Power Dissipation ^A	P_D	$T_A=25^\circ\text{C}$	2	2
		$T_A=70^\circ\text{C}$	1.3	1.3
Avalanche Current ^B	I_{AR}	9	11	A
Repetitive avalanche energy 0.3mH ^B	E_{AR}	12	18	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	$t \leq 10s$	50	62.5
Maximum Junction-to-Ambient ^A			Steady-State	82	110
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	41	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	$t \leq 10s$	50	62.5
Maximum Junction-to-Ambient ^A			Steady-State	82	110
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	41	50	$^\circ\text{C/W}$

N-channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.5	2.1	2.6	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}, V_{DS}=5\text{V}$	64			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=7.4\text{A}$ $T_J=125^\circ\text{C}$		17.7	24	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=6\text{A}$		25.3	36	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=7.4\text{A}$		20		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		373	448	pF
C_{oss}	Output Capacitance			67		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		1.2	1.8	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=7.4\text{A}$		7.2		nC
$Q_g(4.5\text{V})$	Total Gate Charge			3.5		nC
Q_{gs}	Gate Source Charge			1.3		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=2\Omega,$ $R_{GEN}=3\Omega$		4.5		ns
t_r	Turn-On Rise Time			2.7		ns
$t_{D(off)}$	Turn-Off Delay Time			14.9		ns
t_f	Turn-Off Fall Time			2.9		ns
t_{rr}	Body Diode Reverse Recovery Time		$I_F=7.4\text{A}, dl/dt=100\text{A}/\mu\text{s}$		10.5	
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=7.4\text{A}, dl/dt=100\text{A}/\mu\text{s}$		4.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

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N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

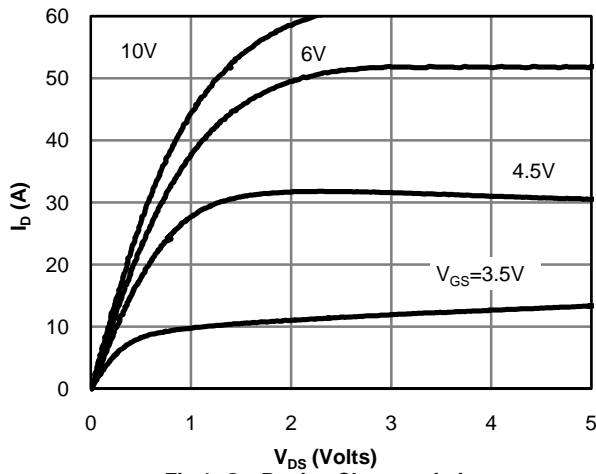


Fig 1: On-Region Characteristics

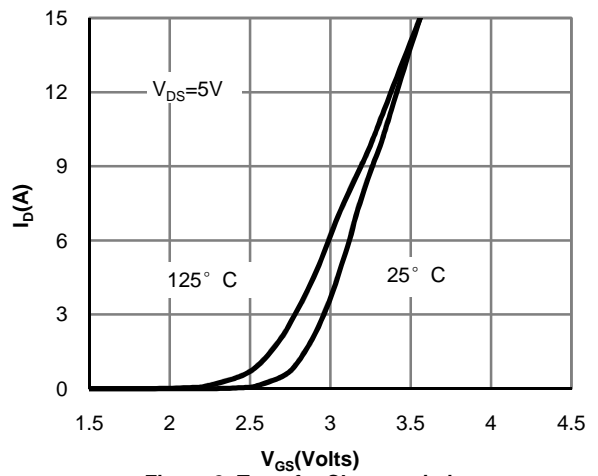


Figure 2: Transfer Characteristics

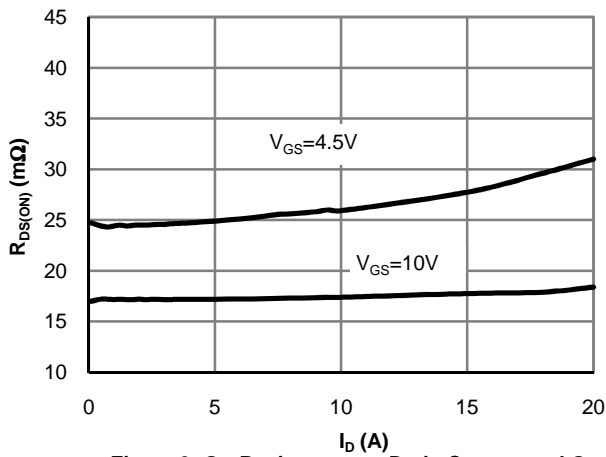


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

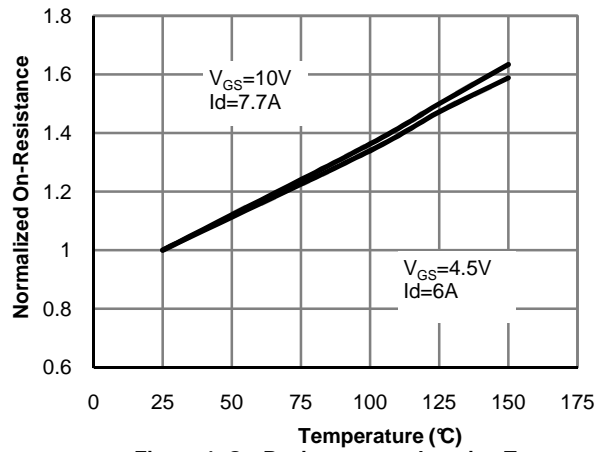


Figure 4: On-Resistance vs. Junction Temperature

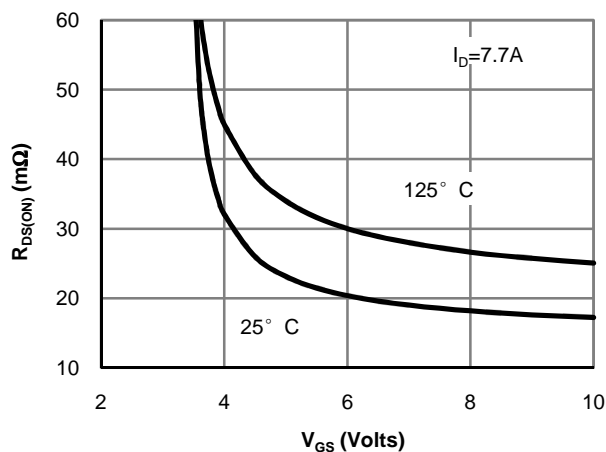


Figure 5: On-Resistance vs. Gate-Source Voltage

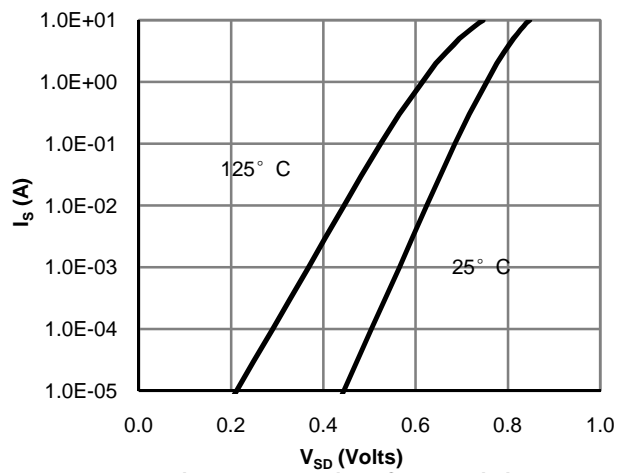


Figure 6: Body-Diode Characteristics

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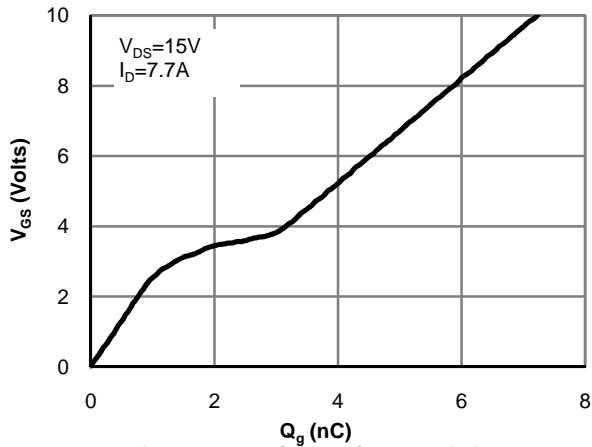


Figure 7: Gate-Charge Characteristics

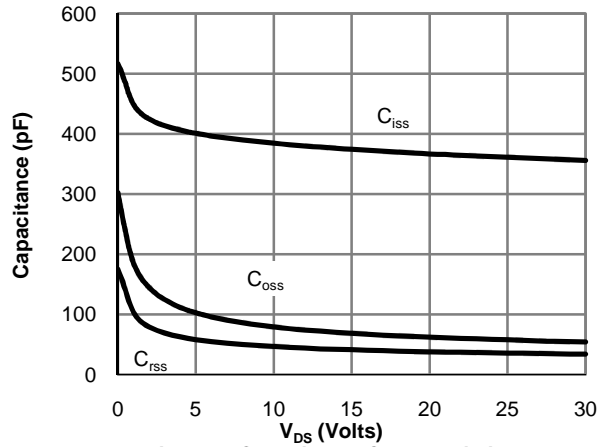


Figure 8: Capacitance Characteristics

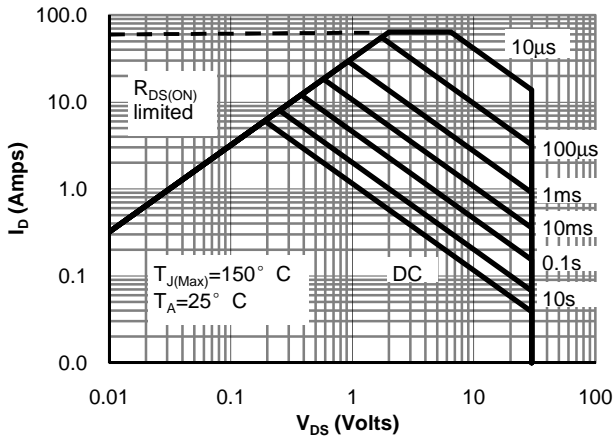


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

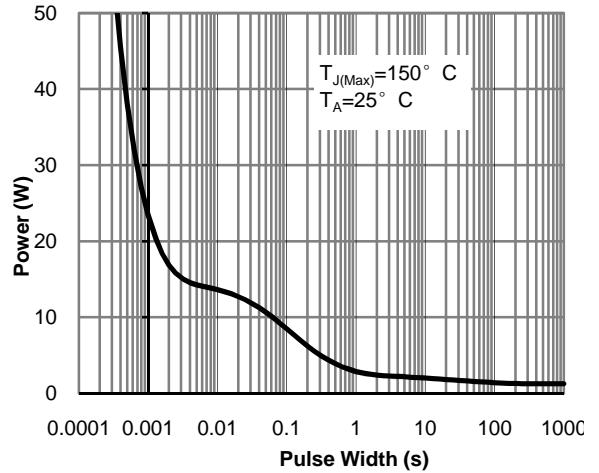


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

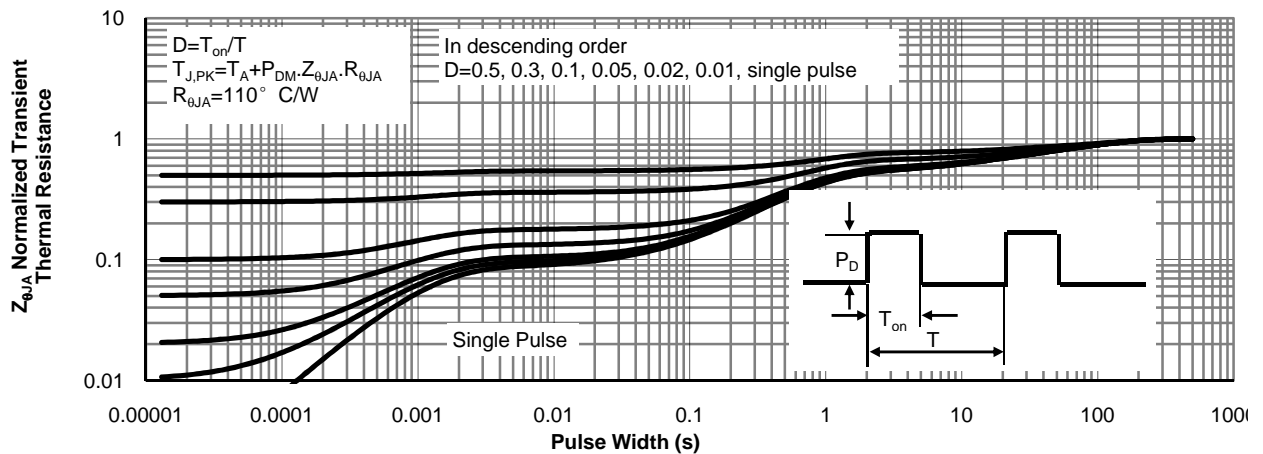


Figure 11: Normalized Maximum Transient Thermal Impedance

P-channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		$T_J=55^\circ\text{C}$			-5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.4	-1.9	-2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-5.2\text{A}$		33	46	m Ω
		$T_J=125^\circ\text{C}$		50	68	
		$V_{GS}=-4.5\text{V}$, $I_D=-4\text{A}$		53	72	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-5.2\text{A}$		14		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.8	-1	V
I_S	Maximum Body-Diode Continuous Current				-3.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		520		pF
C_{oss}	Output Capacitance			100		pF
C_{rss}	Reverse Transfer Capacitance			65		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		7.5	11.5	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-5.2\text{A}$		9.2		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			4.6		nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=3\Omega$, $R_{GEN}=3\Omega$		7.5		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			7		ns
t_{rr}	Body Diode Reverse Recovery Time		$I_F=-5.2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		11	
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-5.2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		5.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

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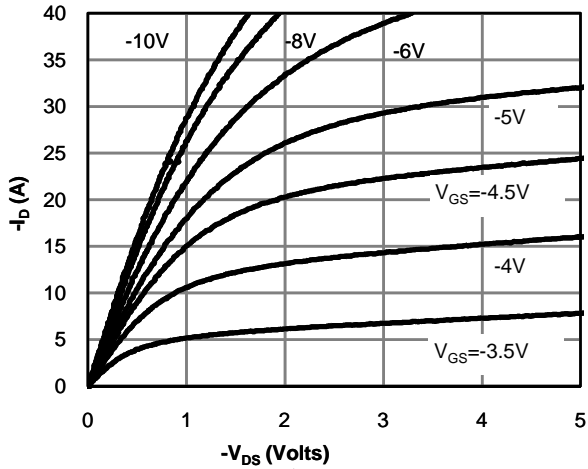


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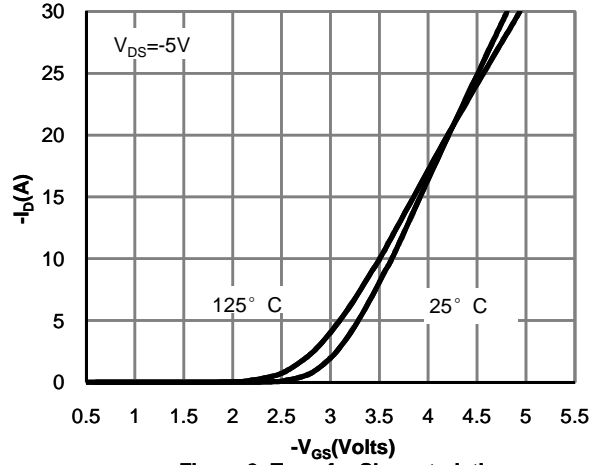


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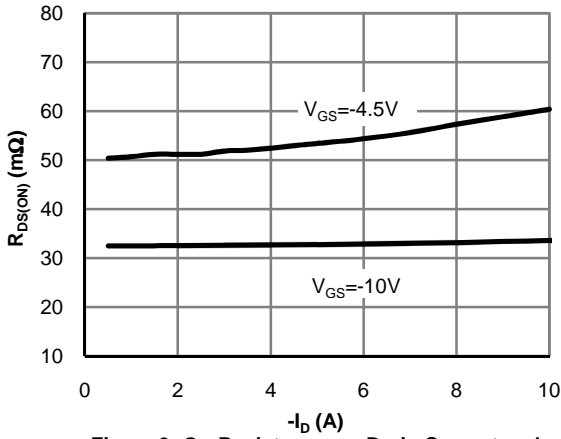


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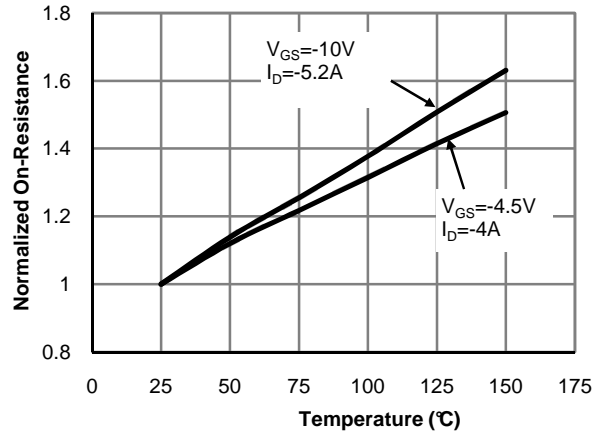


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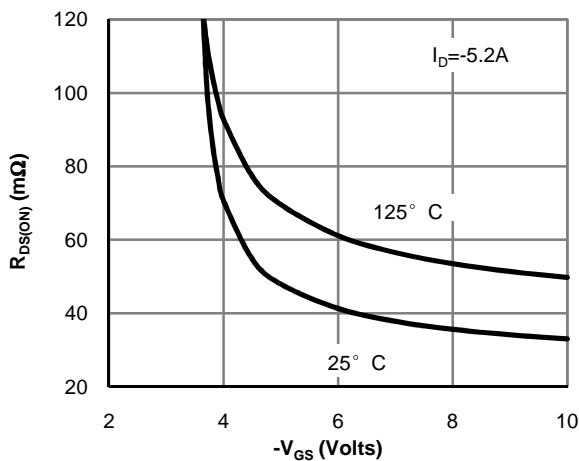


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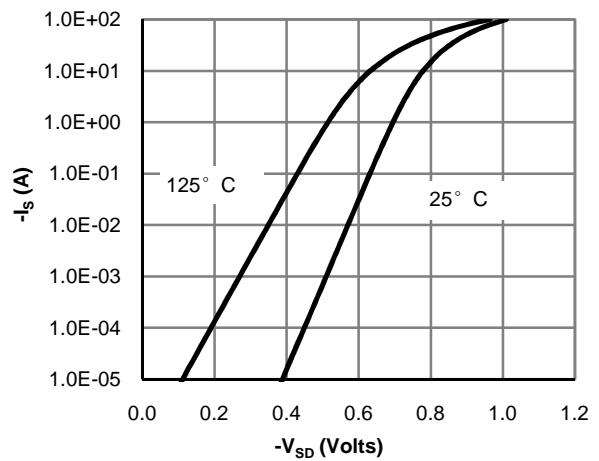


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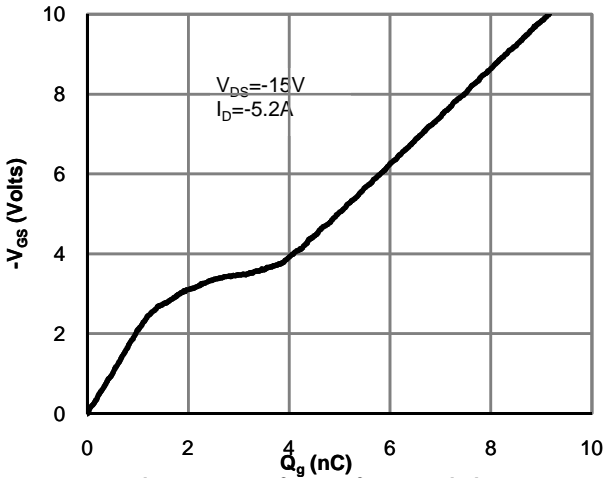


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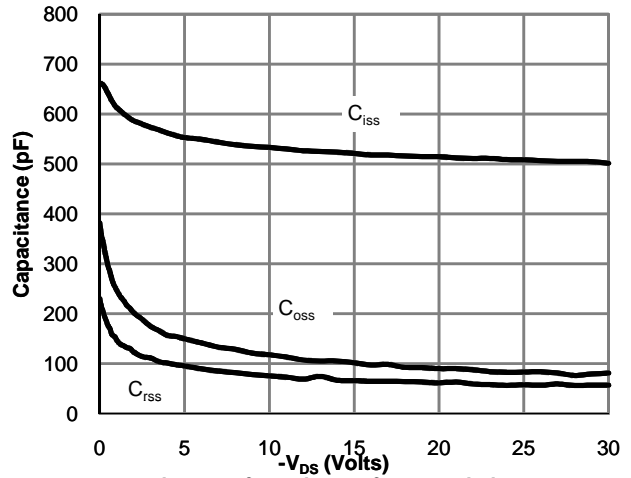


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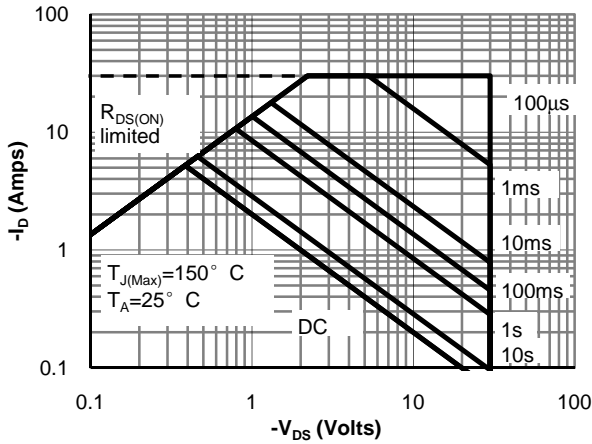


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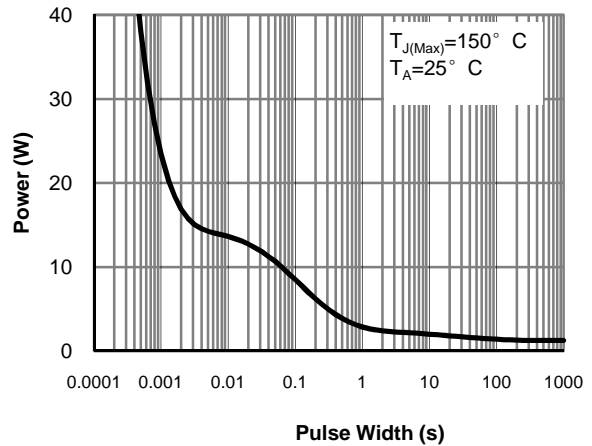


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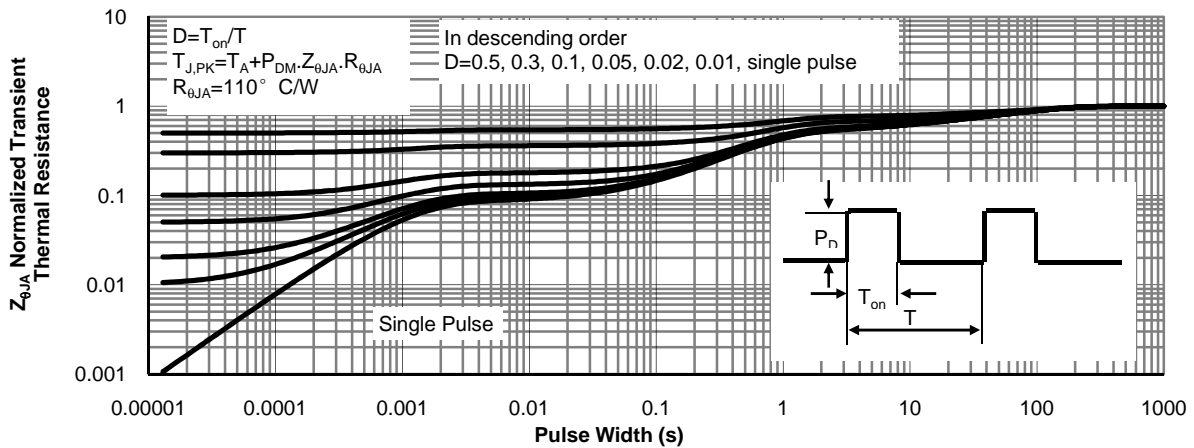


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