

**Revision History****AS4C8M16D1 - 66-pin TSOPII PACKAGE**

Revision	Details	Date
Rev 1.1	Preliminary datasheet	Feb 2009
Rev.1.2	Add Part numbering system	May 2015

## 8M x 16 DDR Synchronous DRAM (SDRAM)

Confidential

Released (Rev. 1.2, May /2015)

### Features

- Fast clock rate: 200MHz
- Differential Clock CK &  $\overline{CK}$  input
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 2M x 16-bit for each bank
- Programmable Mode and Extended Mode registers
  - CAS Latency: 2, 2.5, 3
  - Burst length: 2, 4, 8
  - Burst Type: Sequential & Interleaved
- Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 64ms
- Operating temperature range
  - Commercial (0 ~ 70°C)
  - Industrial (-40 ~ 85°C)
- Precharge & active power down
- Power supplies: VDD & VDDQ = 2.5V ± 5%
- Interface: SSTL\_2 I/O Interface
- Package: 66 Pin TSOP II, 0.65mm pin pitch
  - Pb free and Halogen free

### Overview

The **128Mb DDR AS4C8M16D1 SDRAM** is a high-speed CMOS double data rate synchronous DRAM containing 128 Mbits. It is internally configured as a quad 2M x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and  $\overline{CK}$ .

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The DDR SDRAM provides programmable Read or Write burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, The DDR SDRAM features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and high performance.

**Table 1.Ordering Information**

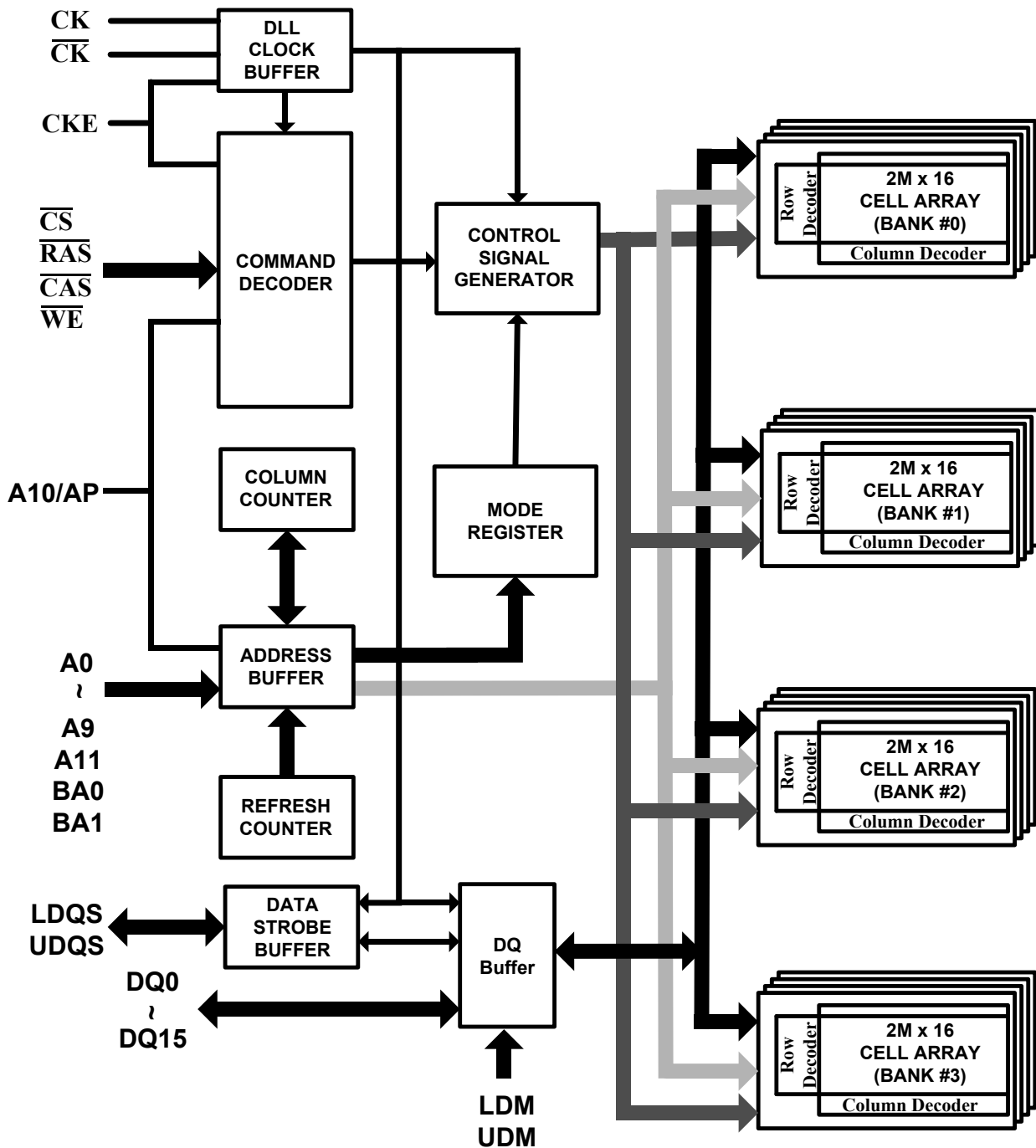
Part Number	Org	Max Clock (MHz)	Temperature	Temp Range	Package
AS4C8M16D1-TCN	8M x 16	200	Commercial	0 ~ 70°C	66pin TSOPII
AS4C8M16D1-5TIN	8M x 16	200	Industrial	-40 ~ 85°C	66pin TSOPII

T: indicates TSOP II package  
 C: indicates Commercial temp.  
 I: indicates Industrial temp.  
 N: indicates lead free ROHS

**Figure 1. Pin Assignment (Top View)**

VDD	1	66	VSS
DQ0	2	65	DQ15
VDDQ	3	64	VSSQ
DQ1	4	63	DQ14
DQ2	5	62	DQ13
VSSQ	6	61	VDDQ
DQ3	7	60	DQ12
DQ4	8	59	DQ11
VDDQ	9	58	VSSQ
DQ5	10	57	DQ10
DQ6	11	56	DQ9
VSSQ	12	55	VDDQ
DQ7	13	54	DQ8
NC	14	53	NC
VDDQ	15	52	VSSQ
LDQS	16	51	UDQS
NC	17	50	NC
VDD	18	49	VREF
NC	19	48	VSS
LDM	20	47	UDM
$\overline{WE}$	21	46	$\overline{CK}$
$\overline{CAS}$	22	45	CK
$\overline{RAS}$	23	44	CKE
$\overline{CS}$	24	43	NC
NC	25	42	NC
BA0	26	41	A11
BA1	27	40	A9
A10/AP	28	39	A8
A0	29	38	A7
A1	30	37	A6
A2	31	36	A5
A3	32	35	A4
VDD	33	34	VSS

Figure 2. Block Diagram



## Pin Descriptions

**Table 2. Pin Details**

Symbol	Type	Description
CK, $\overline{\text{CK}}$	Input	<b>Differential Clock:</b> CK, $\overline{\text{CK}}$ are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. Both CK and $\overline{\text{CK}}$ increment the internal burst counter and controls the output registers.
CKE	Input	<b>Clock Enable:</b> CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	<b>Bank Activate:</b> BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A11	Input	<b>Address Inputs:</b> A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A8 with A10 defining Auto Precharge).
$\overline{\text{CS}}$	Input	<b>Chip Select:</b> $\overline{\text{CS}}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is sampled HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{\text{RAS}}$	Input	<b>Row Address Strobe:</b> The $\overline{\text{RAS}}$ signal defines the operation commands in conjunction with the $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ signals and is latched at the positive edges of CK. When $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ are asserted "LOW" and $\overline{\text{CAS}}$ is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the $\overline{\text{WE}}$ signal. When the $\overline{\text{WE}}$ is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{\text{WE}}$ is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
$\overline{\text{CAS}}$	Input	<b>Column Address Strobe:</b> The $\overline{\text{CAS}}$ signal defines the operation commands in conjunction with the $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ signals and is latched at the positive edges of CK. When $\overline{\text{RAS}}$ is held "HIGH" and $\overline{\text{CS}}$ is asserted "LOW," the column access is started by asserting $\overline{\text{CAS}}$ "LOW." Then, the Read or Write command is selected by asserting $\overline{\text{WE}}$ "HIGH" or "LOW".
$\overline{\text{WE}}$	Input	<b>Write Enable:</b> The $\overline{\text{WE}}$ signal defines the operation commands in conjunction with the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals and is latched at the positive edges of CK. The $\overline{\text{WE}}$ input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, UDQS	Input / Output	<b>Bidirectional Data Strobe:</b> Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15.
LDM, UDM	Input	<b>Data Input Mask:</b> Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0 - DQ15	Input / Output	<b>Data I/O:</b> The DQ0-DQ15 input and output data are synchronized with positive and negative edges of LDQS and UDQS. The I/Os are byte-maskable during Writes.
VDD	Supply	<b>Power Supply:</b> +2.5V $\pm 5\%$
VSS	Supply	<b>Ground</b>
VDDQ	Supply	<b>DQ Power:</b> +2.5V $\pm 5\%$ . Provide isolated power to DQs for improved noise immunity.

VSSQ	Supply	<b>DQ Ground:</b> Provide isolated ground to DQs for improved noise immunity.
VREF	Supply	<b>Reference Voltage for Inputs:</b> +0.5*VDDQ
NC	-	<b>No Connect:</b> No internal connection, these pins suggest to be left unconnected.

## Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 4 shows the truth table for the operation commands.

**Table 3. Truth Table (Note (1), (2))**

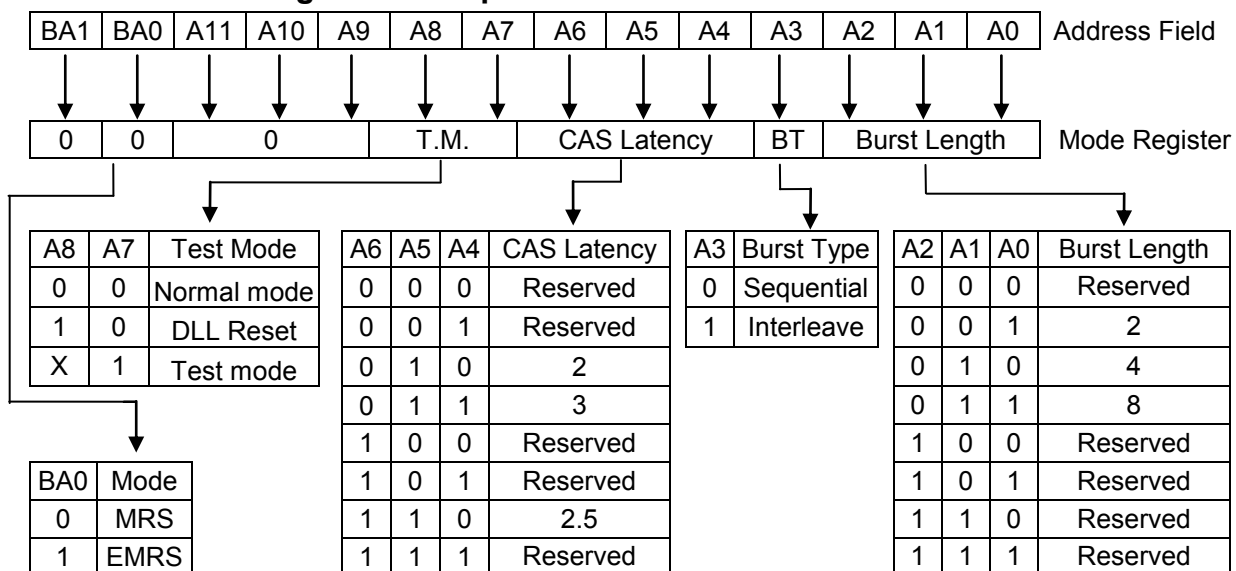
Command	State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	DM	BA0,1	A10	A0-9,11	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$
BankActivate	Idle <sup>(3)</sup>	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active <sup>(3)</sup>	H	X	X	V	L	Column address (A0 ~ A8)	L	H	L	L
Write and AutoPrecharge	Active <sup>(3)</sup>	H	X	X	V	H		L	H	L	L
Read	Active <sup>(3)</sup>	H	X	X	V	L	Column address (A0 ~ A8)	L	H	L	H
Read and Autoprecharge	Active <sup>(3)</sup>	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
Extended MRS	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active <sup>(4)</sup>	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Precharge Power Down Mode Entry	Idle	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Precharge Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Active Power Down Mode Entry	Active	H	L	X	X	X	X	H	X	X	X
								L	V	V	V
Active Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X
Data Input Mask Enable(5)	Active	H	X	H	X	X	X	X	X	X	X

- Note:**
1. V=Valid data, X=Don't Care, L=Low level, H=High level
  2. CKE<sub>n</sub> signal is input level when commands are provided.  
CKE<sub>n-1</sub> signal is input level one clock cycle before the commands are provided.
  3. These are states of bank designated by BA signal.
  4. Device state is 2, 4, and 8 burst operation.
  5. LDM and UDM can be enabled respectively.

## Mode Register Set (MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs CAS Latency, Burst Type, and Burst Length to make the DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed. The Mode Register is written by asserting Low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A11 and BA0, BA1 in the same cycle in which  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and CAS latencies.

**Table 4. Mode Register Bitmap**



- Burst Length Field (A2~A0)**

This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, and 8.

**Table 5. Burst Length**

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



- Addressing Mode Select Field (A3)

The Addressing Mode can be one of two modes, either Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4, and 8.

**Table 6. Addressing Mode**

A3	Addressing Mode
0	Sequential
1	Interleave

- Burst Definition, Addressing Sequence of Sequential and Interleave Mode

**Table 7. Burst Address ordering**

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

- CAS Latency Field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field.

$$t_{CAC}(\min) \leq \text{CAS Latency} \times t_{CK}$$

**Table 8. CAS Latency**

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved

- Test Mode field (A8~A7)

These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

**Table 9. Test Mode**

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset
X	1	Test mode

- (BA0, BA1)

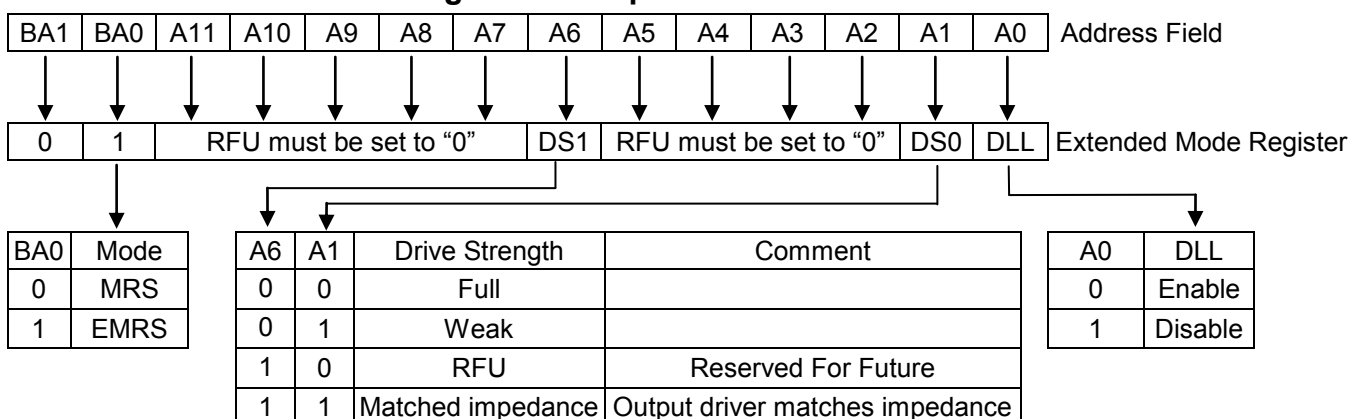
**Table 10. MRS/EMRS**

BA1	BA0	A11 ~ A0
RFU	0	MRS Cycle
RFU	1	Extended Functions (EMRS)

## Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The extended mode register is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$ . The state of A0, A2 ~ A5, A7 ~ A11 and BA1 is written in the mode register in the same cycle as  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

**Table 11. Extended Mode Register Bitmap**



**Table 12. Absolute Maximum Rating**

Symbol	Item	Rating	Unit	Note
		-5		
V <sub>IN</sub> , V <sub>OUT</sub>	I/O Pins Voltage	- 0.5~V <sub>DDQ</sub> + 0.5	V	1,2
V <sub>IN</sub>	V <sub>REF</sub> and Inputs Voltage	- 1~3.6	V	1,2
V <sub>DD</sub> , V <sub>DDQ</sub>	Power Supply Voltage	- 1~3.6	V	1,2
T <sub>A</sub>	Ambient Temperature	Commercial	0~70	°C
		Industrial	-40~85	°C
T <sub>STG</sub>	Storage Temperature	- 55~150	°C	1
P <sub>D</sub>	Power Dissipation	1	W	1
I <sub>OS</sub>	Short Circuit Output Current	50	mA	1

Note1: Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage of the devices

Note2: These voltages are relative to V<sub>SS</sub>

**Table 13. Recommended D.C. Operating Conditions (T<sub>A</sub> = -40 ~ 85 °C)**

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	2.375	2.625	V	1,2
Power Supply Voltage (for I/O Buffer)	V <sub>DDQ</sub>	2.375	2.625	V	1,2
Input Reference Voltage	V <sub>REF</sub>	0.49* V <sub>DDQ</sub>	0.51* V <sub>DDQ</sub>	V	
Termination Voltage	V <sub>TT</sub>	V <sub>REF</sub> - 0.04	V <sub>REF</sub> + 0.04	V	
Input High Voltage (DC)	V <sub>IH</sub> (DC)	V <sub>REF</sub> + 0.15	V <sub>DDQ</sub> + 0.3	V	
Input Low Voltage (DC)	V <sub>IL</sub> (DC)	-0.3	V <sub>REF</sub> - 0.15	V	
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	V <sub>IN</sub> (DC)	-0.3	V <sub>DDQ</sub> + 0.3	V	1,2
Input Leakage current	I <sub>I</sub>	-5	5	μA	
Output Leakage current	I <sub>OZ</sub>	-5	5	μA	
Output High Voltage	V <sub>OH</sub>	V <sub>TT</sub> + 0.76	-	V	I <sub>OH</sub> = -15.2 mA
Output Low Voltage	V <sub>OL</sub>	-	V <sub>TT</sub> - 0.76	V	I <sub>OL</sub> = +15.2mA

**Table 14. Capacitance (V<sub>DD</sub> = 2.5V±5%, f = 1MHz, T<sub>A</sub> = 25 °C)**

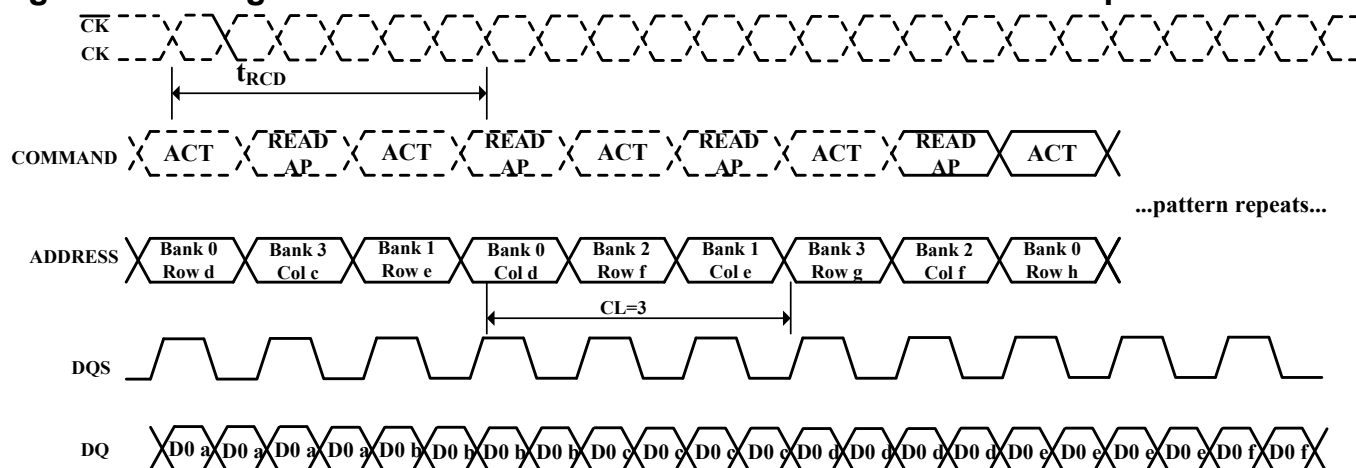
Symbol	Parameter	Min.	Max.	Unit
C <sub>IN1</sub>	Input Capacitance (CK, $\overline{\text{CK}}$ )	2	4	pF
C <sub>IN2</sub>	Input Capacitance (All other input-only pins)	2	4	pF
C <sub>I/O</sub>	DQ, DQS, DM Input/Output Capacitance	4	6	pF

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested

**Table 15. D.C. Characteristics** ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40 \sim 85^\circ C$ )

Parameter & Test Condition	Symbol	-5	Unit
		Max.	
<b>OPERATING CURRENT:</b> One bank; Active-Precharge; $t_{RC}=t_{RC}(\min)$ ; $t_{CK}=t_{CK}(\min)$ ; DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	120	mA
<b>OPERATING CURRENT :</b> One bank; Active-Read-Precharge; BL=4; $t_{RC}=t_{RC}(\min)$ ; $t_{CK}=t_{CK}(\min)$ ; $I_{out}=0mA$ ; Address and control inputs changing once per clock cycle	IDD1	140	mA
<b>PRECHARGE POWER-DOWN STANDBY CURRENT:</b> All banks idle; power-down mode; $t_{CK}=t_{CK}(\min)$ ; CKE=LOW	IDD2P	10	mA
<b>IDLE STANDLY CURRENT :</b> CKE = HIGH; $\overline{CS}$ =HIGH(DESELECT); All banks idle; $t_{CK}=t_{CK}(\min)$ ; Address and control inputs changing once per clock cycle; $V_{IN}=V_{REF}$ for DQ, DQS and DM	IDD2N	50	mA
<b>ACTIVE POWER-DOWN STANDBY CURRENT :</b> one bank active; power-down mode; CKE=LOW; $t_{CK}=t_{CK}(\min)$	IDD3P	40	mA
<b>ACTIVE STANDBY CURRENT :</b> $\overline{CS}$ =HIGH;CKE=HIGH; one bank active ; $t_{RC}=t_{RC}(\max)$ ; $t_{CK}=t_{CK}(\min)$ ;Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	80	mA
<b>OPERATING CURRENT BURST READ :</b> BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; $t_{CK}=t_{CK}(\min)$ ; $I_{out}=0mA$ ;50% of data changing on every transfer	IDD4R	180	mA
<b>OPERATING CURRENT BURST Write :</b> BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; $t_{CK}=t_{CK}(\min)$ ; DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	180	mA
<b>AUTO REFRESH CURRENT :</b> $t_{RC}=t_{RFC}(\min)$ ; $t_{CK}=t_{CK}(\min)$	IDD5	200	mA
<b>SELF REFRESH CURRENT:</b> Self Refresh Mode ; CKE $\leq 0.2V$ ; $t_{CK}=t_{CK}(\min)$	IDD6	4	mA
<b>BURST OPERATING CURRENT 4 bank operation:</b> Four bank interleaving READs; BL=4;with Auto Precharge; $t_{RC}=t_{RC}(\min)$ ; $t_{CK}=t_{CK}(\min)$ ; Address and control inputs change only during Active, READ , or WRITE command	IDD7	300	mA

**Figure 3: Timing Waveform for IDD7 Measurement at 200 MHz CK Operation**



**Table 16. Electrical AC Characteristics ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40 \sim 85^\circ C$ )**

Symbol	Parameter		-5		Unit
			Min	Max	
t <sub>CK</sub>	Clock cycle time	CL=2	7.5	12	ns
		CL=2.5	6	12	ns
		CL = 3	5	12	ns
t <sub>CH</sub>	Clock high level width		0.45	0.55	t <sub>CK</sub>
t <sub>CL</sub>	Clock low level width		0.45	0.55	t <sub>CK</sub>
t <sub>DQSK</sub>	DQS-out access time from CK, $\overline{CK}$		-0.6	0.6	ns
t <sub>AC</sub>	Output access time from CK, $\overline{CK}$		-0.7	0.7	ns
t <sub>DQSQ</sub>	DQS-DQ Skew		-	0.4	ns
t <sub>RPRE</sub>	Read preamble		0.9	1.1	t <sub>CK</sub>
t <sub>RPST</sub>	Read postamble		0.4	0.6	t <sub>CK</sub>
t <sub>DQSS</sub>	CK to valid DQS-in		0.72	1.25	t <sub>CK</sub>
t <sub>WPRES</sub>	DQS-in setup time		0	-	ns
t <sub>WPRE</sub>	DQS write preamble		0.25	-	t <sub>CK</sub>
t <sub>WPST</sub>	DQS write postamble		0.4	0.6	t <sub>CK</sub>
t <sub>DQSH</sub>	DQS in high level pulse width		0.35	-	t <sub>CK</sub>
t <sub>DQSL</sub>	DQS in low level pulse width		0.35	-	t <sub>CK</sub>
t <sub>IS</sub>	Address and Control input setup time	Fast slew rate	0.6	-	ns
		Slow slew rate	0.7	-	
t <sub>IH</sub>	Address and Control input hold time	Fast slew rate	0.6	-	
		Slow slew rate	0.7	-	
t <sub>DS</sub>	DQ & DM setup time to DQS		0.4	-	ns
t <sub>DH</sub>	DQ & DM hold time to DQS		0.4	-	ns
t <sub>HP</sub>	Clock half period		t <sub>CLMIN</sub> or t <sub>CHMIN</sub>	-	ns
t <sub>QH</sub>	DQ/DQS output hold time from DQS		t <sub>HP</sub> - t <sub>QHS</sub>	-	ns
t <sub>RC</sub>	Row cycle time		60	-	ns
t <sub>RFC</sub>	Refresh row cycle time		70	-	ns
t <sub>RAS</sub>	Row active time		40	70K	ns
t <sub>RCD</sub>	Active to Read or Write delay		18	-	ns
t <sub>RP</sub>	Row precharge time		18	-	ns
t <sub>RRD</sub>	Row active to Row active delay		10	-	ns
t <sub>WR</sub>	Write recovery time		15	-	ns
t <sub>MRD</sub>	Mode register set cycle time		2	-	t <sub>CK</sub>
t <sub>CCD</sub>	Col. Address to Col. Address delay		1	-	t <sub>CK</sub>
t <sub>DAL</sub>	Auto precharge write recovery + Precharge time		7	-	t <sub>CK</sub>
t <sub>XS RD</sub>	Self refresh exit to read command delay		200	-	t <sub>CK</sub>
t <sub>PDEX</sub>	Power down exit time		t <sub>CK</sub> + t <sub>IS</sub>	-	ns
t <sub>REFI</sub>	Refresh interval time		-	15.6	μs
t <sub>IPW</sub>	Control and Address input pulse width		2.2	-	ns
t <sub>DIPW</sub>	DQ & DM input pulse width (for each input)		1.75	-	ns
t <sub>HZ</sub>	Data-out high-impedance window from CK, $\overline{CK}$		-	0.7	ns
t <sub>LZ</sub>	Data-out low-impedance window from CK, $\overline{CK}$		-0.7	0.7	ns
t <sub>QHS</sub>	Data Hold Skew Factor		-	0.5	ns
t <sub>DSS</sub>	DQS falling edge to CK rising – setup time		0.2	-	t <sub>CK</sub>
t <sub>DSH</sub>	DQS falling edge to CK rising – hold time		0.2	-	t <sub>CK</sub>

t <sub>WTR</sub>	Internal Write to Read command delay	2	-	t <sub>CK</sub>
t <sub>XSNR</sub>	Exit Self-Refresh to non-Read command	75	-	ns
t <sub>RAP</sub>	Active to Autoprecharge delay	t <sub>RASmin</sub>	-	ns

**Table 17. Recommended A.C. Operating Conditions (V<sub>DD</sub> = 2.5V ± 5%, T<sub>A</sub> = -40~85 °C)**

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (AC)	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.35	-	V
Input Low Voltage (AC)	V <sub>IL</sub> (AC)	-	V <sub>REF</sub> - 0.35	V
Input Different Voltage, CK and $\overline{CK}$ inputs	V <sub>ID</sub> (AC)	0.7	V <sub>DDQ</sub> + 0.6	V
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V <sub>IX</sub> (AC)	0.5*V <sub>DDQ</sub> -0.2	0.5*V <sub>DDQ</sub> +0.2	V

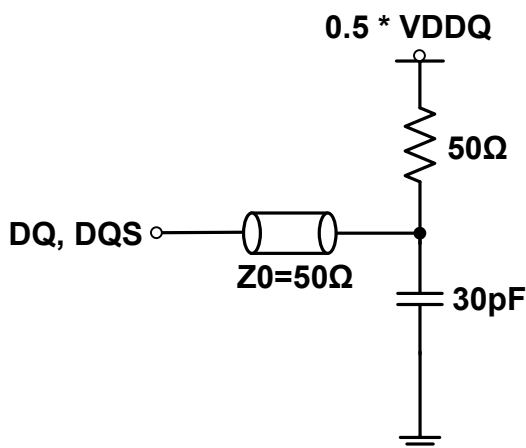
**Note:**

1. All voltages are referenced to V<sub>SS</sub>.
2. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t<sub>CK</sub> and t<sub>RC</sub>. Input signals are changed one time during t<sub>CK</sub>.
3. Power-up sequence is described in Note 5.
4. A.C. Test Conditions

**Table 18. SSTL\_2 Interface**

Reference Level of Output Signals (V <sub>REF</sub> )	0.5 * V <sub>DDQ</sub>
Output Load	Reference to the Test Load
Input Signal Levels(V <sub>IH</sub> / V <sub>IL</sub> )	V <sub>REF</sub> +0.35 V / V <sub>REF</sub> -0.35V
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 * V <sub>DDQ</sub>

**Figure 4. SSTL\_2 A.C. Test Load**



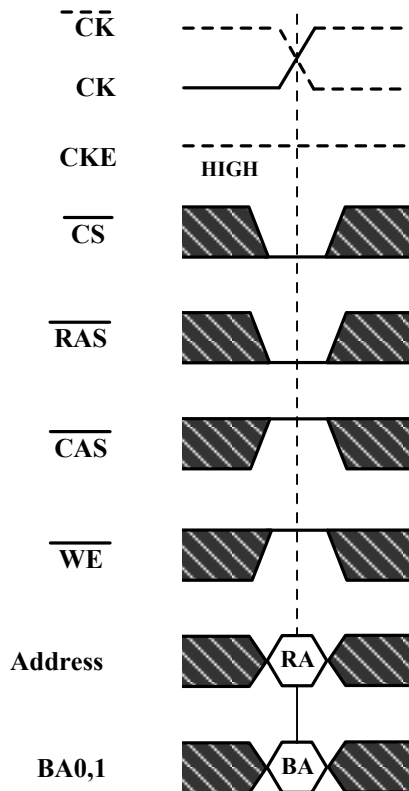
## 5. Power up Sequence

Power up must be performed in the following sequence.

- 1) Apply power to  $V_{DD}$  before or at the same time as  $V_{DDQ}$ ,  $V_{TT}$  and  $V_{REF}$  when all input signals are held "NOP" state and maintain CKE "LOW".
- 2) Start clock and maintain stable condition for minimum 200 $\mu$ s.
- 3) Issue a "NOP" command and keep CKE "HIGH"
- 4) Issue a "Precharge All" command.
- 5) Issue EMRS – enable DLL.
- 6) Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
- 7) Precharge all banks of the device.
- 8) Issue two or more Auto Refresh commands.
- 9) Issue MRS – with A8 to low to initialize the mode register.

## Timing Waveforms

Figure 5. Activating a Specific Row in a Specific Bank



RA=Row Address

BA=Bank Address

 Don't Care



Figure 6. tRCD and tRRD Definition

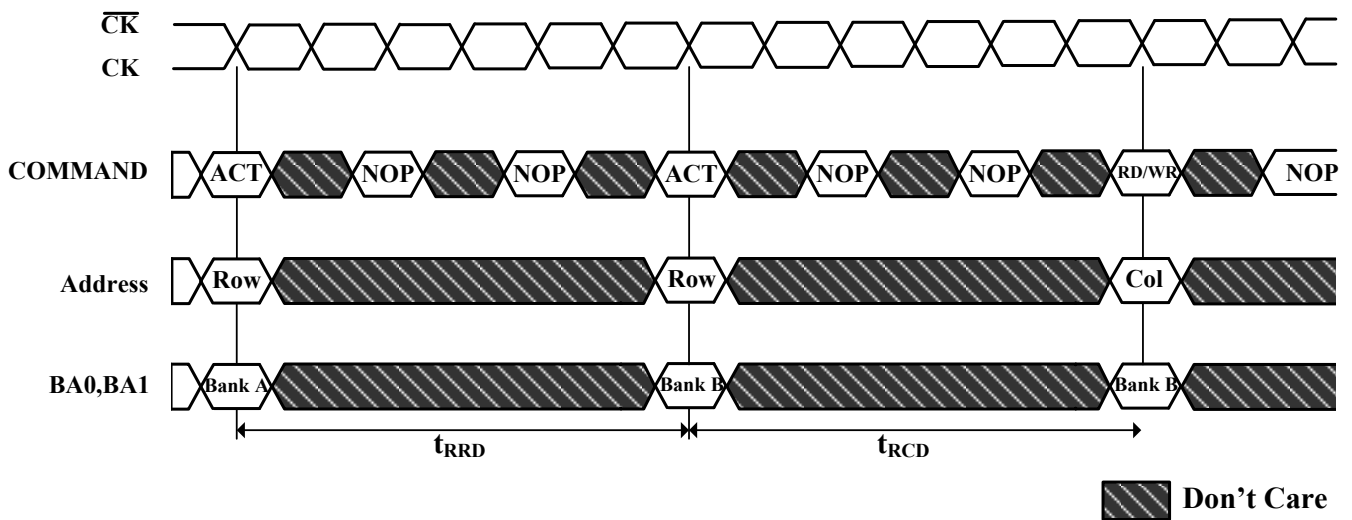
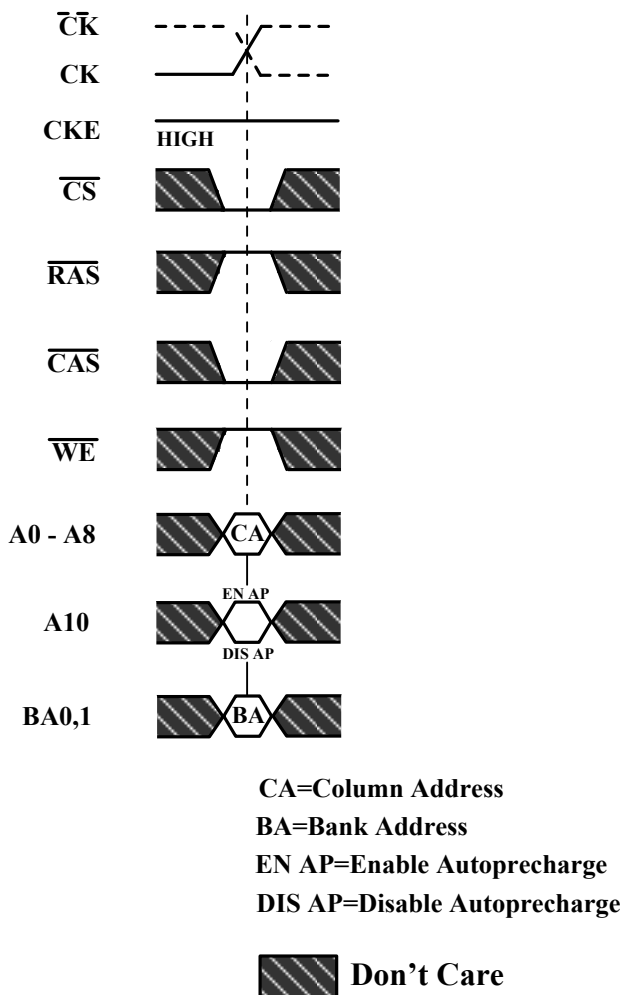
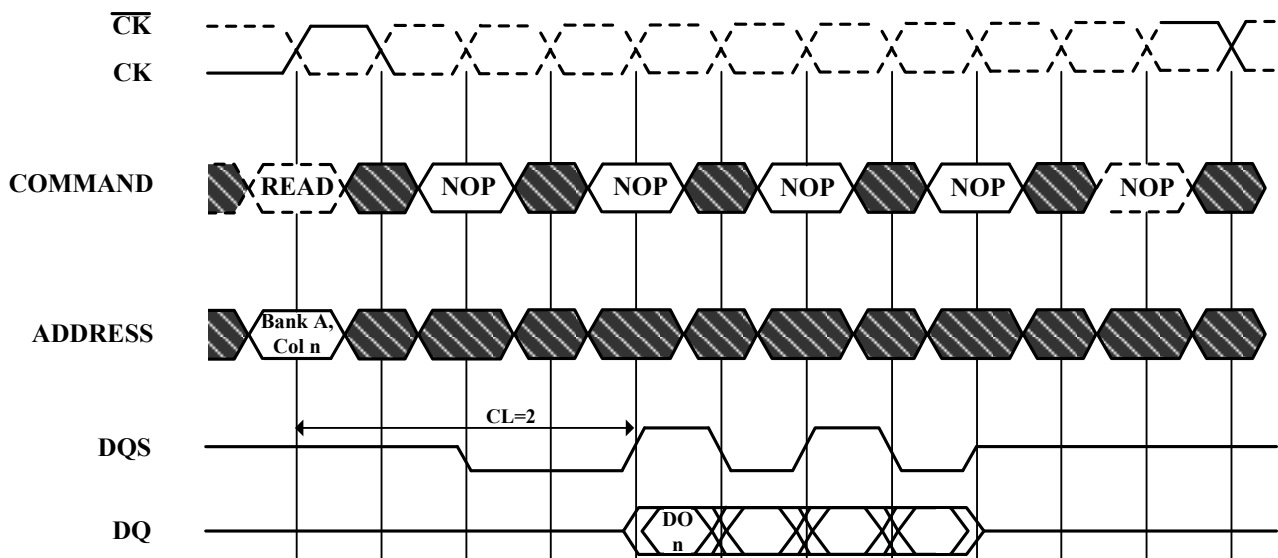


Figure 7. READ Command



**Figure 8. Read Burst Required CAS Latencies (CL=2)**



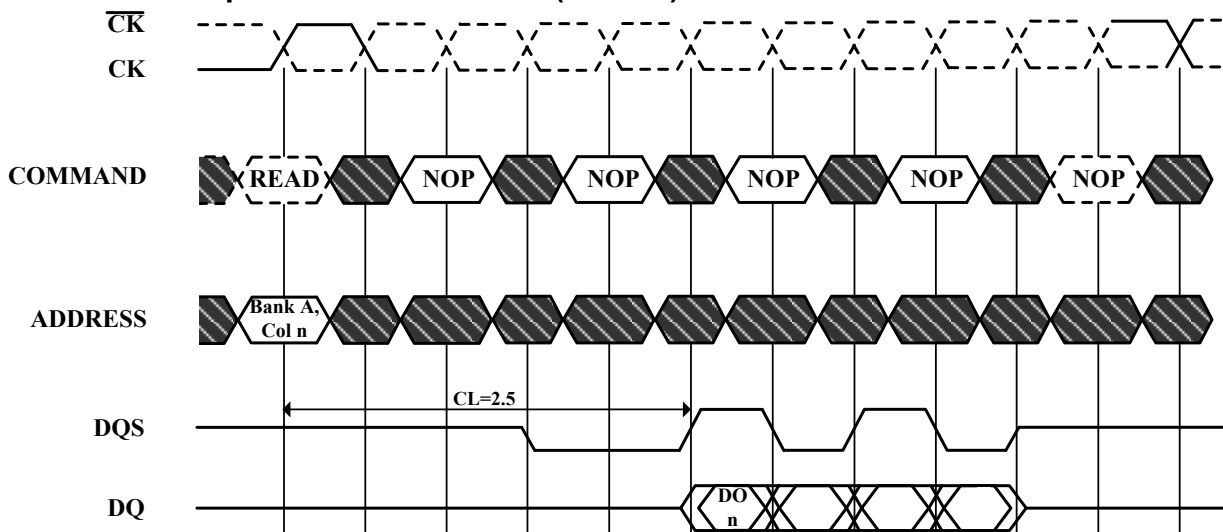
DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

**Read Burst Required CAS Latencies (CL=2.5)**



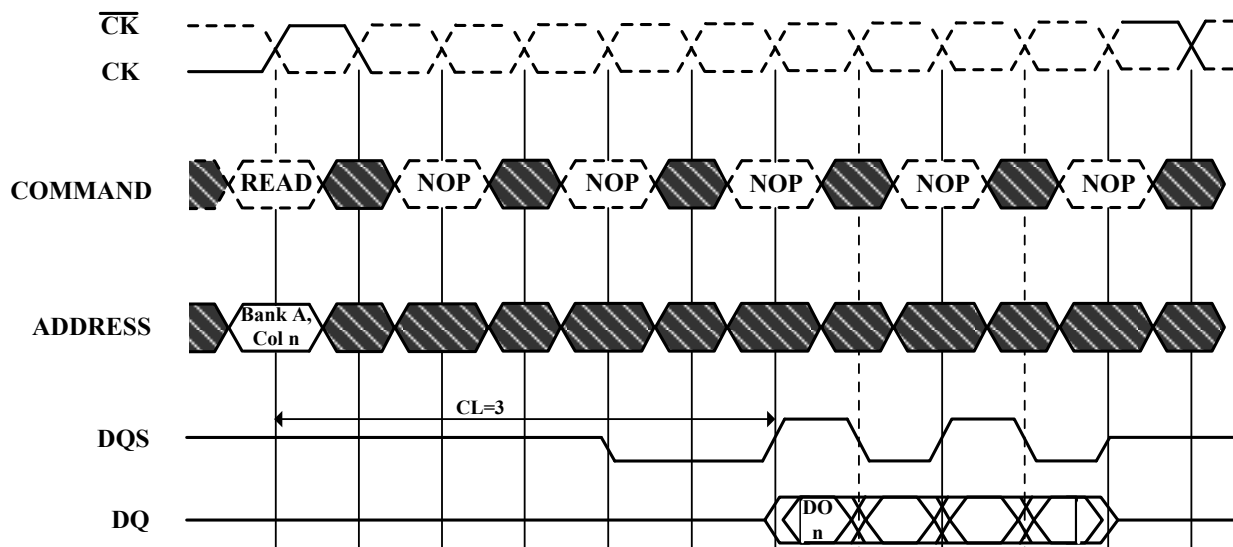
DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

## Read Burst Required CAS Latencies (CL=3)



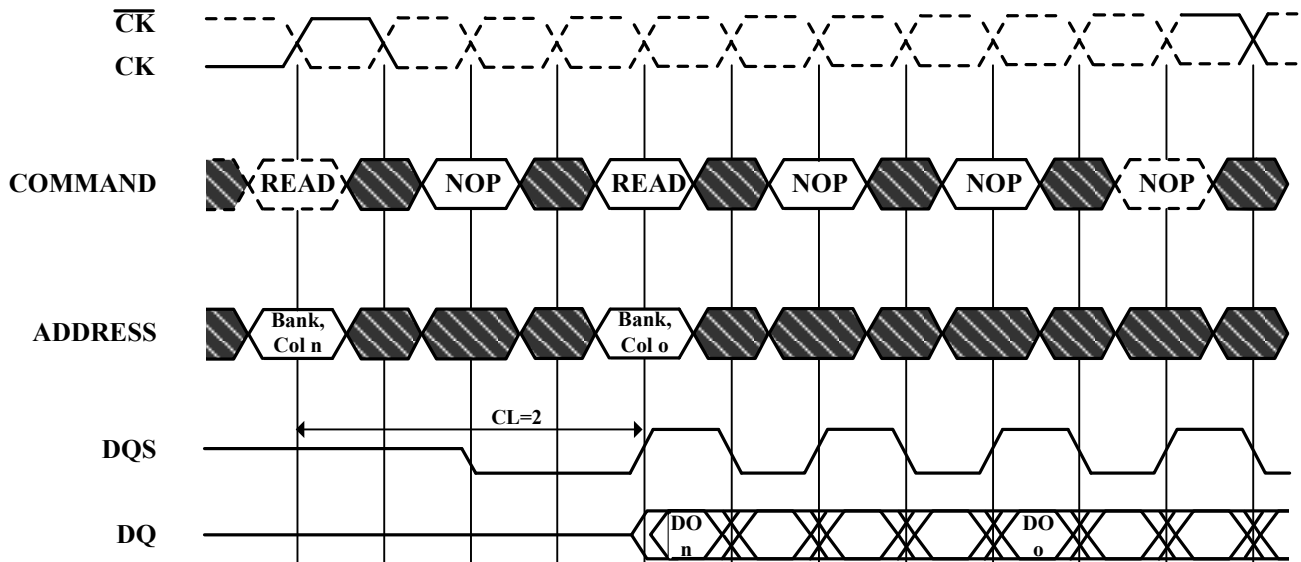
DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

**Figure 9. Consecutive Read Bursts Required CAS Latencies (CL=2)**



**DO n (or o)=Data Out from column n (or column o)**

**Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)**

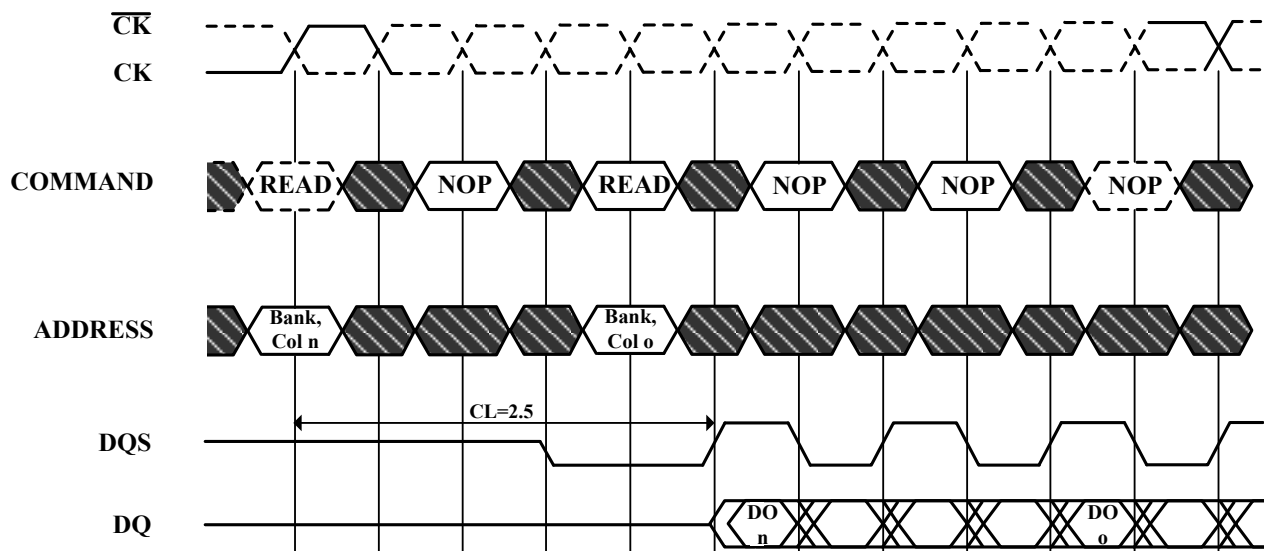
**3 subsequent elements of Data Out appear in the programmed order following DO n**

**3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o**

**Read commands shown must be to the same device**

 **Don't Care**

## Consecutive Read Bursts Required CAS Latencies (CL=2.5)



DO n (or o)=Data Out from column n (or column o)

Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

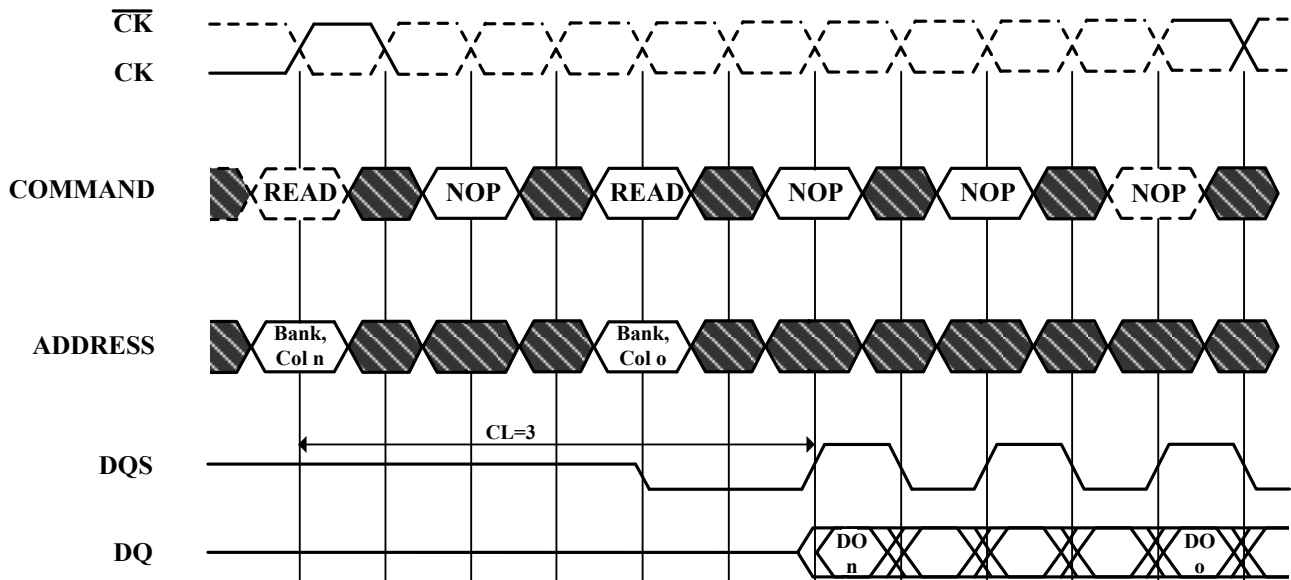
3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o

Read commands shown must be to the same device

 Don't Care

## Consecutive Read Bursts Required CAS Latencies (CL=3)



DO n (or o)=Data Out from column n (or column o)

Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

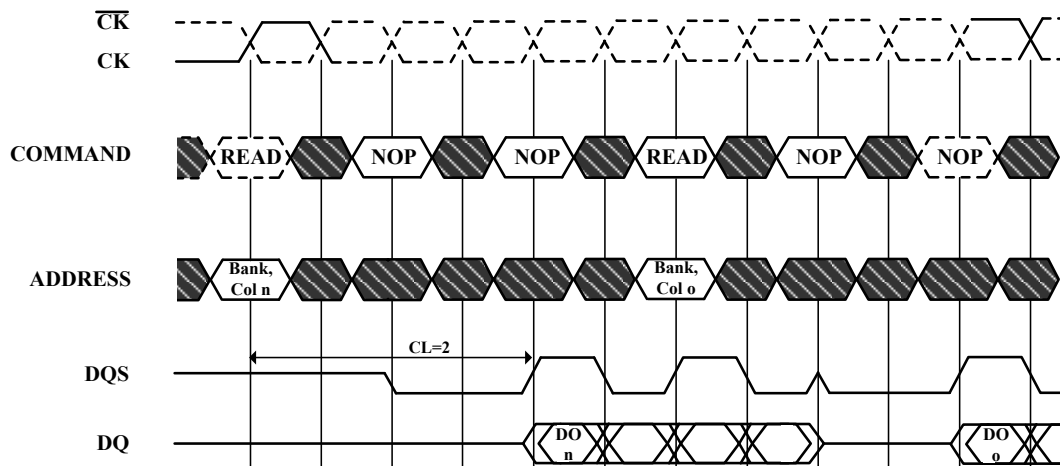
3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o

Read commands shown must be to the same device

 Don't Care

**Figure 10. Non-Consecutive Read Bursts Required CAS Latencies (CL=2)**



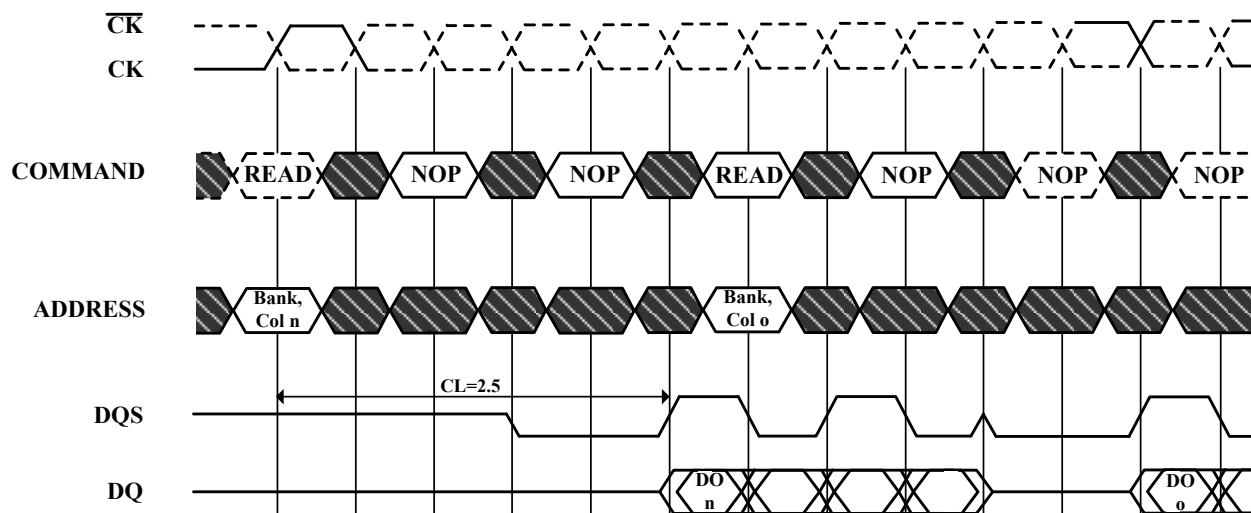
DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n  
(and following DO o)

 Don't Care

**Non-Consecutive Read Bursts Required CAS Latencies (CL=2.5)**



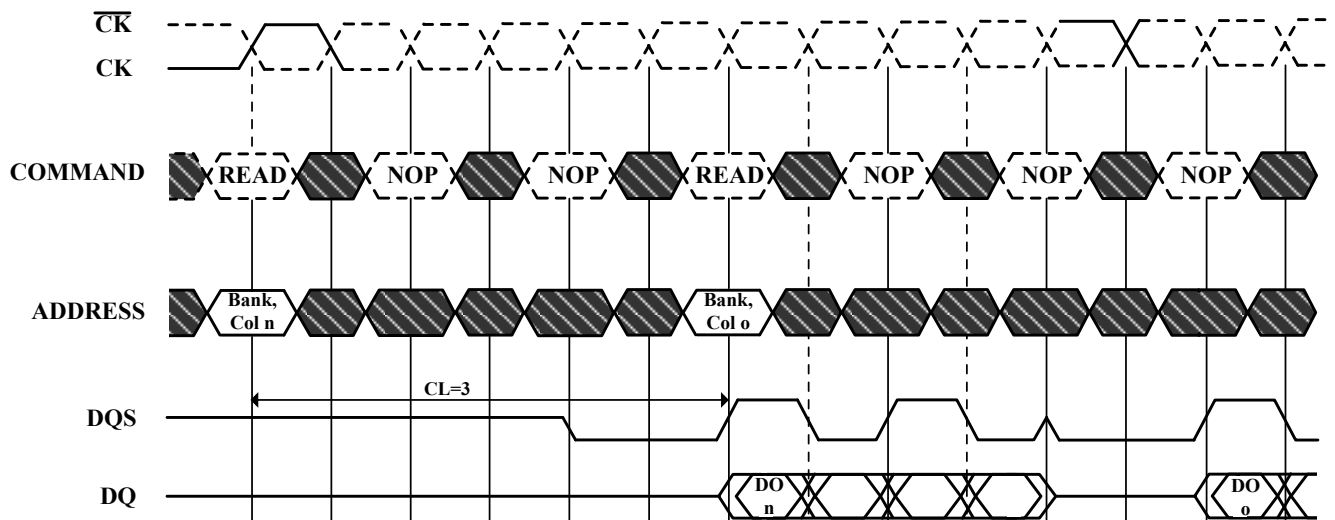
DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n  
(and following DO o)

 Don't Care

## Non-Consecutive Read Bursts Required CAS Latencies (CL=3)



DO n (or o)=Data Out from column n (or column o)

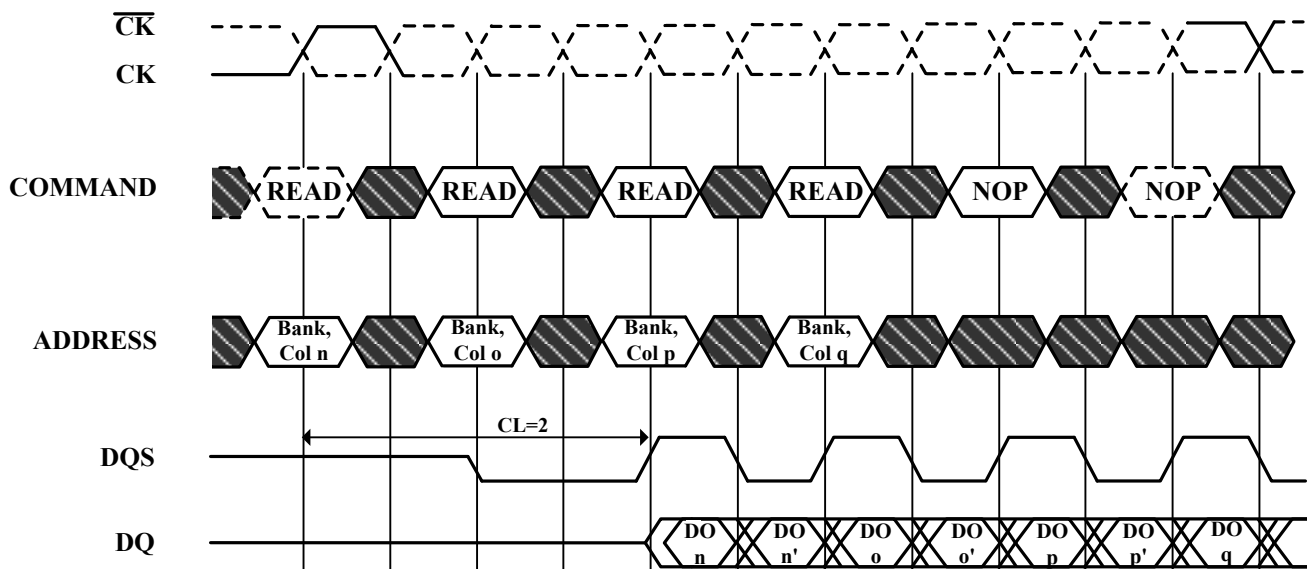
Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n  
(and following DO o)

 Don't Care



Figure 11. Random Read Accesses Required CAS Latencies (CL=2)



DO n, etc. =Data Out from column n, etc.

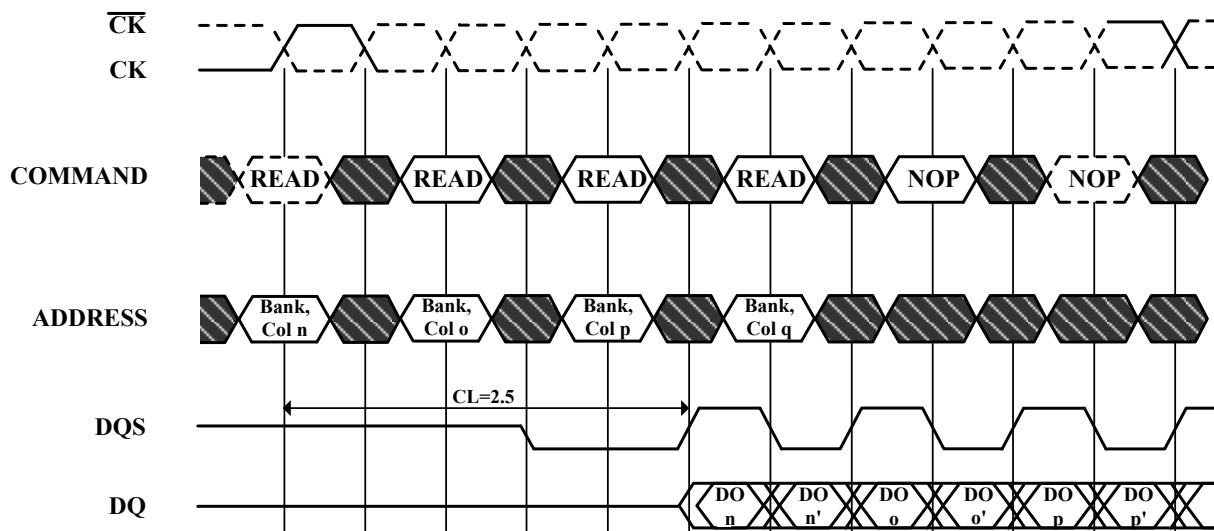
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

 Don't Care

## Random Read Accesses Required CAS Latencies (CL=2.5)



DO n, etc. =Data Out from column n, etc.

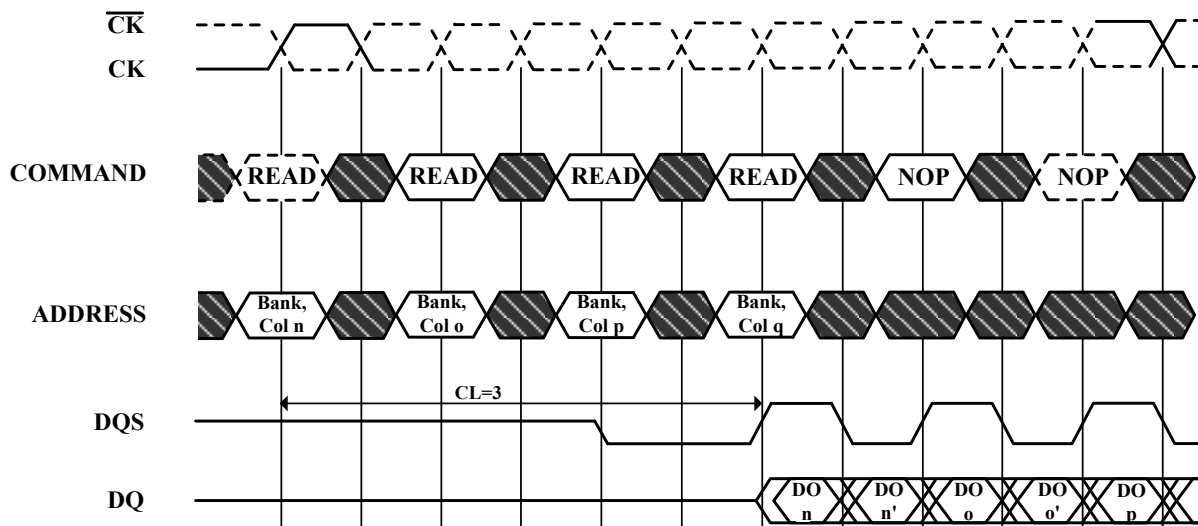
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

 Don't Care

## Random Read Accesses Required CAS Latencies (CL=3)



DO n, etc. =Data Out from column n, etc.

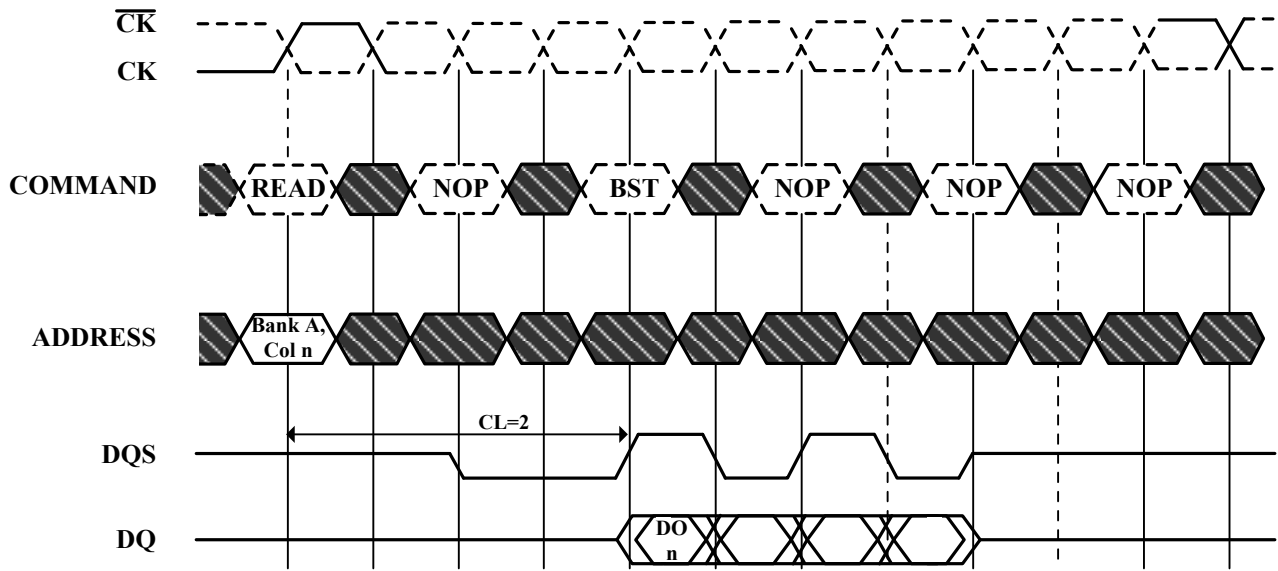
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

 Don't Care

Figure 12. Terminating a Read Burst Required CAS Latencies (CL=2)



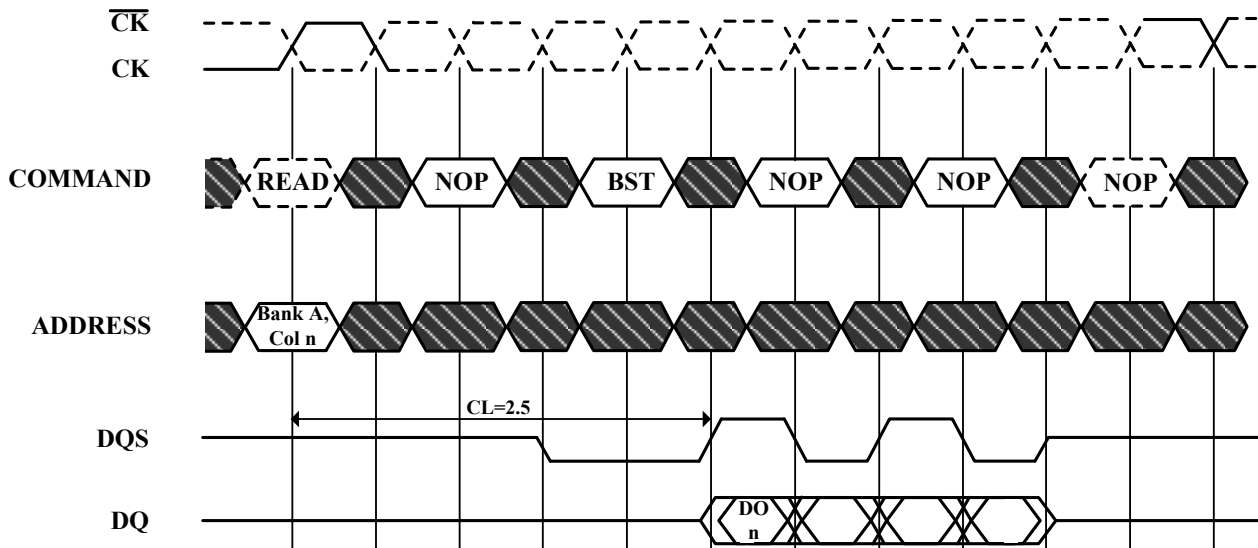
DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

## Terminating a Read Burst Required CAS Latencies (CL=2.5)



DO n = Data Out from column n

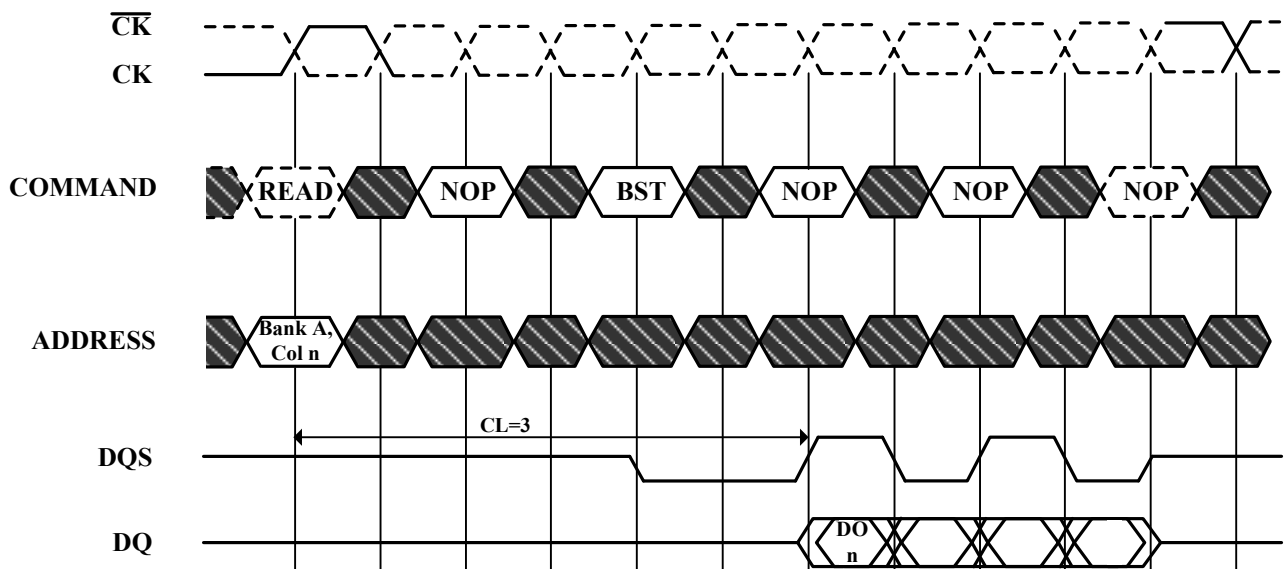
Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n



Don't Care

## Terminating a Read Burst Required CAS Latencies (CL=3)



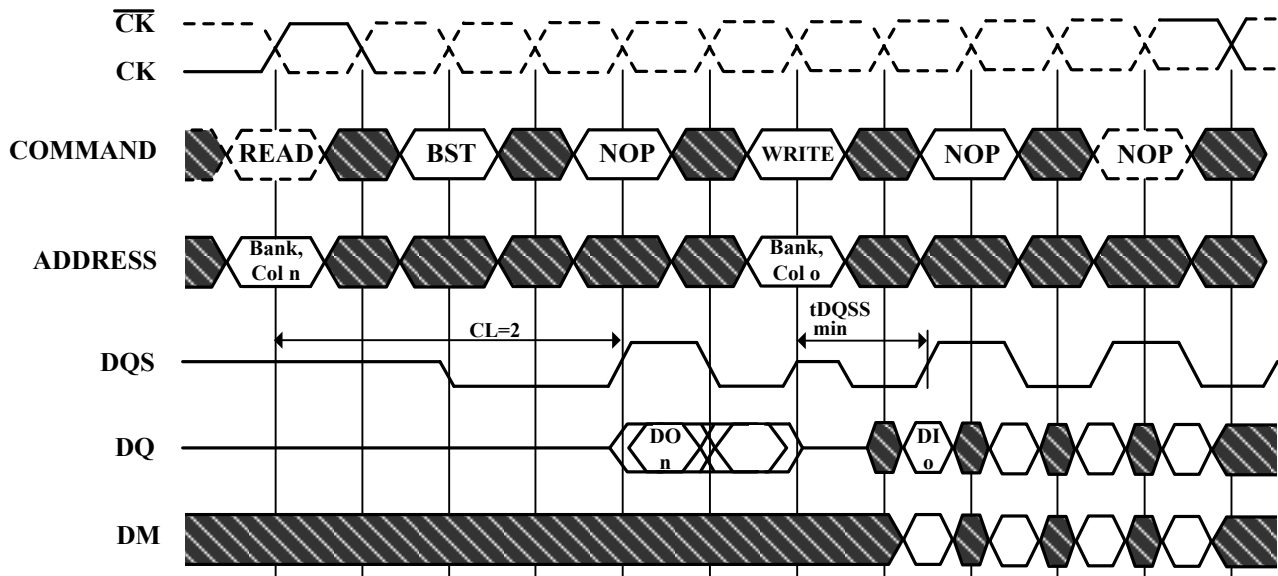
DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

Figure 13. Read to Write Required CAS Latencies (CL=2)



**DO n (or o) = Data Out from column n (or column o)**

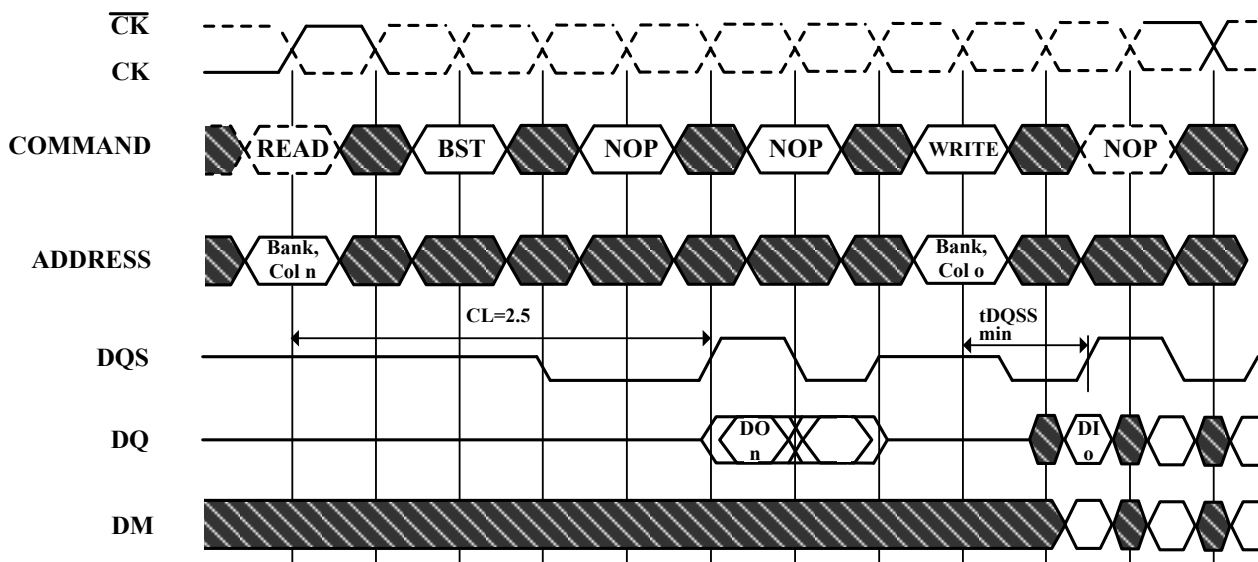
**Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)**

**1 subsequent element of Data Out appears in the programmed order following DO n**

**Data in elements are applied following DI o in the programmed order**

 **Don't Care**

## Read to Write Required CAS Latencies (CL=2.5)



DO n (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

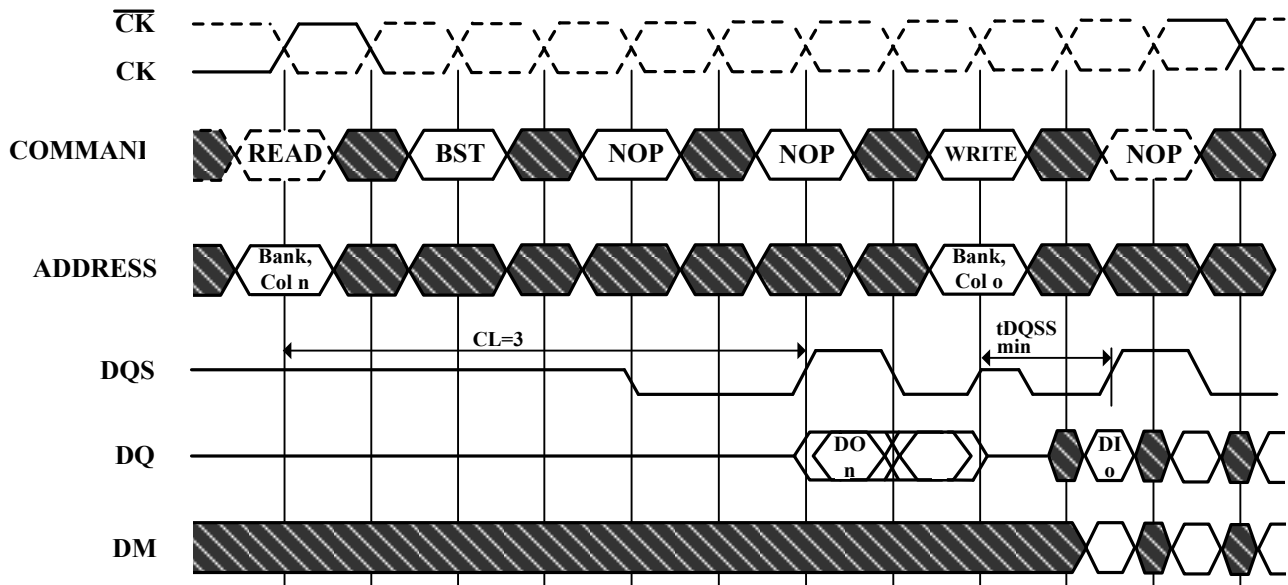
1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

 Don't Care



## Read to Write Required CAS Latencies (CL=3)



DO n (or o)= Data Out from column n (or column o)

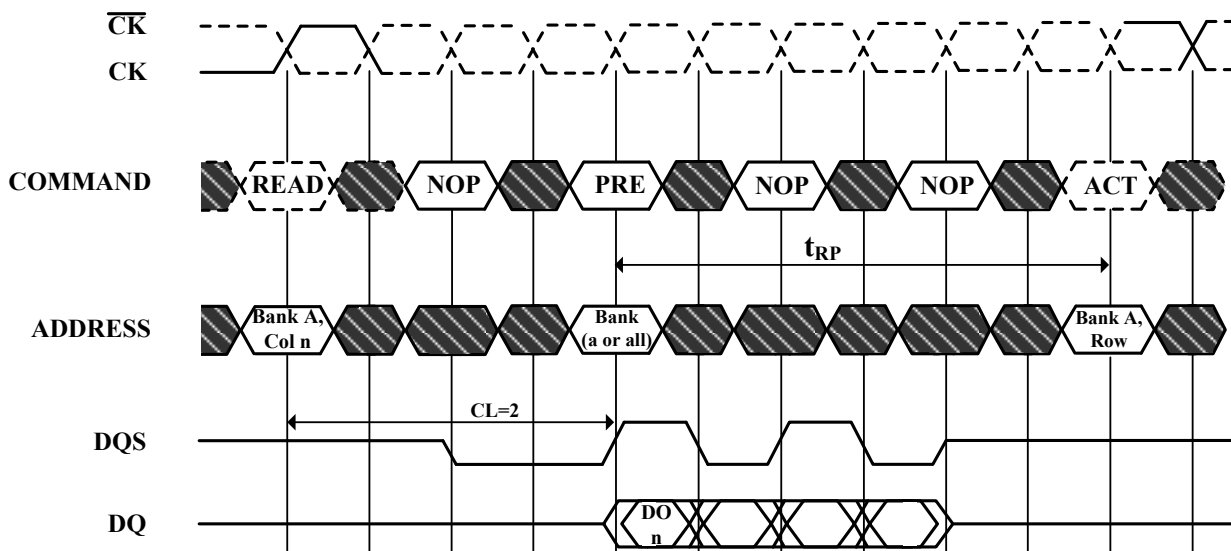
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

 Don't Care

Figure 14. Read to Precharge Required CAS Latencies (CL=2)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8  
 3 subsequent elements of Data Out appear in the programmed order  
 following DO n

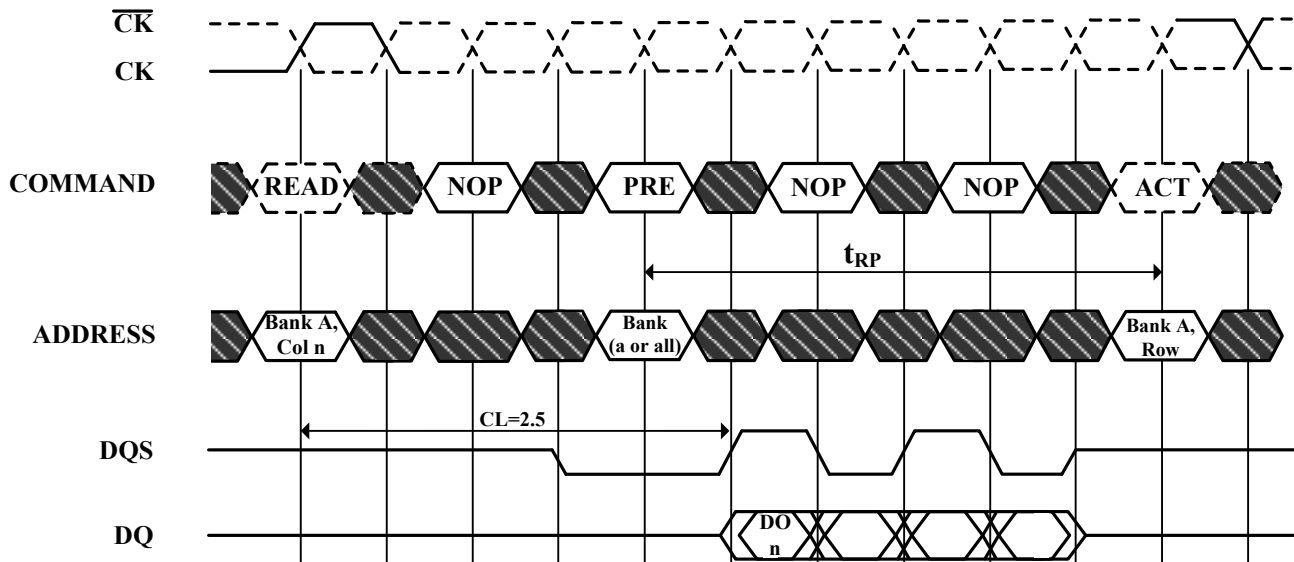
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE  
 command for applicable banks

The Active command may be applied if tRC has been met

 Don't Care

## Read to Precharge Required CAS Latencies (CL=2.5)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8  
3 subsequent elements of Data Out appear in the programmed order  
following DO n

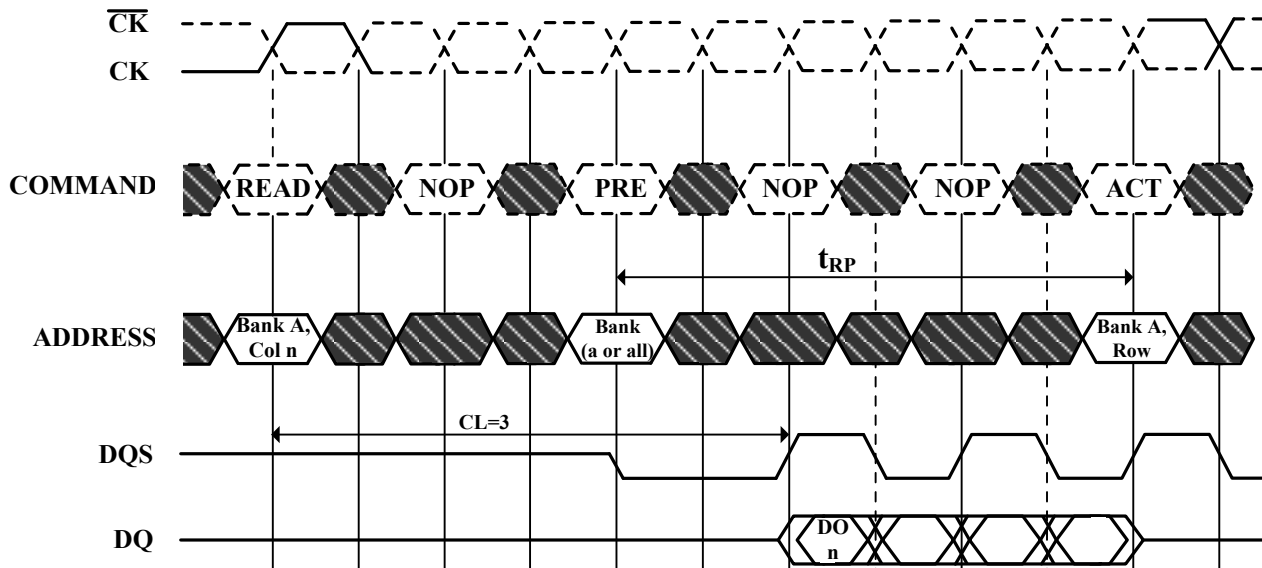
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE  
command for applicable banks

The Active command may be applied if tRC has been met

 Don't Care

## Read to Precharge Required CAS Latencies (CL=3)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8  
 3 subsequent elements of Data Out appear in the programmed order  
 following DO n

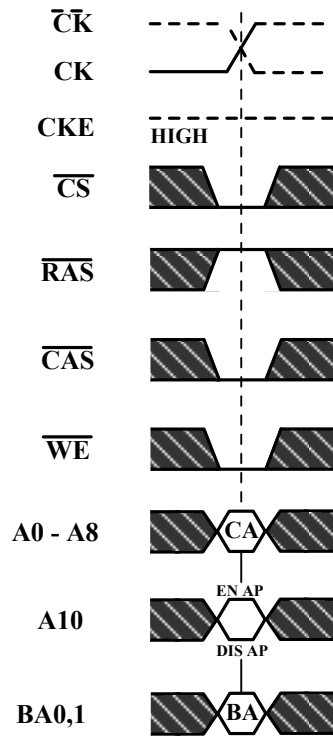
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE  
 command for applicable banks

The Active command may be applied if tRC has been met

 Don't Care

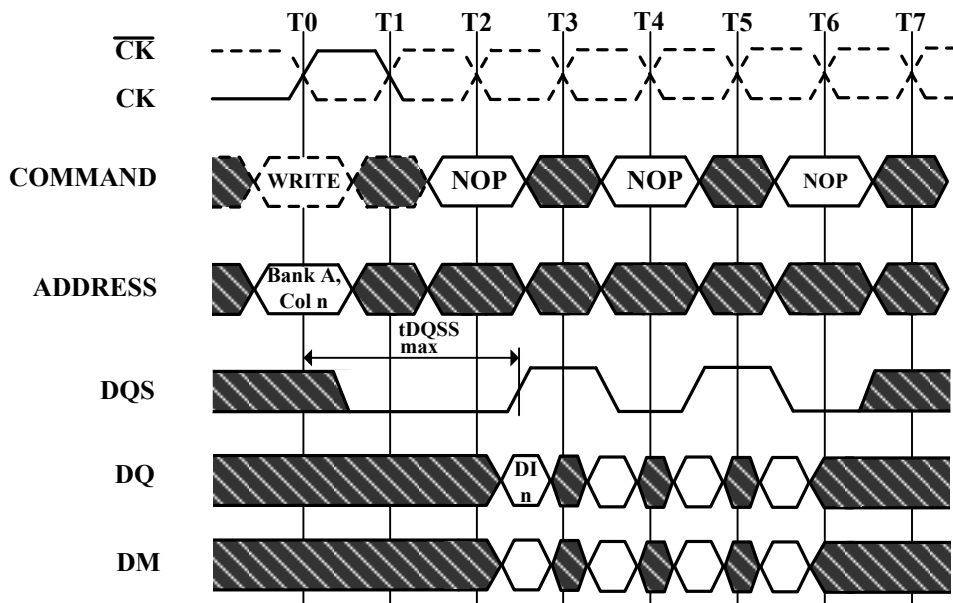
**Figure 15. Write Command**



CA=Column Address  
 BA=Bank Address  
 EN AP=Enable Autoprecharge  
 DIS AP=Disable Autoprecharge

 Don't Care

Figure 16. Write Max DQSS



DI n = Data In for column n

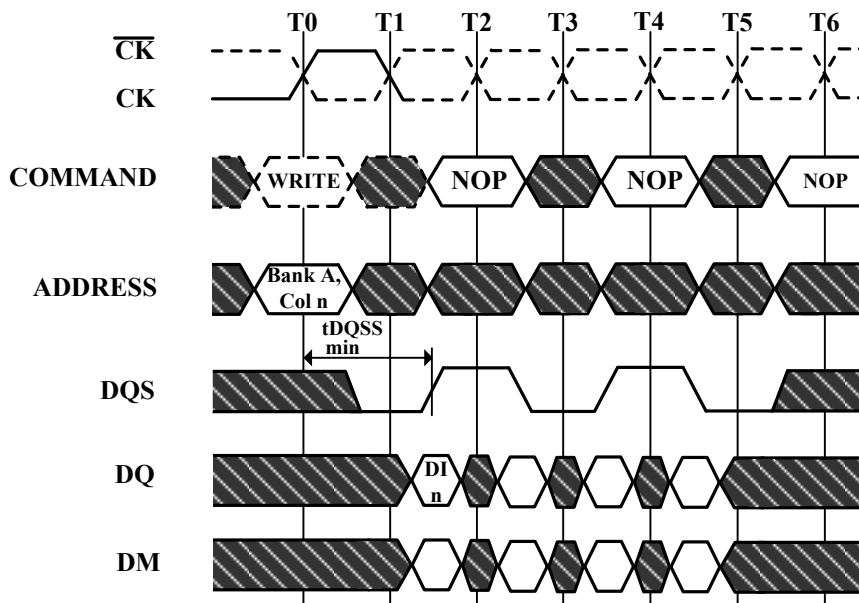
3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

 Don't Care

Figure 17. Write Min DQSS



DI n = Data In for column n

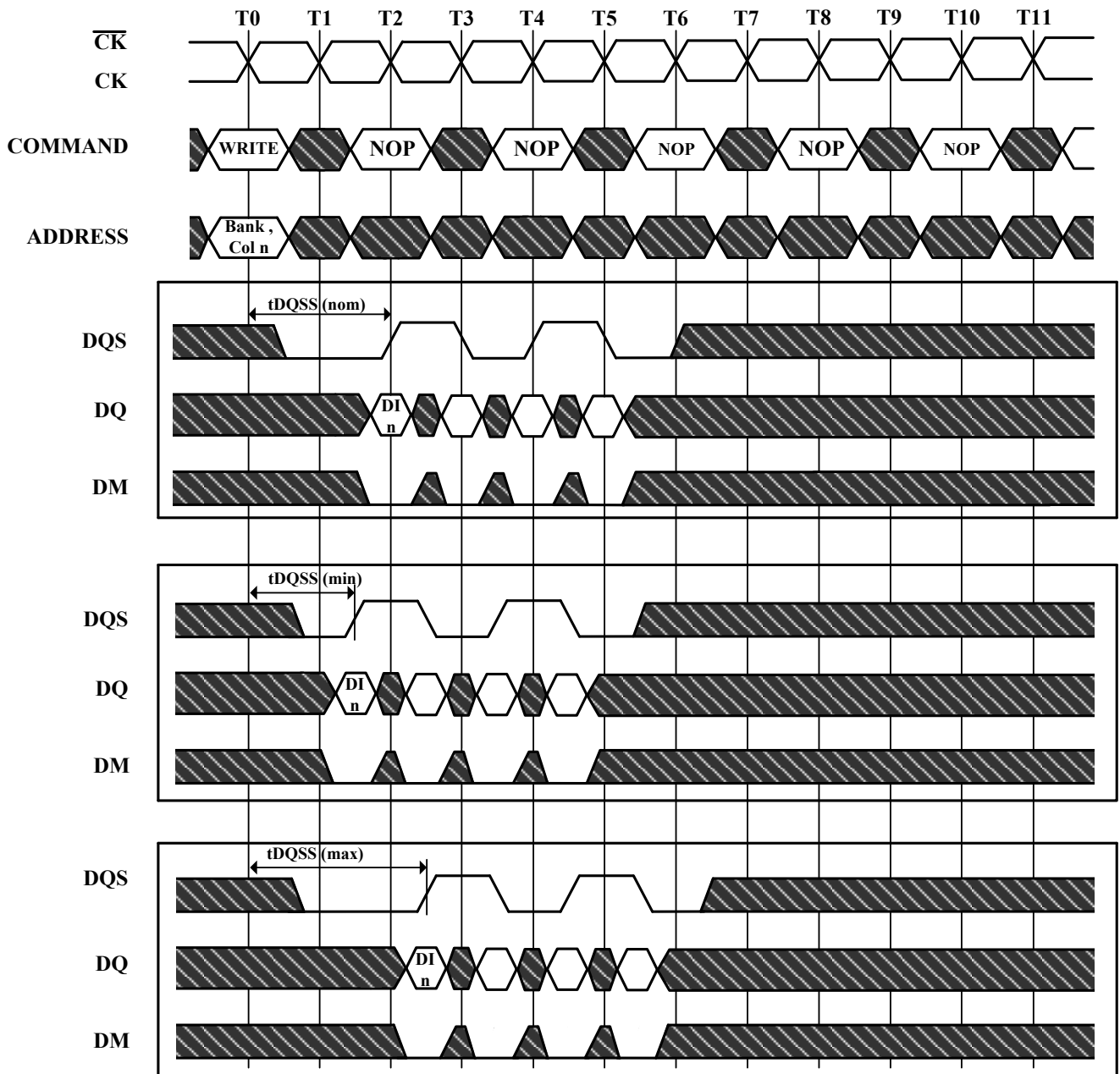
3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

 Don't Care

Figure 18. Write Burst Nom, Min, and Max tDQSS



DI n = Data In for column n

3 subsequent elements of Data are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

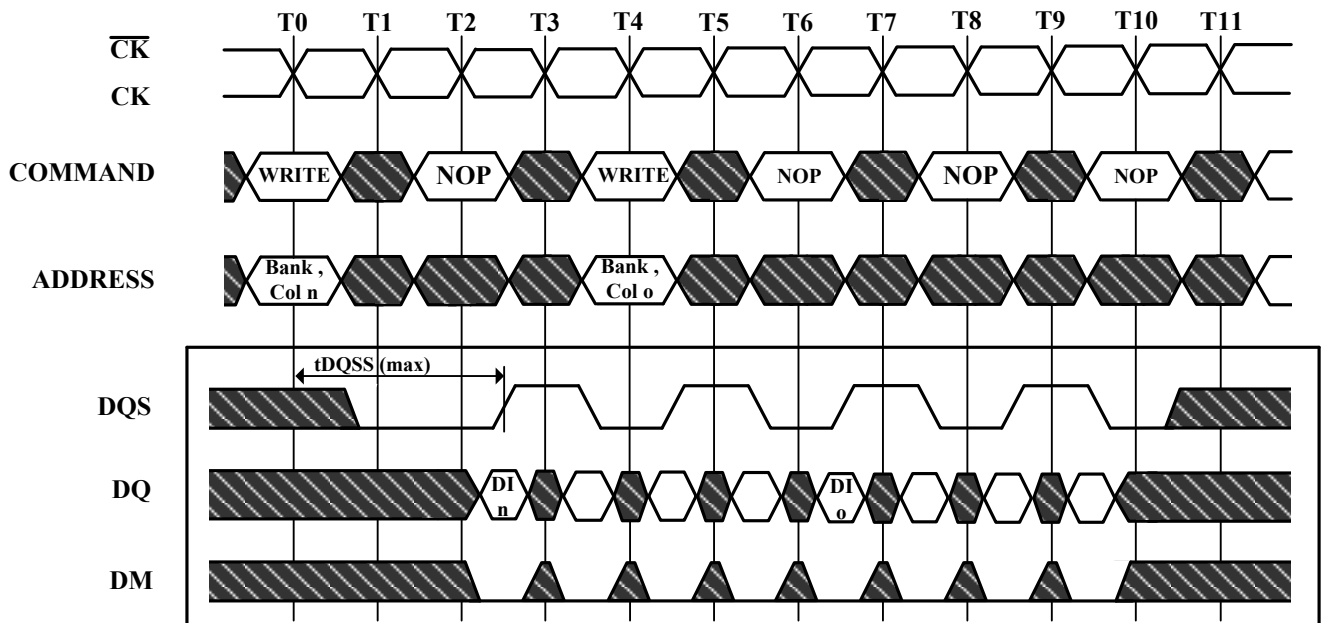
A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

DM=UDM & LDM

 Don't Care



Figure 19. Write to Write Max tDQSS



DI n , etc. = Data In for column n,etc.

3 subsequent elements of Data In are applied in the programmed order following DI n

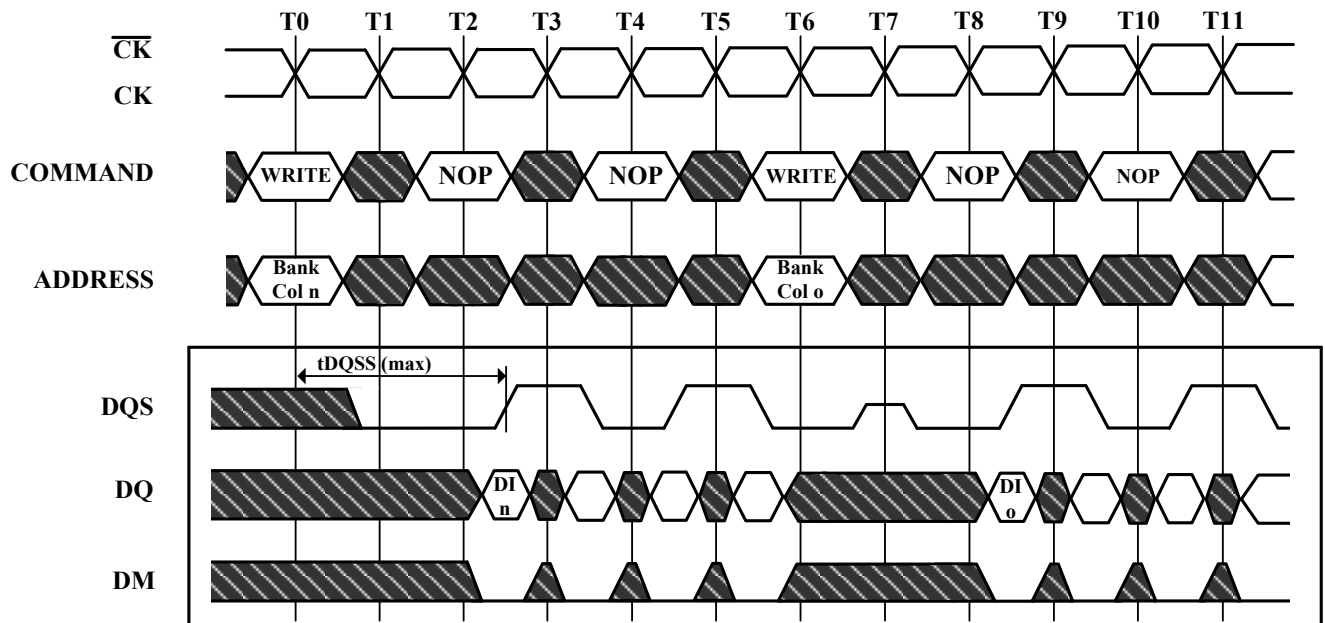
3 subsequent elements of Data In are applied in the programmed order following DI o

Non-interrupted bursts of 4 are shown

DM= UDM & LDM

 Don't Care

**Figure 20. Write to Write Max tDQSS, Non Consecutive**



DI n, etc. = Data In for column n, etc.

3 subsequent elements of Data In are applied in the programmed order following DI n

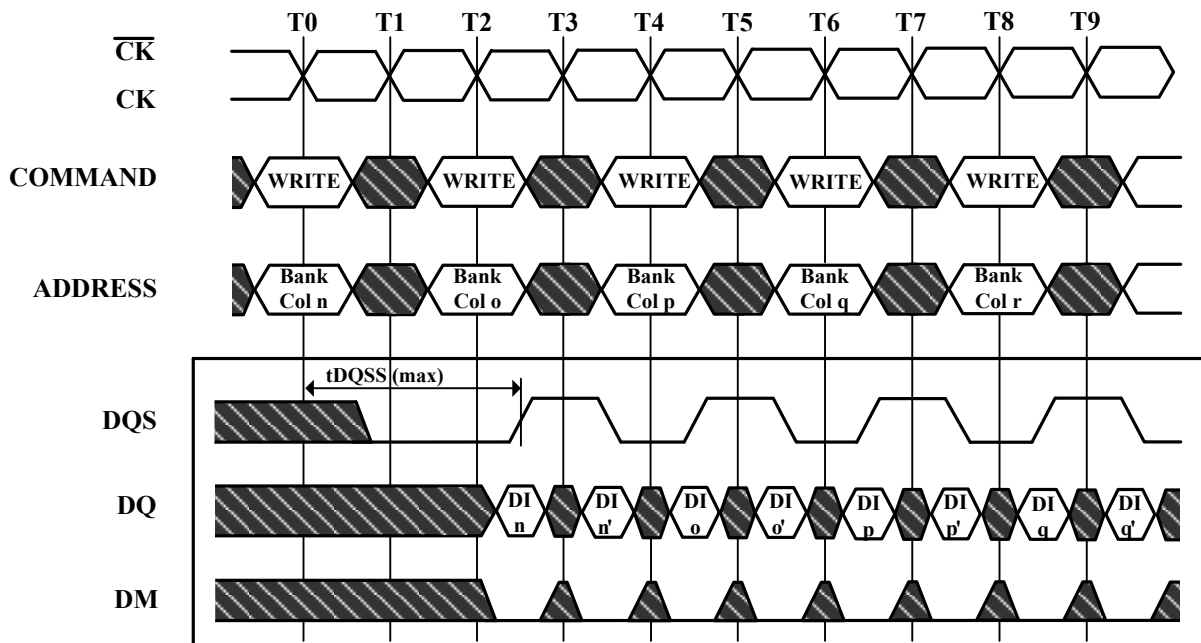
3 subsequent elements of Data In are applied in the programmed order following DI o

Non-interrupted bursts of 4 are shown

DM= UDM & LDM

 Don't Care

Figure 21. Random Write Cycles Max tDQSS



DI n, etc. = Data In for column n, etc.

n', etc. = the next Data In following DI n, etc. according to the programmed burst order

Programmed Burst Length 2, 4, or 8 in cases shown

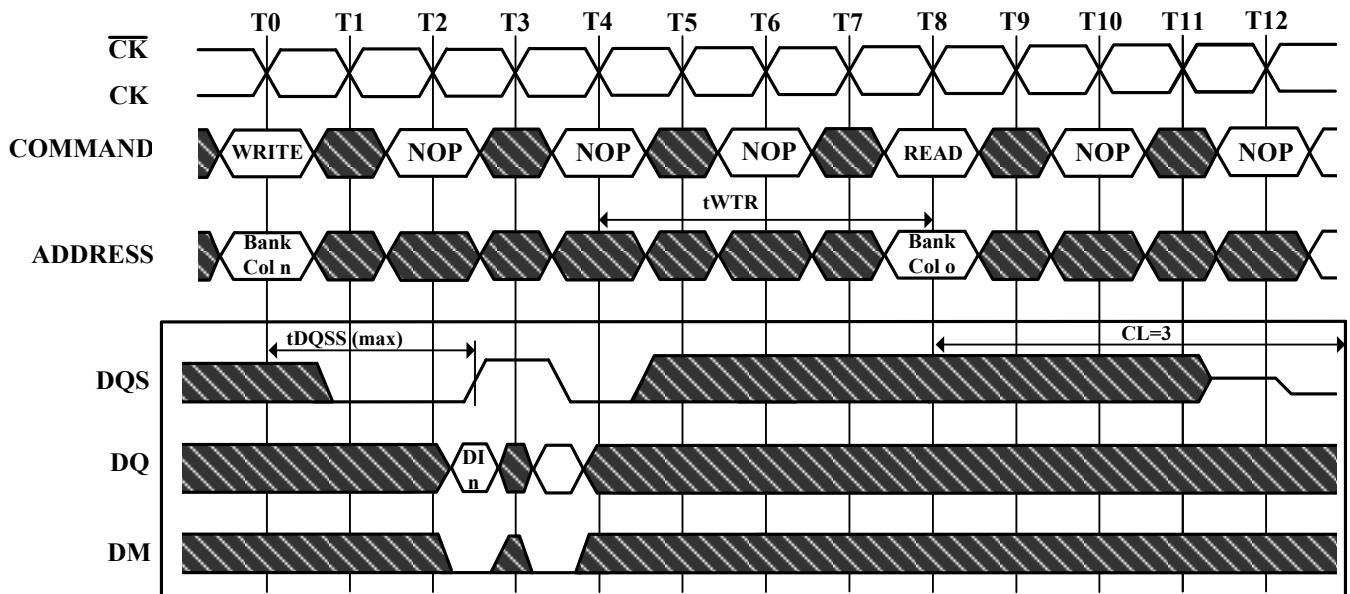
If burst of 4 or 8, the burst would be truncated

Each WRITE command may be to any bank and may be to the same or different devices

DM= UDM & LDM

 Don't Care

Figure 22. Write to Read Max tDQSS Non Interrupting



DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 2 is shown

tWTR is referenced from the first positive CK edge after the last Data In Pair

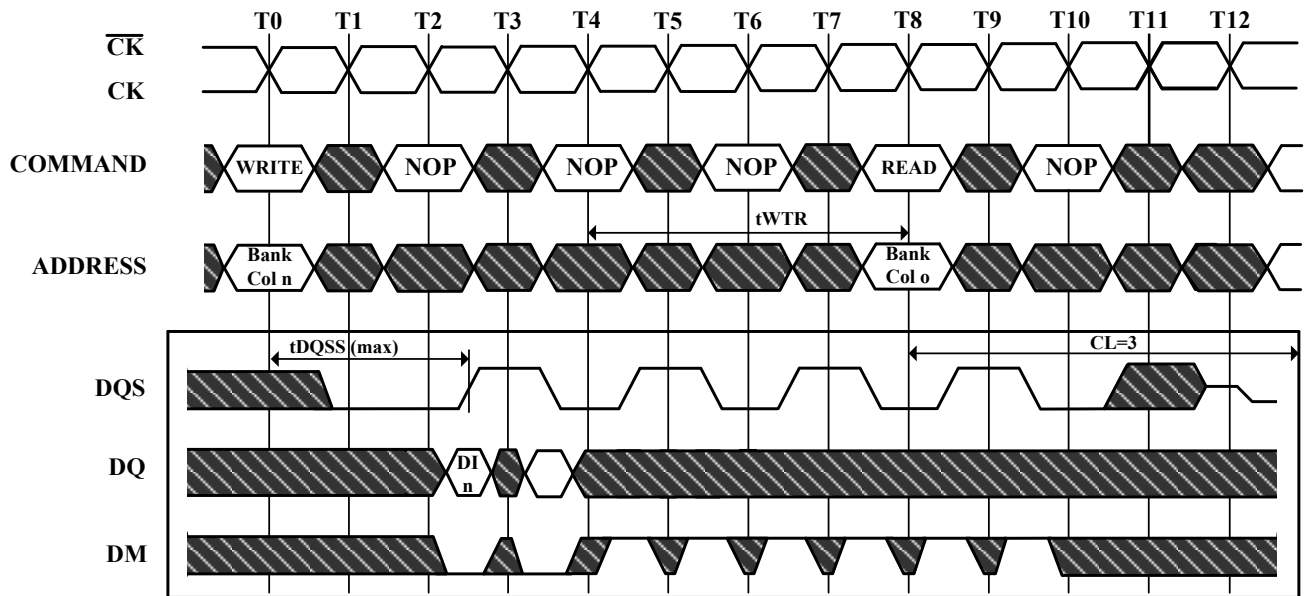
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= UDM & LDM

 Don't Care

**Figure 23. Write to Read Max tDQSS Interrupting**



DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

An interrupted burst of 8 is shown, 2 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair

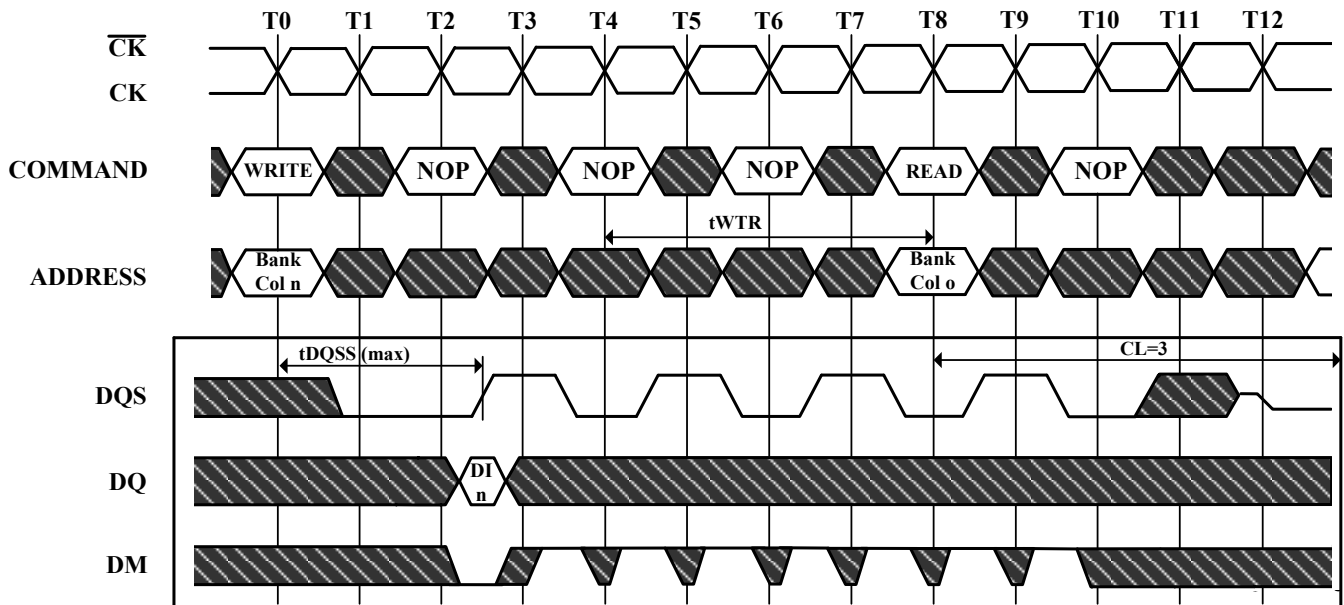
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= UDM & LDM

 Don't Care

**Figure 24. Write to Read Max tDQSS, ODD Number of Data, Interrupting**



DI n = Data In for column n

An interrupted burst of 8 is shown, 1 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair (not the last desired Data In element)

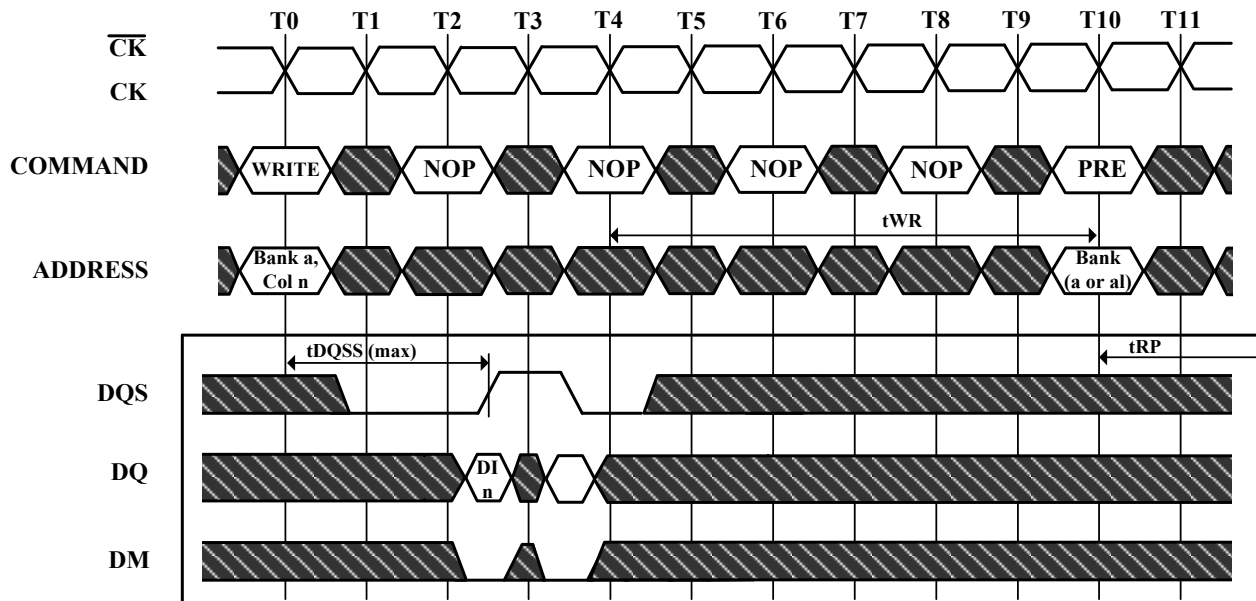
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= UDM & LDM

 Don't Care

**Figure 25. Write to Precharge Max tDQSS, NON- Interrupting**



**DI n = Data In for column n**

**1 subsequent elements of Data In are applied in the programmed order following DI n**

**A non-interrupted burst of 2 is shown**

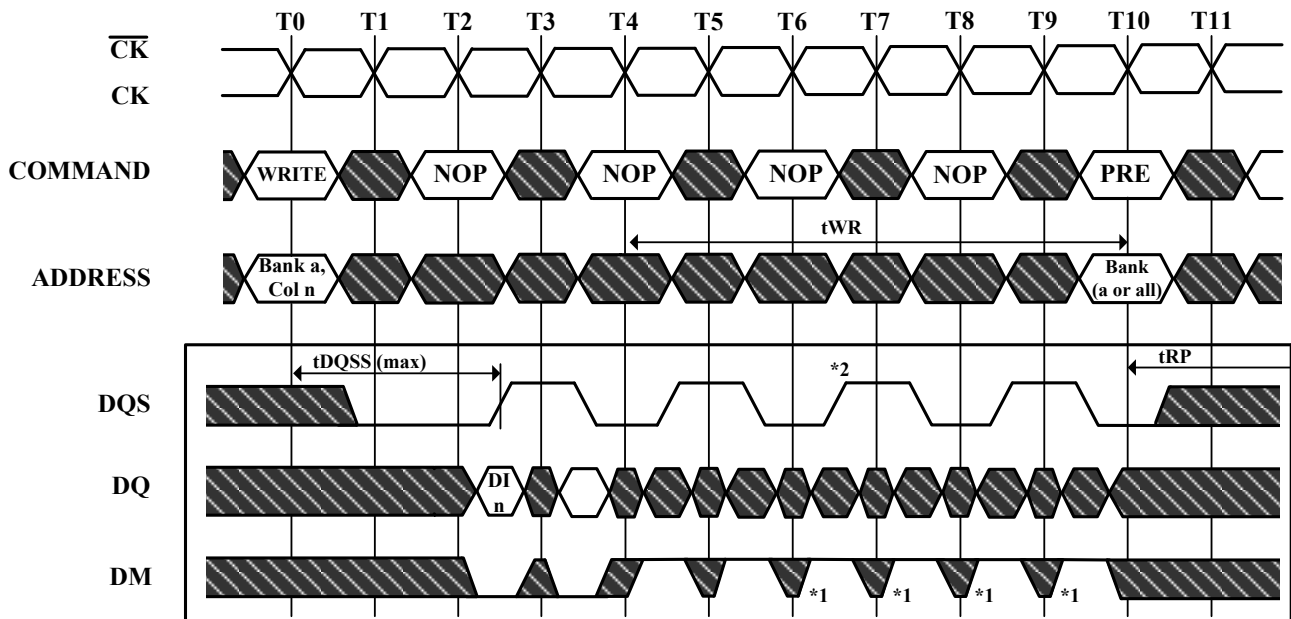
**tWR is referenced from the first positive CK edge after the last Data In Pair**

**A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)**

**DM= UDM & LDM**

 **Don't Care**

Figure 26. Write to Precharge Max tDQSS, Interrupting



DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 2 data elements are written

tWR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

\*1 = can be don't care for programmed burst length of 4

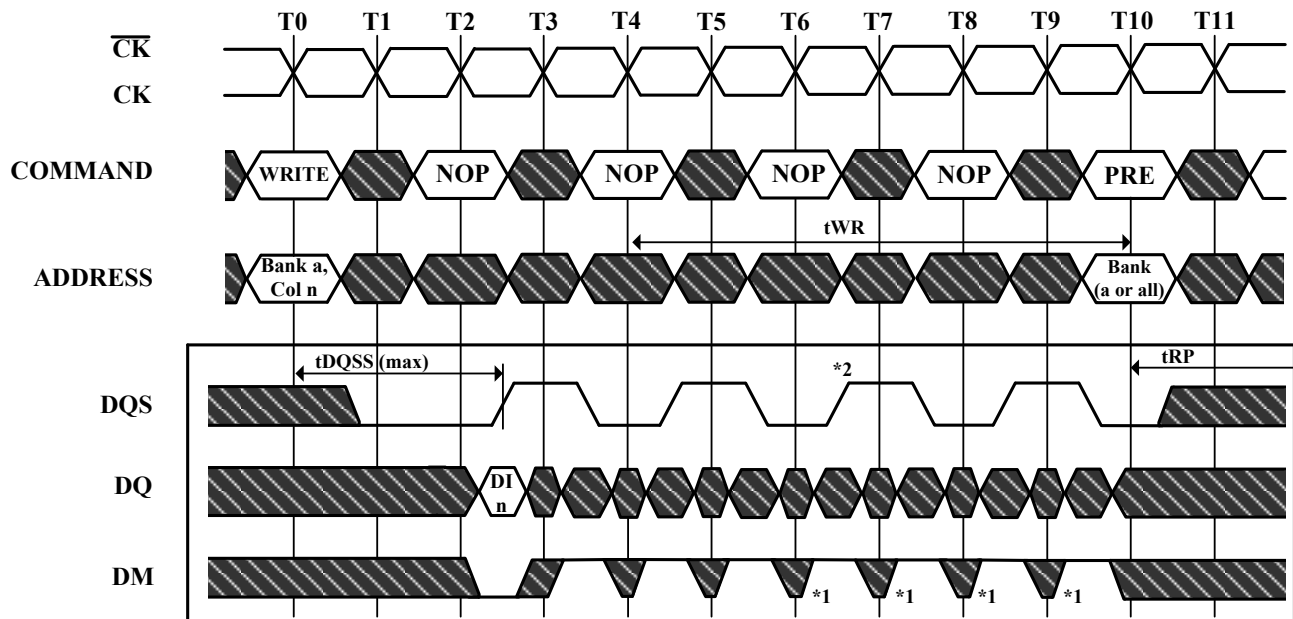
\*2 = for programmed burst length of 4, DQS becomes don't care at this point

DM= UDM & LDM

 Don't Care



**Figure 27. Write to Precharge Max tDQSS, ODD Number of Data Interrupting**



DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 1 data element is written

tWR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

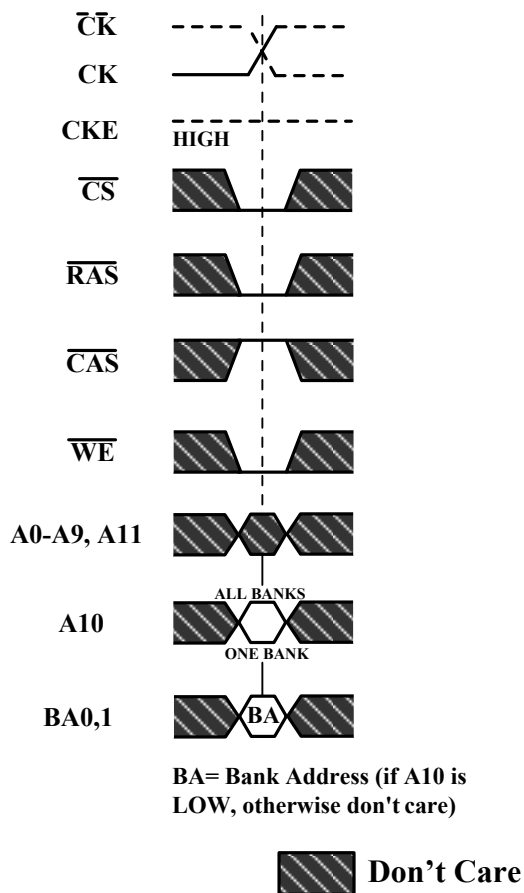
\*1 = can be don't care for programmed burst length of 4

\*2 = for programmed burst length of 4, DQS becomes don't care at this point

DM= UDM & LDM

 Don't Care

**Figure 28. Precharge Command**



The diagram illustrates the timing of a memory device's control signals. The horizontal axis represents time, with vertical dashed lines marking clock cycles T0 through Tn+6. The signals shown are:

- COMMAND:** A sequence of commands represented by hexagons. A solid white hexagon is labeled "VALID". Hexagons with diagonal hatching are labeled "Don't Care". The sequence is: VALID (at T0), Don't Care (T1), NOP (T2), Don't Care (T3), Don't Care (T4), Don't Care (Tn), Don't Care (Tn+1), Don't Care (Tn+2), NOP (Tn+3), Don't Care (Tn+4), VALID (Tn+5), Don't Care (Tn+6).
- CKE (Clock Enable):** A signal that transitions from high to low at T1 and back to high at Tn+3. The time from the falling edge to the rising edge is labeled  $t_{IS}$ .
- CK (Clock):** A periodic signal shown as a solid line with a dashed baseline. The period is marked by vertical dashed lines at each clock cycle.
- $\overline{CK}$  (Inverted Clock):** A signal that is the inverse of CK, shown as a dashed line with a solid baseline.

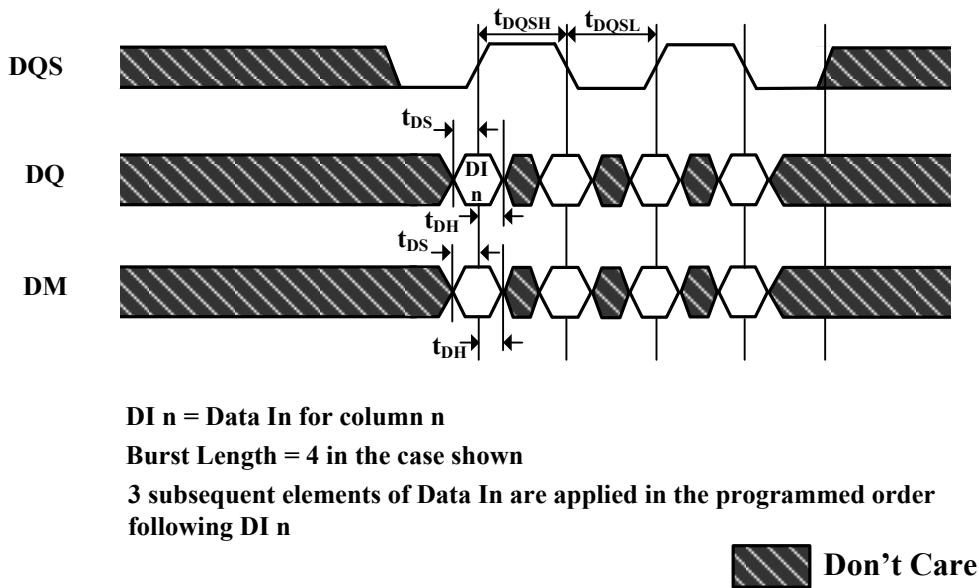
Annotations at the bottom of the diagram indicate the state of the device during specific time intervals:

- No column access in progress:** Indicated by an upward arrow at T0.
- Enter power-down mode:** Indicated by an upward arrow at T2.
- Exit power-down mode:** Indicated by an upward arrow at Tn+3.

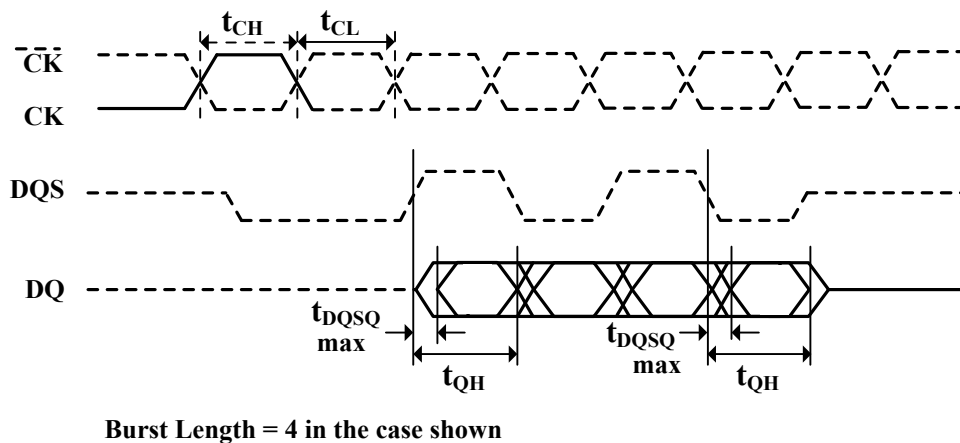
A legend at the bottom right shows a hatched box next to the text "Don't Care".

The diagram illustrates the timing for exiting the PLL from power-down. The clock signal (CK) is shown as a series of cycles labeled T0, T1, T2, T4, Tx, Tx+1, Ty, Ty+1, Ty+2, Ty+3, Ty+4, and Tz. The command signal (CMD) is a sequence of commands: NOP, NOP, a series of shaded blocks representing power-down, DLL RESET, NOP, NOP, and Valid. The clock enable signal (CKE) is a pulse that goes low at T2 and returns high at Ty+1. Key timing parameters are indicated:  $t_{RP}$  (pulse width of CKE), a minimum of 2 clock cycles before frequency change,  $t_{IS}$  (stable new clock before power down exit), and a 200-clock period after DLL RESET.

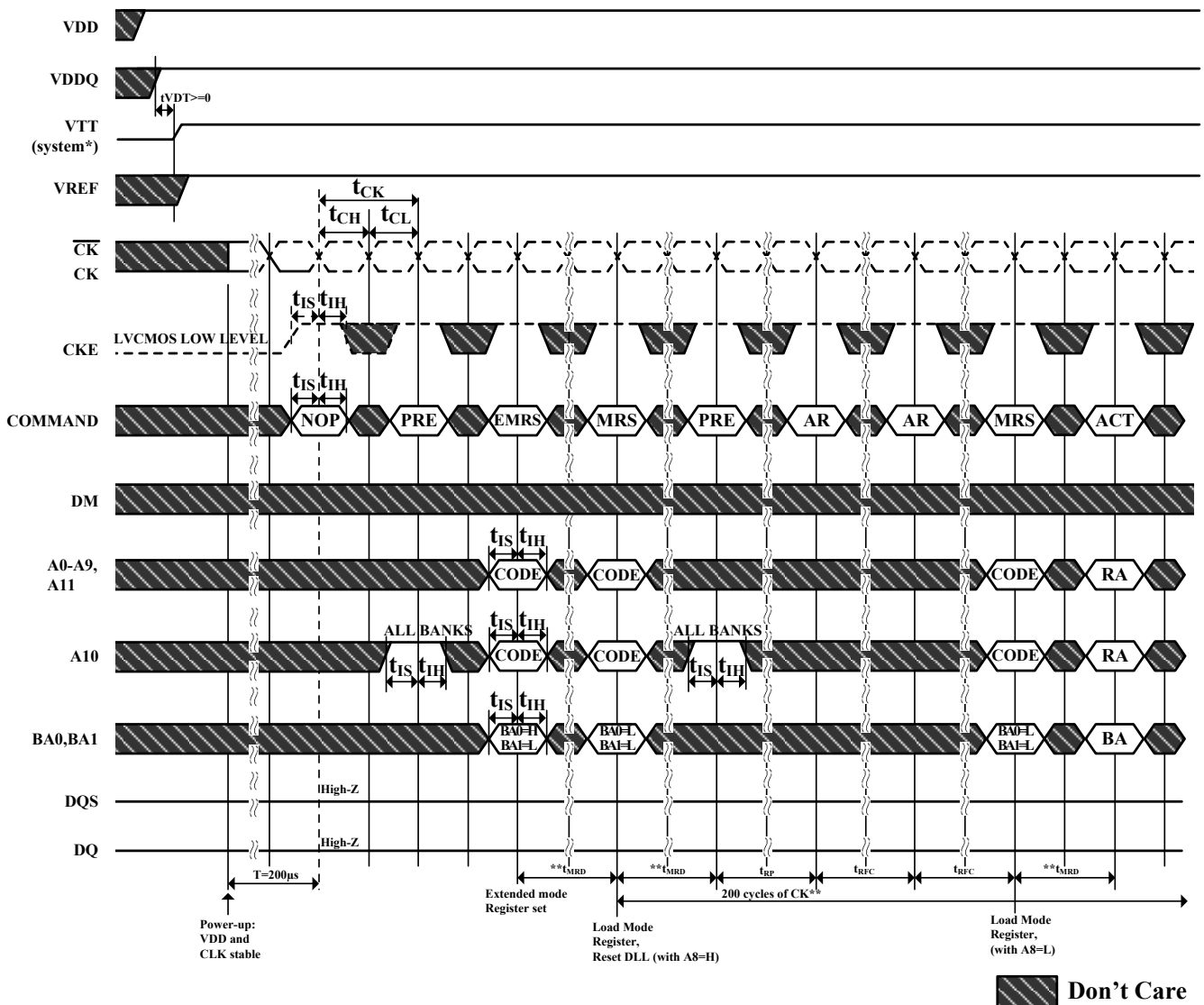
**Figure 31. Data input (Write) Timing**



**Figure 32. Data Output (Read) Timing**



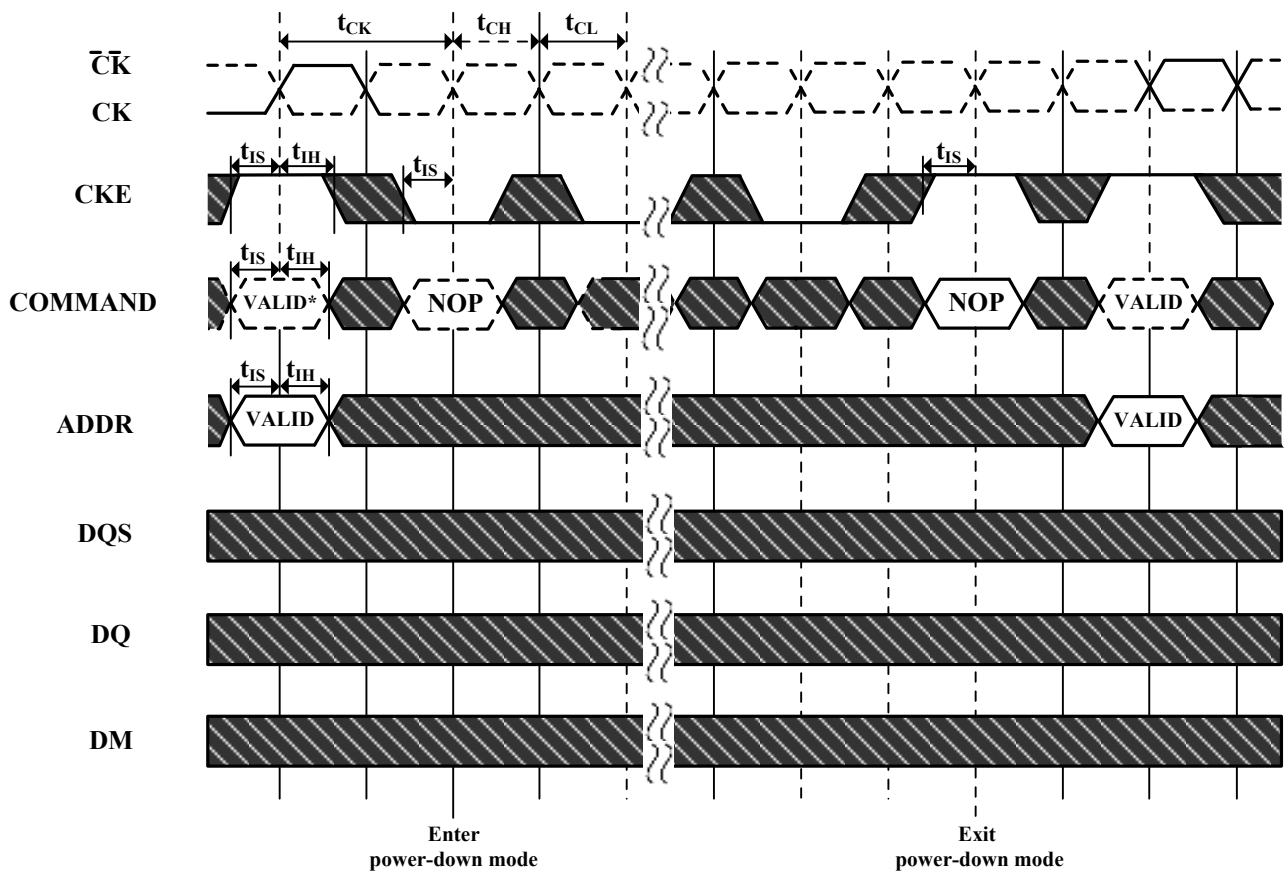
**Figure 33. Initialize and Mode Register Sets**



\*=VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up.

\*\* = tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied the two auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

Figure 34. Power Down Mode

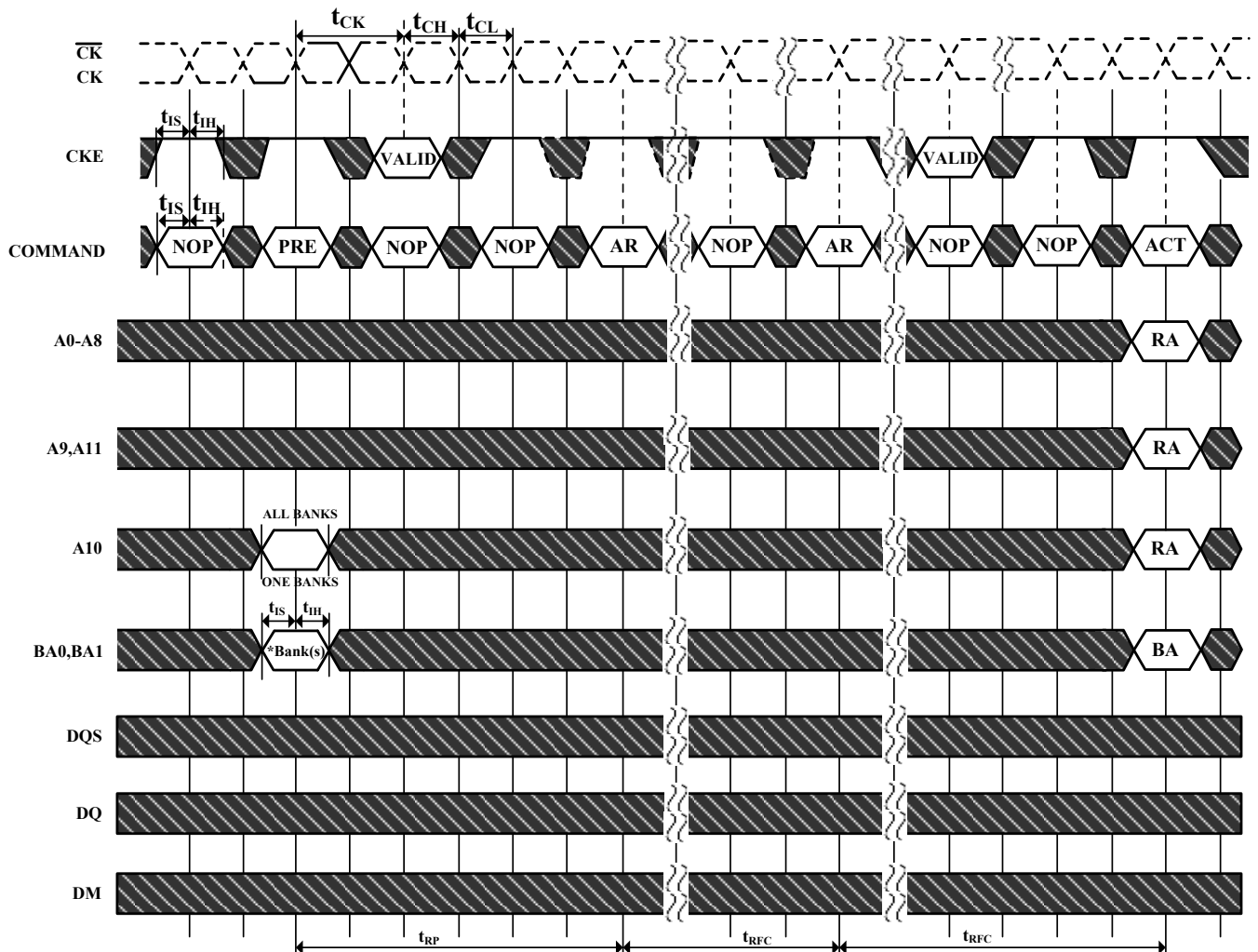


No column accesses are allowed to be in progress at the time Power-Down is entered

\*=If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is active Power Down.

 Don't Care

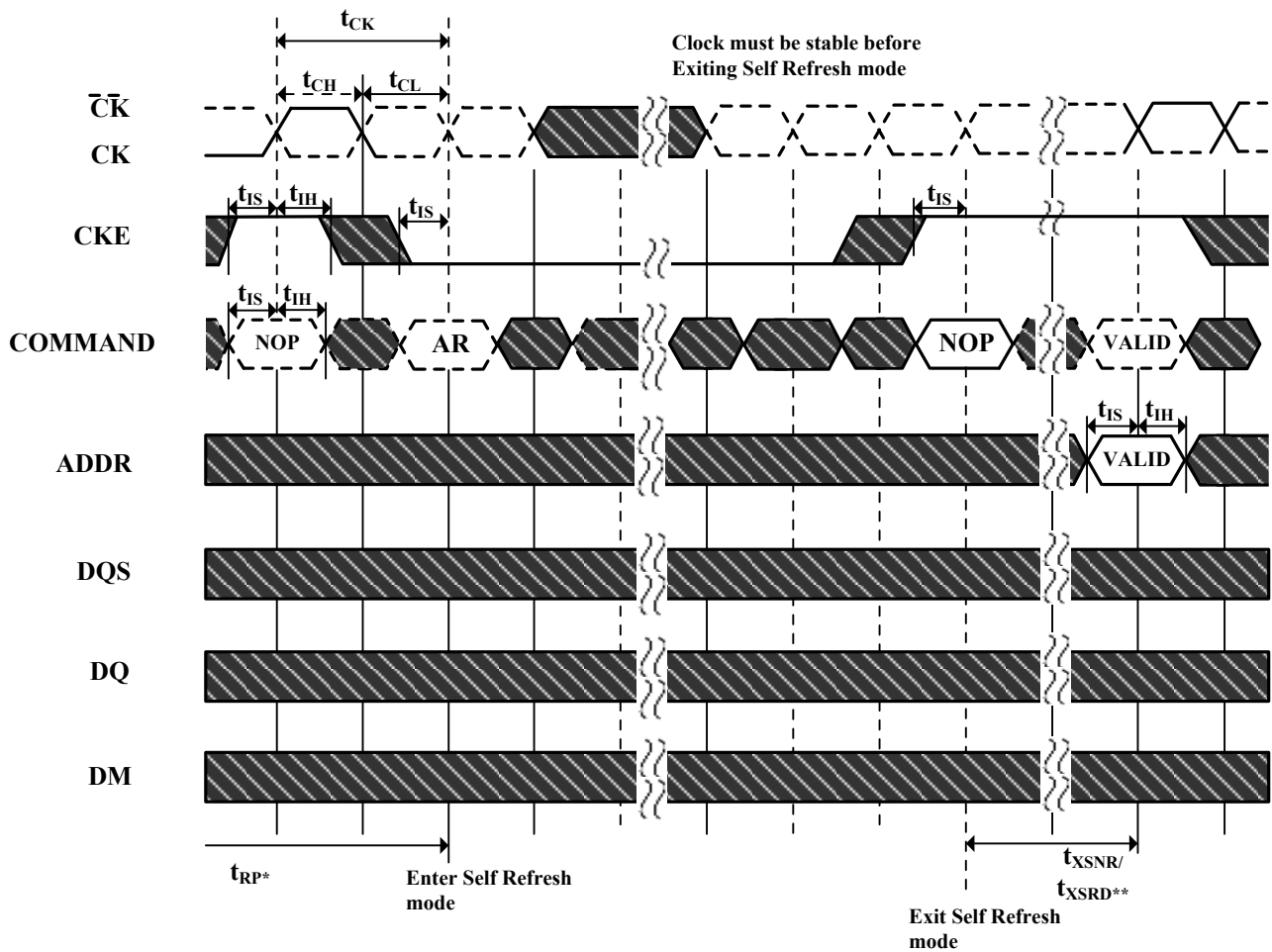
Figure 35. Auto Refresh Mode



\* = "Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)  
 PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH  
 NOP commands are shown for ease of illustration; other valid commands may be possible after  $t_{RFC}$   
 DM, DQ and DQS signals are all "Don't Care" /High-Z for operations shown

 Don't Care

Figure 36. Self Refresh Mode

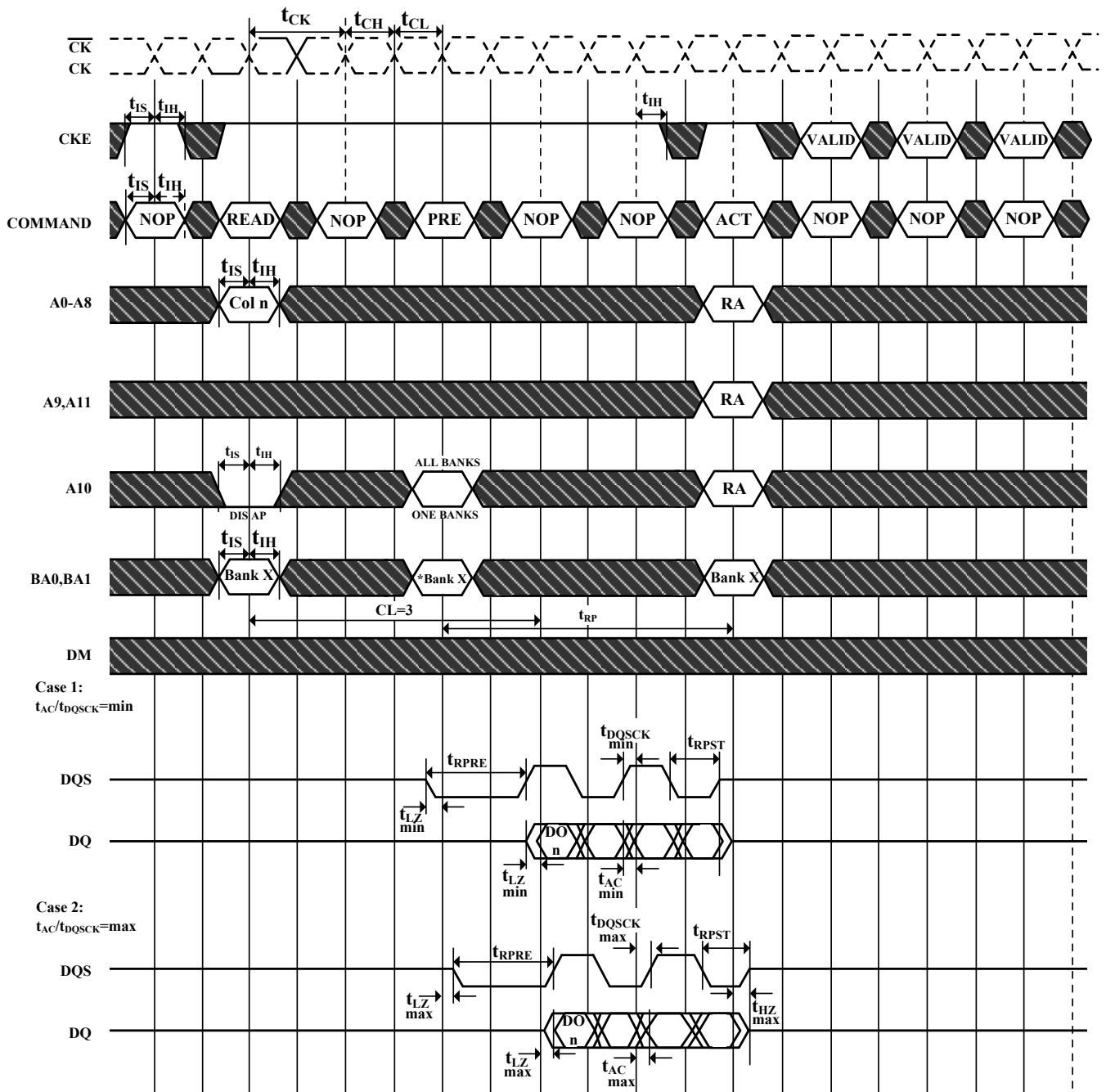


\* = Device must be in the "All banks idle" state prior to entering Self Refresh mode

\*\* =  $t_{XSNR}$  is required before any non-READ command can be applied, and  $t_{XSRD}$  (200 cycles of CK) is required before a READ command can be applied.



Figure 37. Read without Auto Precharge



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

\* = "Don't Care", if A10 is HIGH at this point

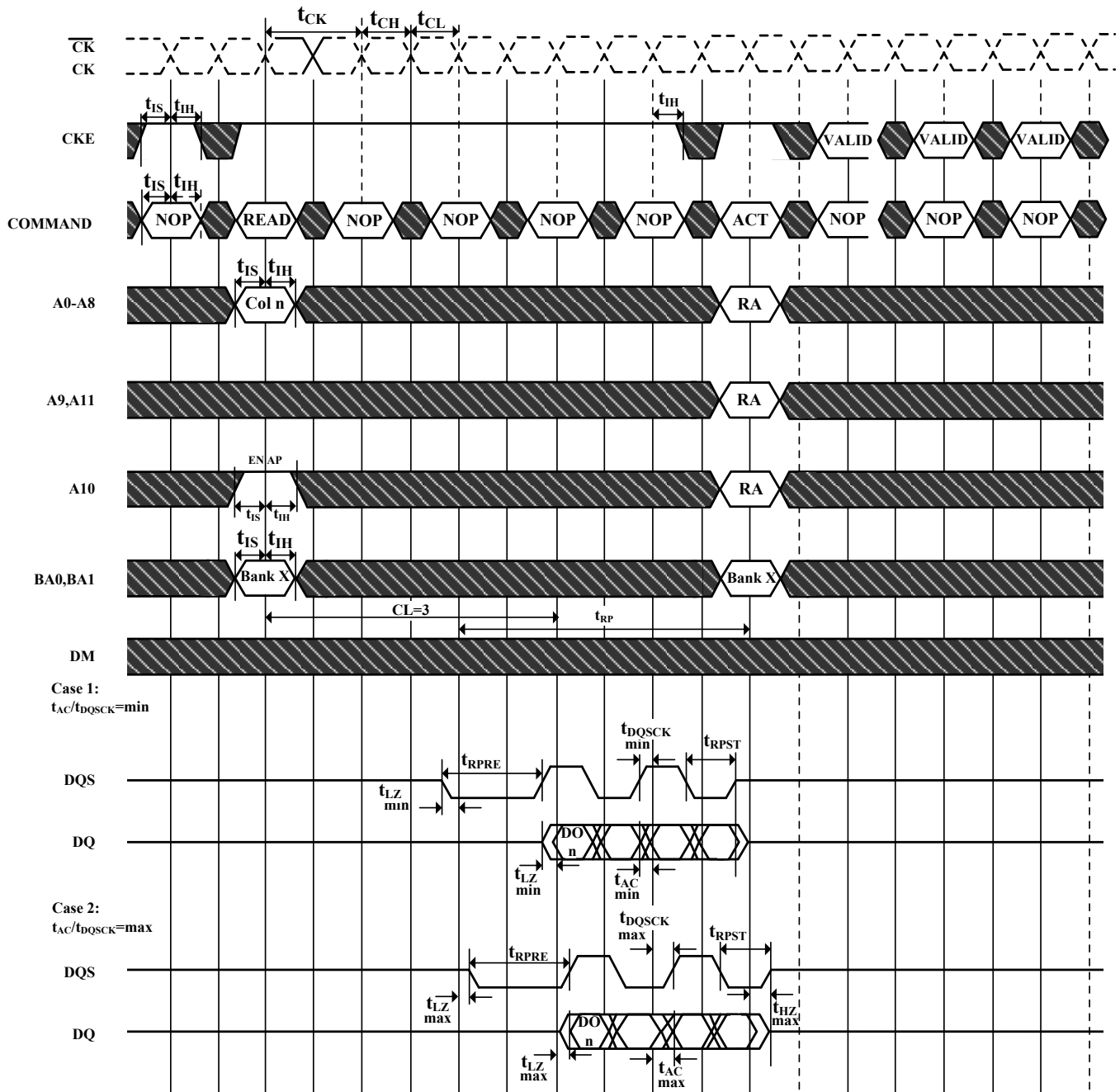
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other commands may be valid at these times

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

 Don't Care

Figure 38. Read with Auto Precharge



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

EN AP = Enable Autoprecharge

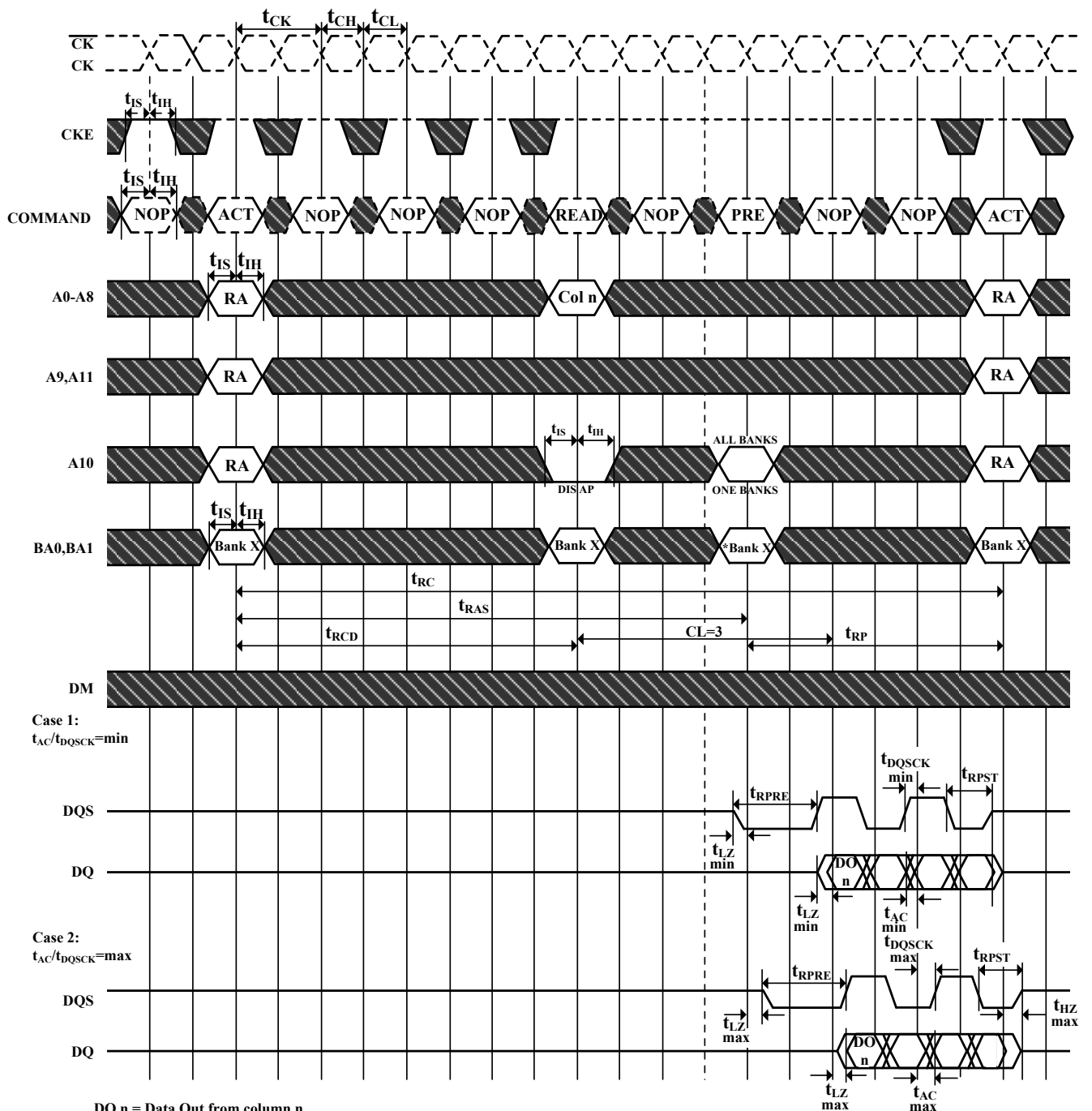
ACT = ACTIVE, RA = Row Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

The READ command may not be issued until  $t_{RAP}$  has been satisfied. If Fast Autoprecharge is supported,  $t_{RAP} = t_{RCD}$ , else the READ may not be issued prior to  $t_{RASmin} - (BL * t_{CK}/2)$

 Don't Care

Figure 39. Bank Read Access



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

\* = "Don't Care", if A10 is HIGH at this point

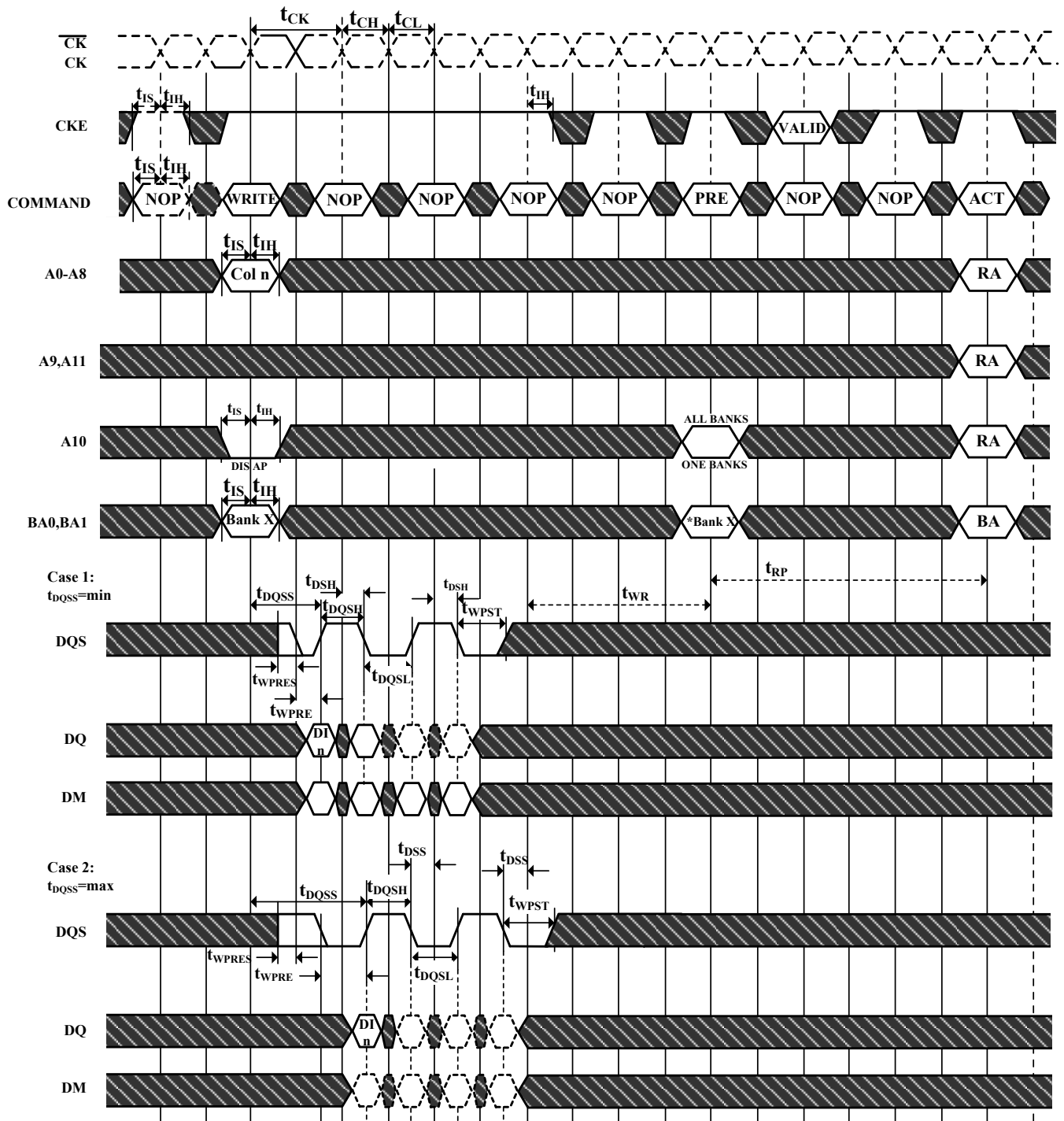
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Note that  $t_{RCD} > t_{RCD \min}$  so that the same timing applies if Autoprecharge is enabled (in which case  $t_{RAS}$  would be limiting)

 Don't Care

**Figure 40. Write without Auto Precharge**



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

\*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

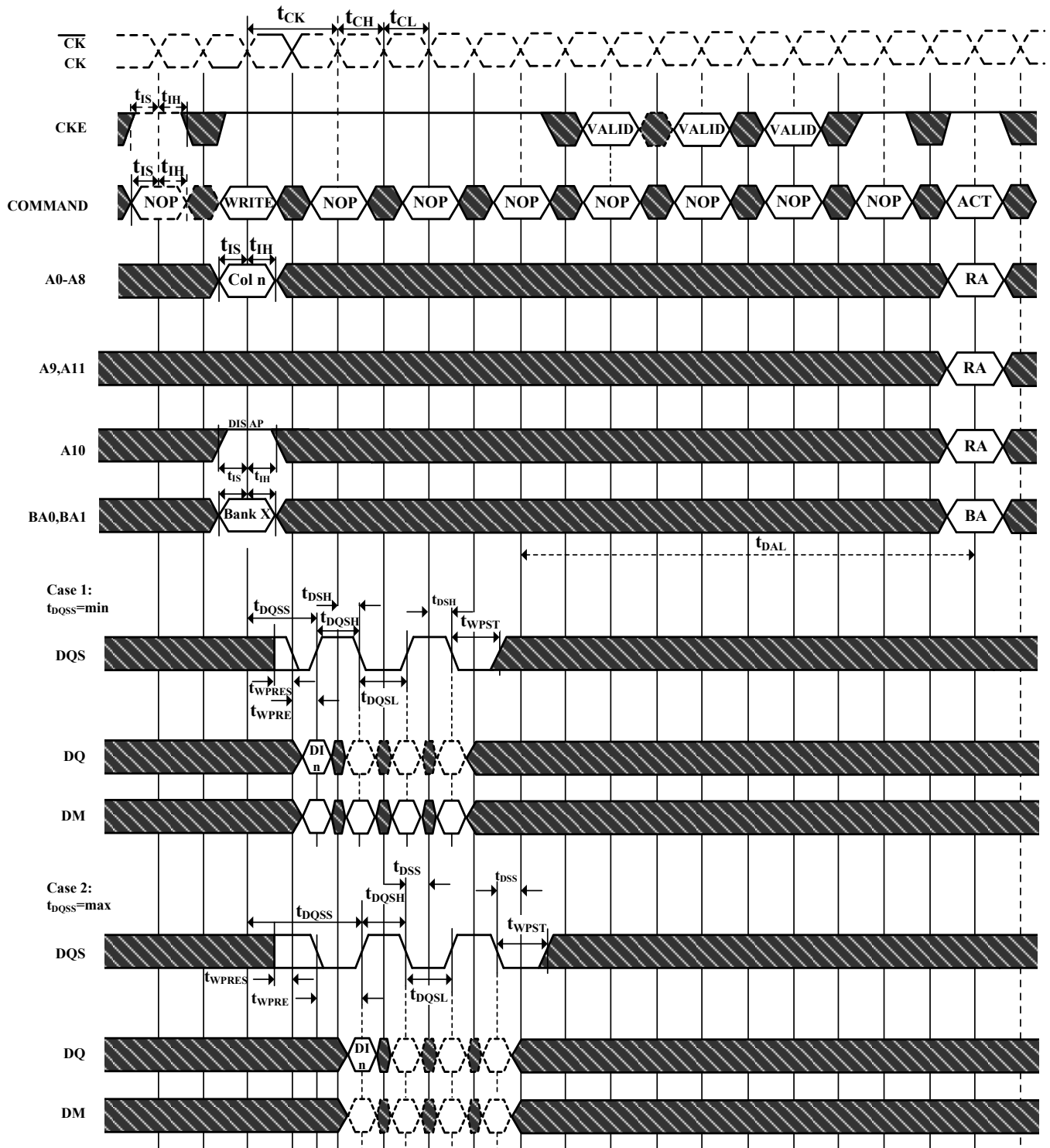
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the  $\pm 25\%$  window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

 Don't Care

**Figure 41. Write with Auto Precharge**



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

EN AP = Enable Autoprecharge

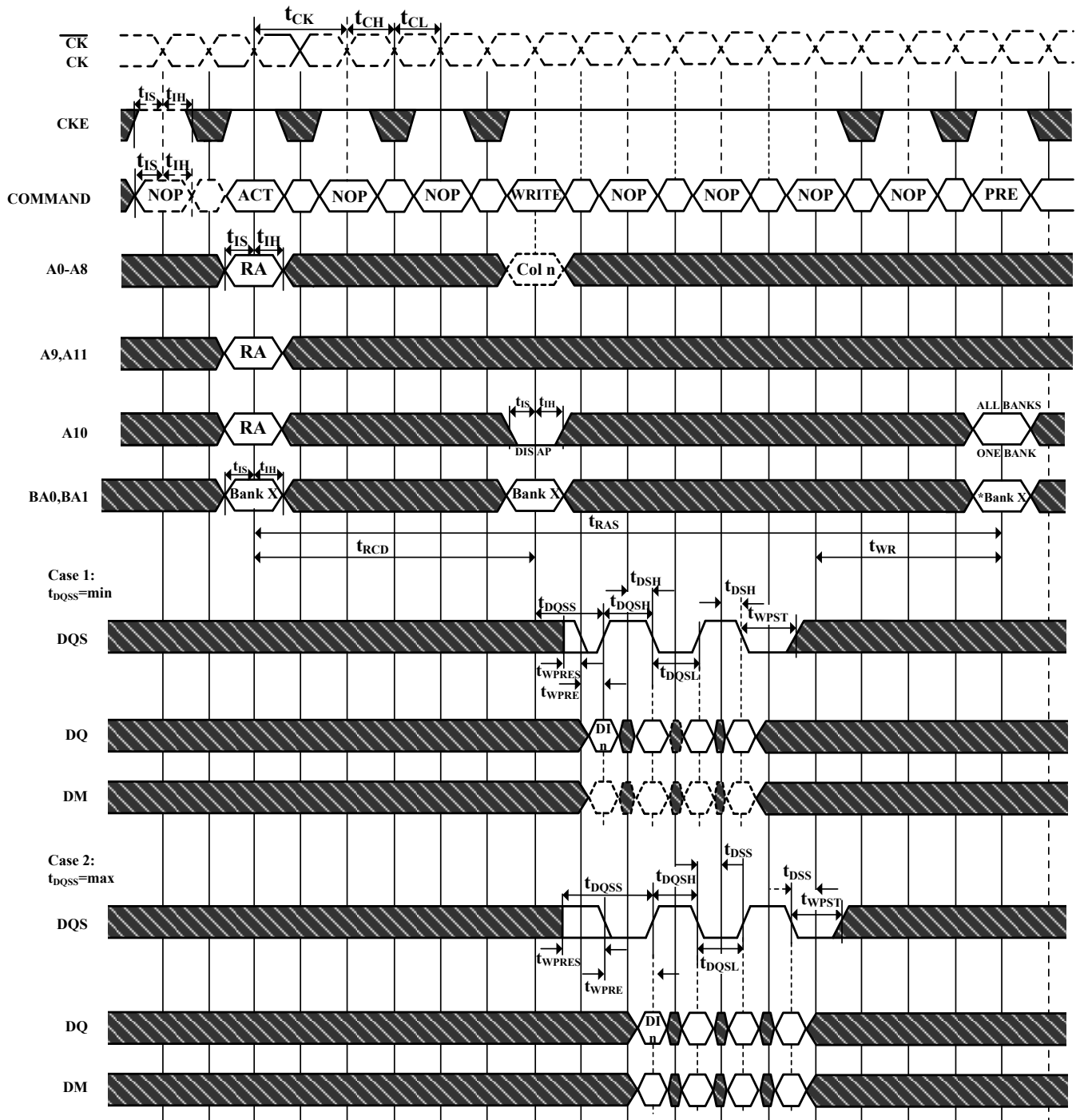
ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although  $t_{DQSS}$  is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the  $\pm 25\%$  window of the corresponding positive clock edge

 Don't Care

**Figure 42. Bank Write Access**



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

\*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

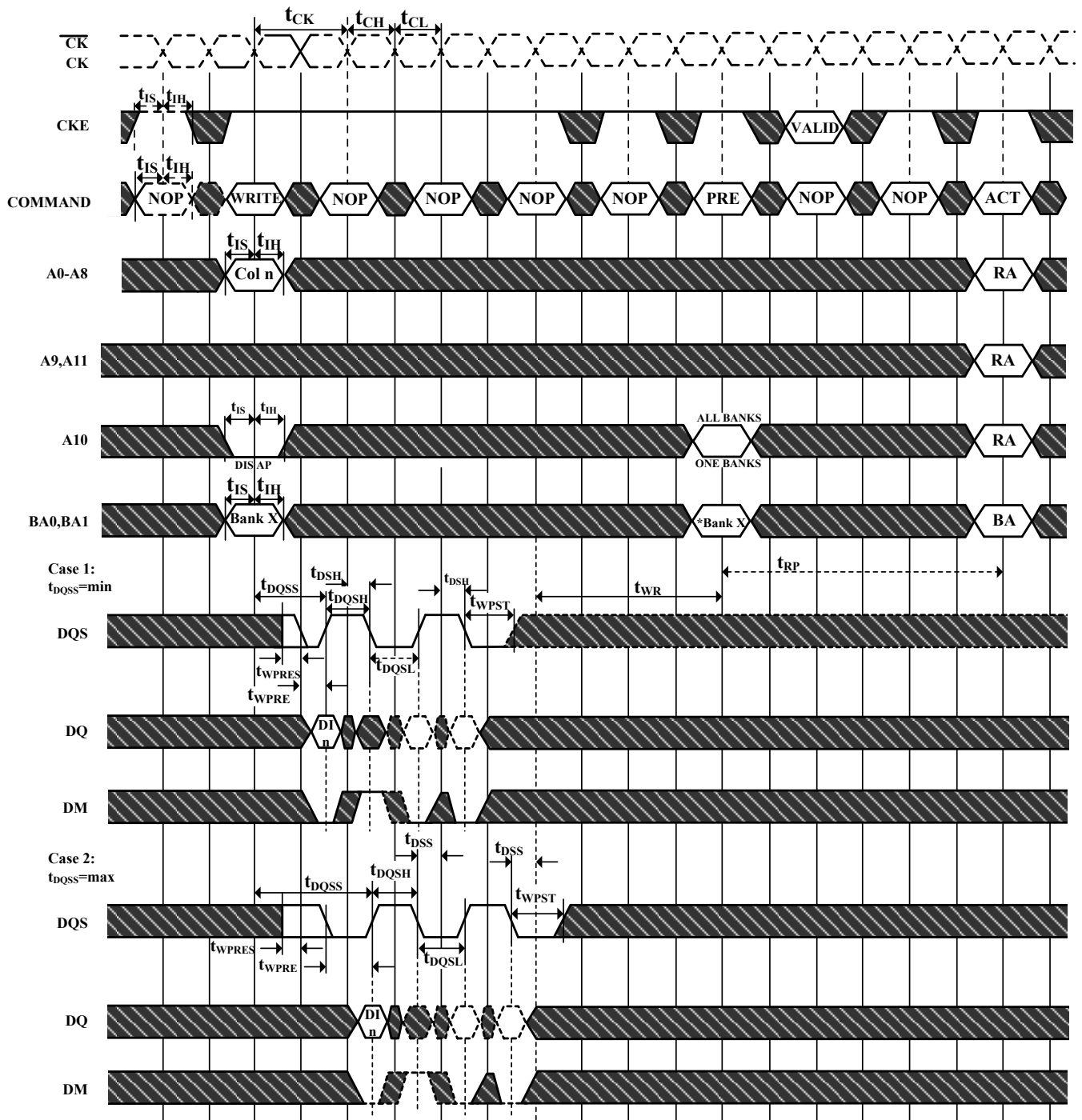
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the  $\pm 25\%$  window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

 Don't Care

**Figure 43. Write DM Operation**



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

\*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

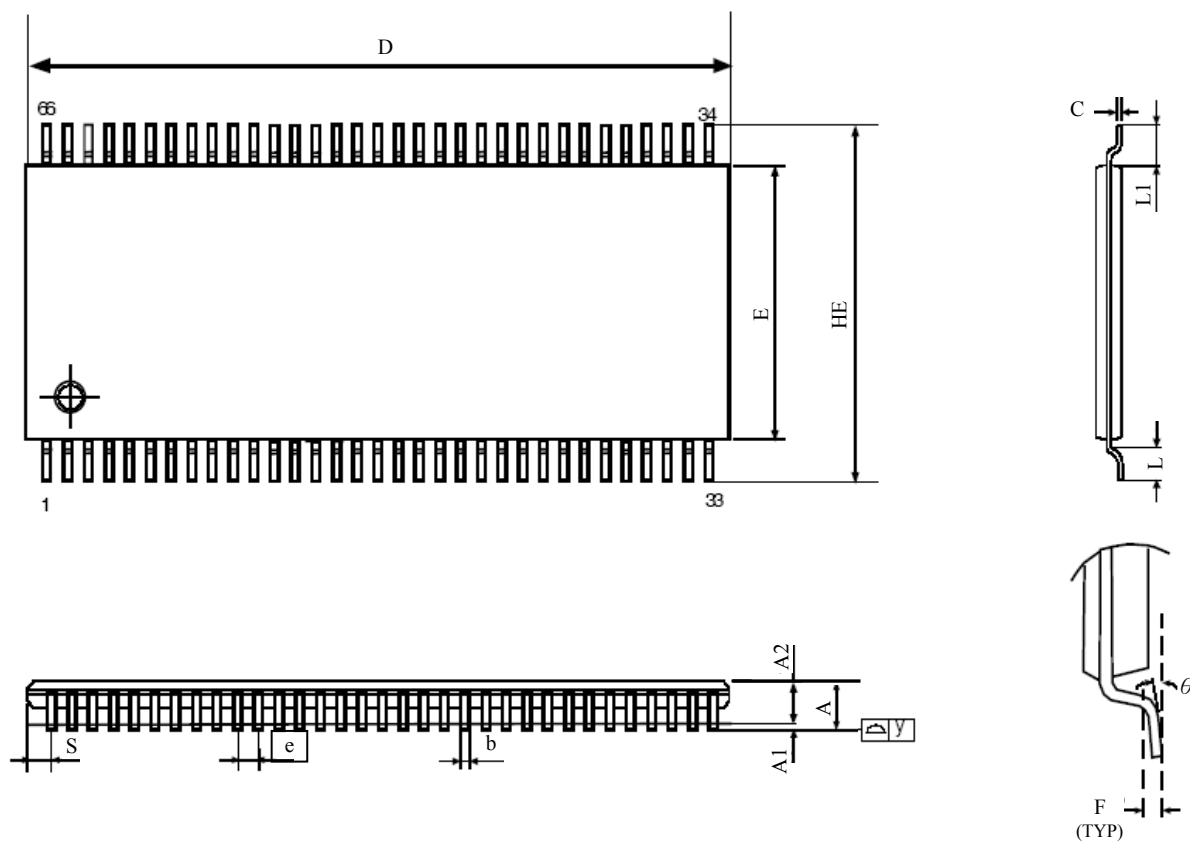
Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the  $\pm 25\%$  window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

 Don't Care

**Figure 44. 66 Pin TSOP II Package Outline Drawing Information:**

Units: mm



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.2	---	---	0.047
A1	0.05	---	0.2	0.002	---	0.008
A2	0.9	1.0	1.1	0.035	0.039	0.043
b	0.22	---	0.45	0.009	---	0.018
e	---	0.65	---	---	0.026	---
C	0.095	0.125	0.21	0.004	0.005	0.008
D	22.09	22.22	22.35	0.87	0.875	0.88
E	10.03	10.16	10.29	0.395	0.4	0.405
HE	11.56	11.76	11.96	0.455	0.463	0.471
L	0.40	0.5	0.6	0.016	0.02	0.024
L1	---	0.8	---	---	0.032	---
F	---	0.25	---	---	0.01	---
$\theta$	0°	---	8°	0°	---	8°
S	---	0.71	---	---	0.028	---
$\Delta y$	---	---	0.10	---	---	0.004



## PART NUMBERING SYSTEM

AS4C	8M16D1	5	T	C/I	N
DRAM	8M16 = 8Mx16 D1=DDR1	5=200MHz	T = TSOPII	C=Commercial (0° C~70° C) I=Industrial (-40° C~85° C)	Indicates Pb and Halogen Free



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