DABiC-5 32-Bit Serial Input Latched Sink Drivers

Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: November 1, 2010

Deadline for receipt of LAST TIME BUY orders: April 30, 2011

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

DABiC-5 32-Bit Serial Input Latched Sink Drivers

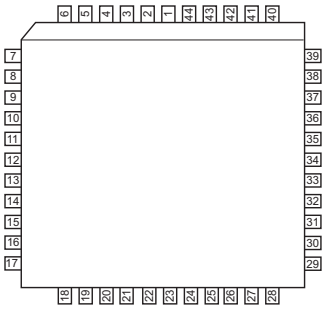
Features and Benefits

- 3.3 to 5 V logic supply range
- To 10 MHz data input rate
- 30 V minimum output breakdown
- Darlington current-sink outputs
- Low-power CMOS logic and latches
- Schmitt trigger inputs for improved noise immunity

Applications:

- Thermal printheads
- Multiplexed LED displays
- Incandescent lamps

Package: 44-pin PLCC (suffix EP)



Not to scale

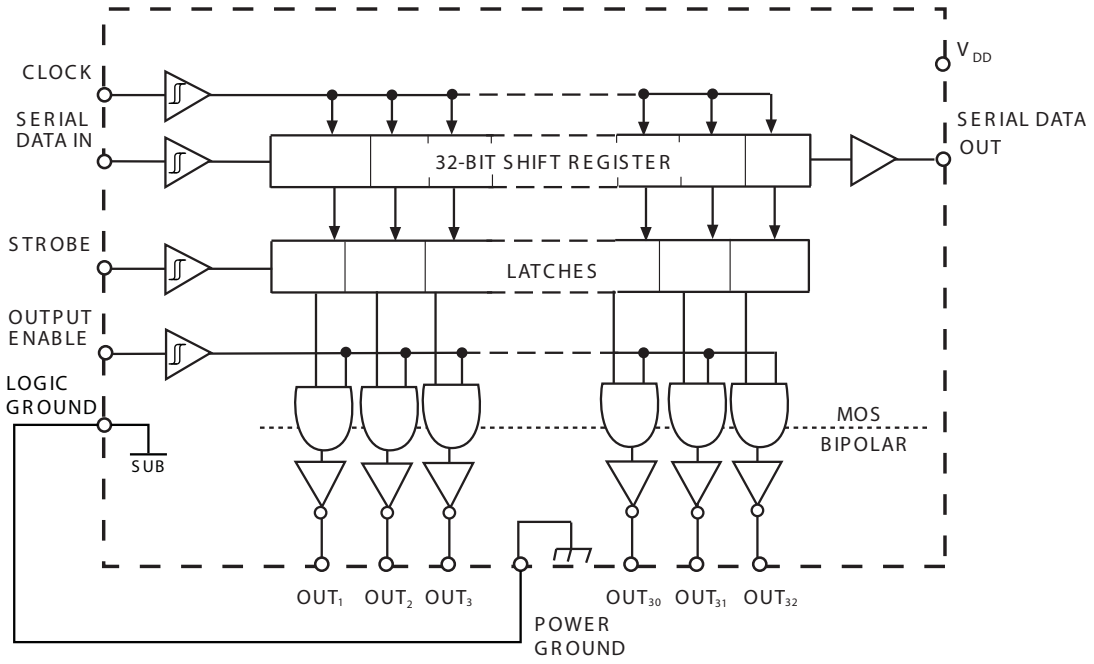
Description

Designed to reduce logic supply current, chip size, and system cost, the A6833 integrated circuit offers high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives the A6833 smart power IC an interface flexibility beyond the reach of standard buffers and power driver circuits.

This 32-bit drivers have bipolar open-collector NPN Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

The A6833 is supplied in a 44-lead plastic chip carrier (quad pack), intended for surface mounting on solder lands with 0.050 in. (1.27 mm) centers. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

Functional Block Diagram



Selection Guide

Part Number	Packing	Package
A6833SEPTR-T	450 pieces per reel	44-pin PLCC

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Logic Supply Voltage	V_{DD}		7	V
Input Voltage Range	V_{IN}	Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.	–0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		30	V
Continuous Output Current	I_{OUT}	Each output	125	mA
Output Current Sink	$I_{OUT(sink)}$		10	mA
Package Power Dissipation	P_D	Derate linearly to 0 W at 150ºC	2.5	W
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

ELECTRICAL CHARACTERISTICS[1] Unless otherwise noted: T_A = 25°C, logic supply operating voltage V_{dd} = 3.0 V to 5.5 V

Characteristic	Symbol	Test Conditions	V_{dd} = 3.3 V			V_{dd} = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V	–	–	10	–	–	10	µA
Collector–Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	–	–	0.7	–	–	0.7	V
		I_{OUT} = 100 mA	–	–	1.0	–	–	1.0	V
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	–	< 0.01	1.0	–	< 0.01	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	–	<–0.01	–1.0	–	<–0.01	–1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = –200 µA	2.8	3.05	–	4.5	4.75	–	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency[2]	f_c		10	–	–	10	–	–	MHz
Logic Supply Current	$I_{DD(1)}$	One output on, I_{OUT} = 100 mA	–	–	2.0	–	–	2.0	mA
	$I_{DD(0)}$	All outputs off	–	–	100	–	–	100	µA
Output Enable-to-Output Delay	$t_{dis(BQ)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	$t_{en(BQ)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	$t_{p(STH-QH)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Fall Time	t_f	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	500	–	–	500	ns
Output Rise Time	t_r	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	500	–	–	500	ns
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 µA	–	50	–	–	50	–	ns

[1]Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.
[2]Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

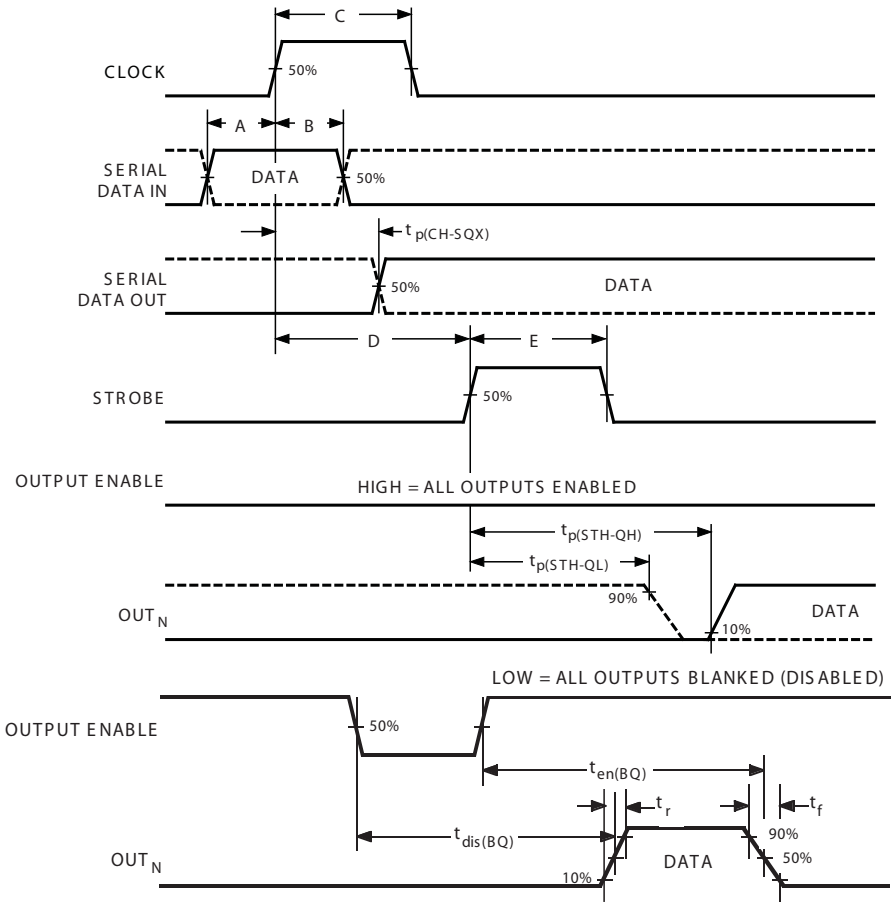
Truth Table

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	L	H H H ... H H

L = Low Logic Level
H = High Logic Level
X = Irrelevant

P = Present State
R = Previous State

Timing Requirements and Specifications
(Logic Levels are V_{DD} and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_{h(D)}$	25
C	Clock Pulse Width	$t_{w(CH)}$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_{w(STH)}$	50

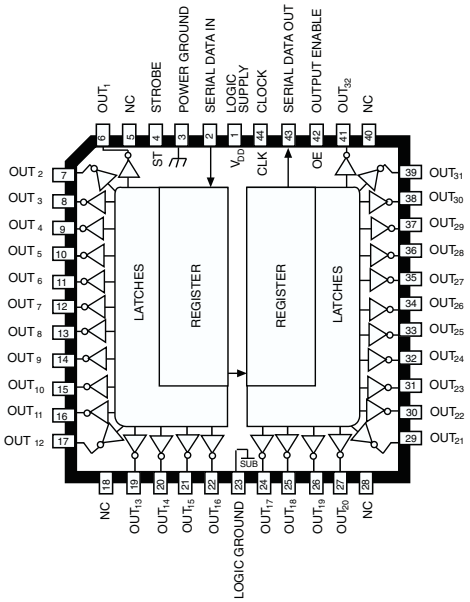
NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

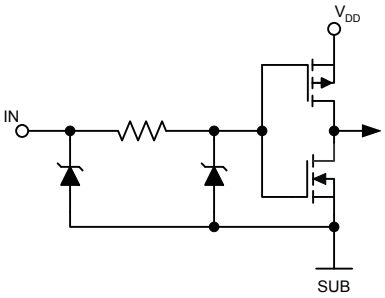
Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, the output sink drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input high, the outputs are controlled by the state of their respective latches.

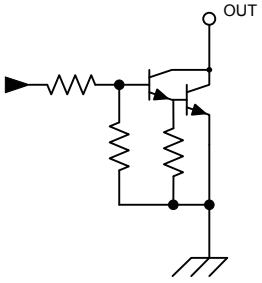
Pin-out Diagram



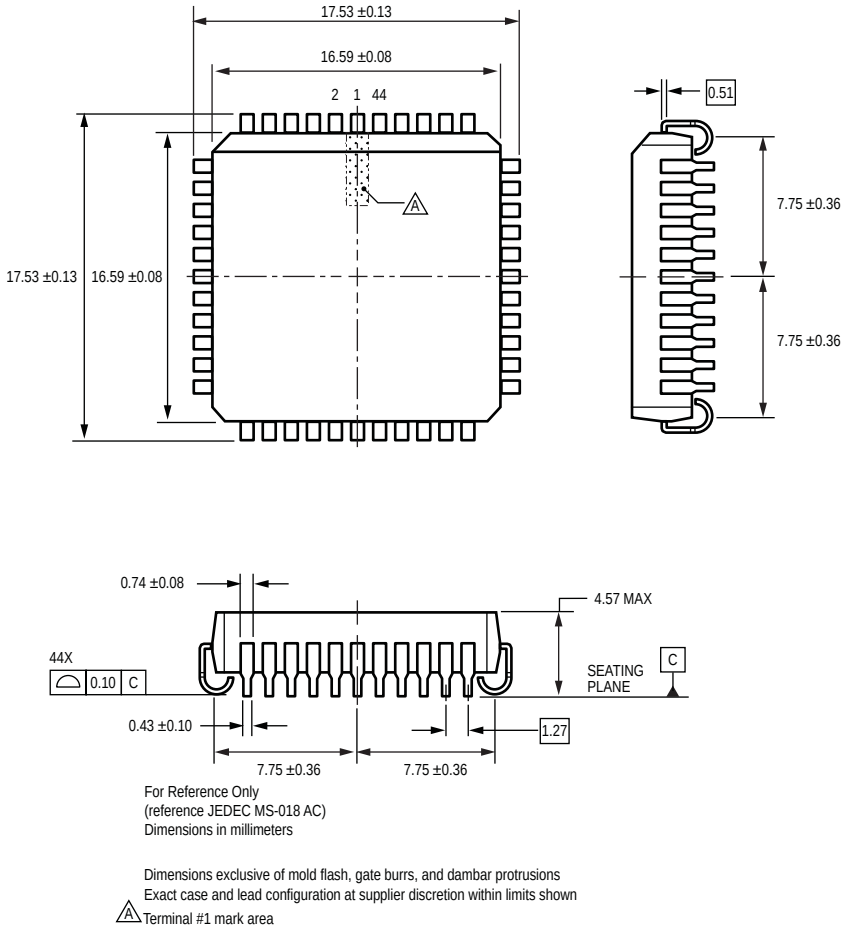
Typical Input Circuit



Typical Output Driver



Package EP, 44-pin PLCC



For Reference Only
(reference JEDEC MS-018 AC)
Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

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