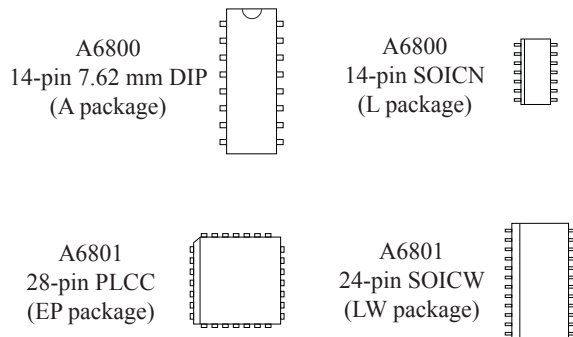


## DABiC-5 Latched Sink Drivers

### Features and Benefits

- 3.3 to 5 V logic supply range
- Up to 10 MHz data input rate
- High-voltage, high-current outputs
- Darlington current-sink outputs, with improved low-saturation voltages
- CMOS, TTL compatible inputs
- Output transient protection
- Internal pull-down resistors
- Low-power CMOS latches

### Packages



Approximate scale 1:1

### Description

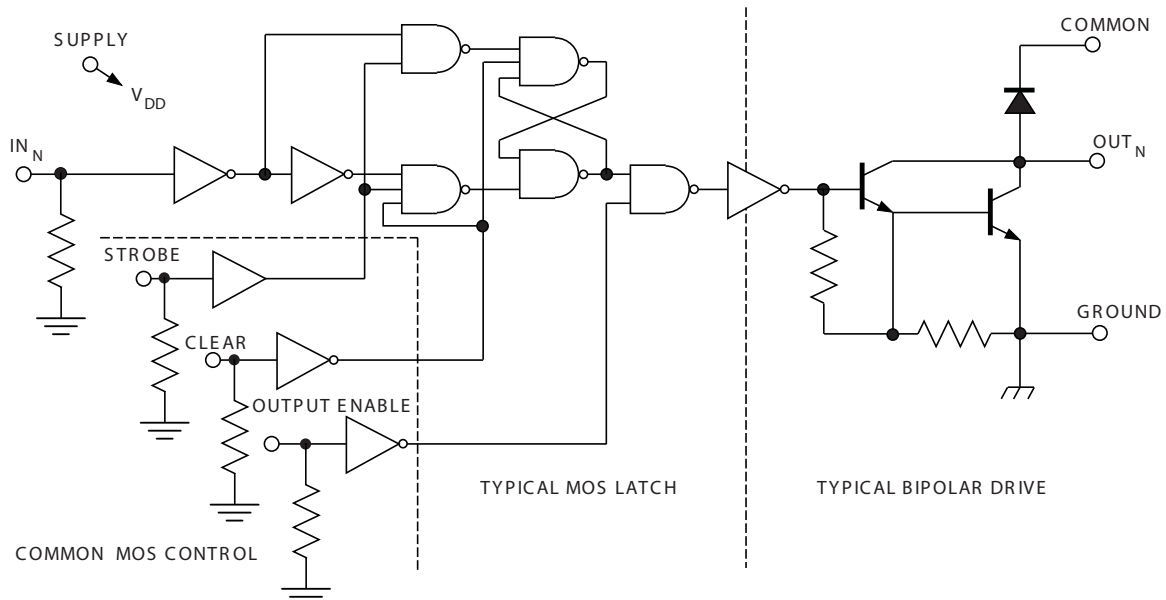
The A6800 and A6801 latched-input BiMOS ICs merge high-current, high-voltage outputs with CMOS logic. The CMOS input section consists of 4 or 8 data (D type) latches with associated common CLEAR, STROBE, and OUTPUT ENABLE circuitry. The power outputs are bipolar NPN Darlington. This merged technology provides versatile, flexible interface. These BiMOS power interface ICs greatly benefit the simplification of computer or microprocessor I/O. The A6800 ICs each contain four latched drivers. A6801 ICs contain eight latched drivers.

The CMOS inputs are compatible with standard CMOS circuits. TTL circuits may mandate the addition of input pull-up resistors. The bipolar Darlington outputs are suitable for directly driving many peripheral/power loads: relays, lamps, solenoids, small DC motors, and so forth.

All devices have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 600 mA and can withstand at least 50 V in the off state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

Continued on the next page...

### Functional Block Diagram



## Description (continued)

The A6800SA is furnished in a 14-pin DIP with 7.62 mm (0.300 in.) row centers, the A6800SL and A6801SLW in surface-mountable SOICs; and the A6801SEP in a 28-lead PLCC. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

Applications include:

- Relays
- Lamps
- Solenoids
- Small DC motors

## Selection Guide

Part Number	Package	Packing
A6800SA-T*	14-pin DIP	25 per tube
A6800SLTR-T	14-pin SOIC	2500 per reel
A6801SEPTR-T	28-pin PLCC	800 per reel
A6801SLWTR-T	24-pin SOIC	1000 per reel

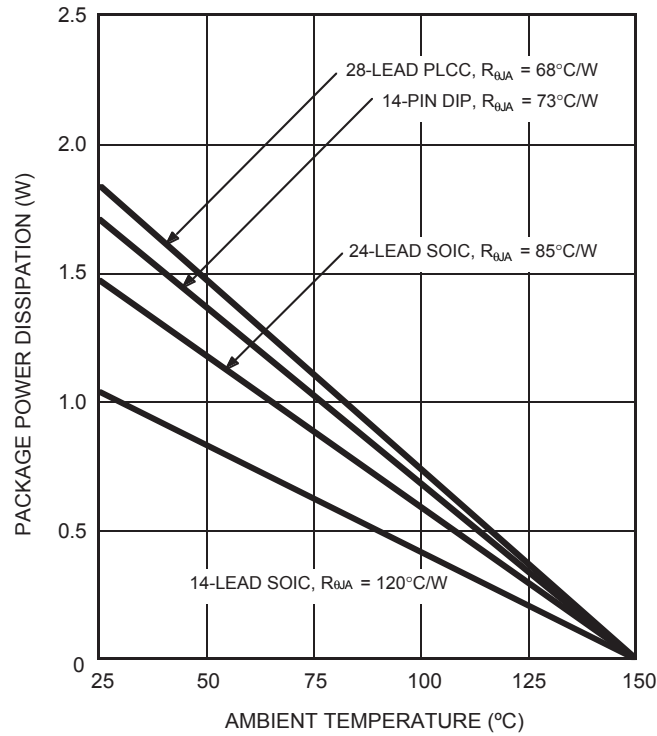
\*Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

## Absolute Maximum Ratings\*

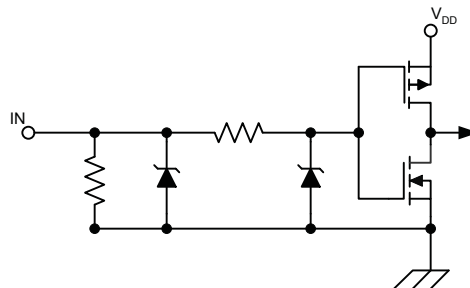
Characteristic	Symbol	Notes	Rating	Units
Output Voltage	$V_{CE}$		50	V
Supply Voltage	$V_{DD}$		7	V
Input Voltage Range	$V_{IN}$		-0.3 to $V_{DD} + 0.3$	V
Continuous Collector Current	$I_C$		600	mA
Operating Ambient Temperature	$T_A$	Range S	-20 to 85	°C
Maximum Junction Temperature	$T_J(\max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

\*Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

Allowable Power Dissipation



Typical Input Circuit



**ELECTRICAL CHARACTERISTICS<sup>1</sup>** Unless otherwise noted:  $T_A = 25^\circ\text{C}$ , logic supply operating voltage  $V_{DD} = 3.0$  to  $5.5\text{V}$

Characteristic	Symbol	Test Conditions	$V_{DD} = 3.3\text{V}$			$V_{DD} = 5\text{V}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	$I_{CEX}$	$V_{OUT} = 50\text{V}$	–	–	10	–	–	10	$\mu\text{A}$
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 350\text{mA}$ , $L = 3\text{mH}$	35	–	–	35	–	–	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{mA}$	–	0.8	1.0	–	0.8	1.0	V
		$I_{OUT} = 200\text{mA}$	–	0.9	1.1	–	0.9	1.1	V
		$I_{OUT} = 350\text{mA}$ (See note 2)	–	1.0	1.3	–	1.0	1.3	V
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Resistance	$R_{IN}$		50	–	–	50	–	–	$\text{k}\Omega$
Logic Supply Current	$I_{DD(1)}$	One output on, $I_{OUT} = 100\text{mA}$	–	–	1.0	–	–	1.0	$\text{mA}$
	$I_{DD(0)}$	All outputs off	–	130	150	–	130	150	$\mu\text{A}$
Clamp Diode Leakage Current	$I_r$	$V_r = 50\text{V}$	–	–	50	–	–	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_f$	$I_f = 350\text{mA}$	–	–	2.0	–	–	2.0	V
Output Fall Time	$t_f$	$V_{CC} = 50\text{V}$ , $R_1 = 500\Omega$ , $C_1 \leq 30\text{pF}$	–	80	–	–	80	–	ns
Output Rise Time	$t_r$	$V_{CC} = 50\text{V}$ , $R_1 = 500\Omega$ , $C_1 \leq 30\text{pF}$	–	100	–	–	100	–	ns

<sup>1</sup> Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic 1.

<sup>2</sup> Because of limitations on package power dissipation, the simultaneous operation of multiple drivers can only be accomplished by reduction in duty cycle.

Truth Table

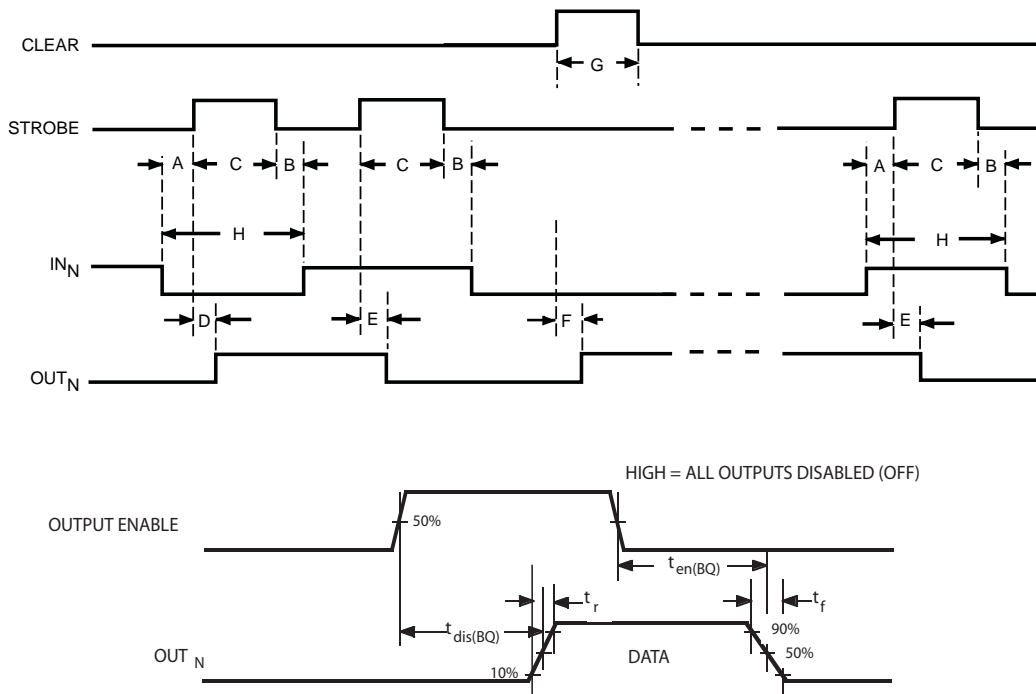
$IN_N$	STROBE	CLEAR	OUTPUT ENABLE	$OUT_N$	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant

t-1 = previous output state

t = present output state

**Timing Requirements and Specifications**  
(Logic Levels are  $V_{DD}$  and Ground)

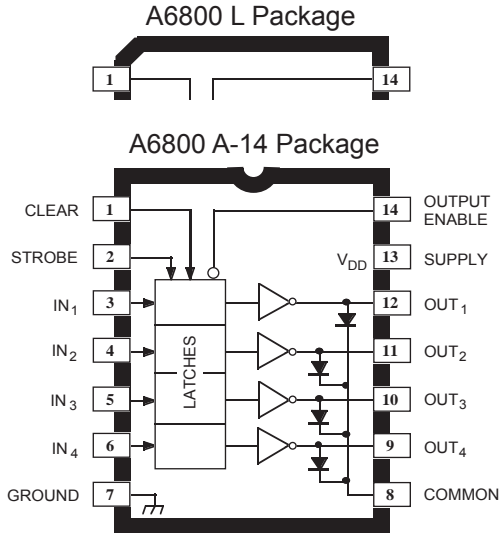


Key	Description	Time (ns)
A	Minimum data active time before Strobe enabled (Data Set-Up Time)	25
B	Minimum data active time after Strobe disabled (Data Hold Time)	25
C	Minimum Strobe pulse width	50
D	Maximum time between Strobe activation and transition from output on to output off*	500
E	Maximum time between Strobe activation and transition from output off to output on*	500
F	Maximum time between Clear activation and transition from output on to output off*	500
G	Minimum Clear pulse width	50
H	Minimum data pulse width	100
$t_{dis(BQ)}$	Output Enable to output off delay*	500
$t_{en(BQ)}$	Output Enable to output on delay*	500

\*Conditions for output transition testing are:  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $R_1 = 500\ \Omega$ ,  $C_1 \leq 30\text{ pF}$ .

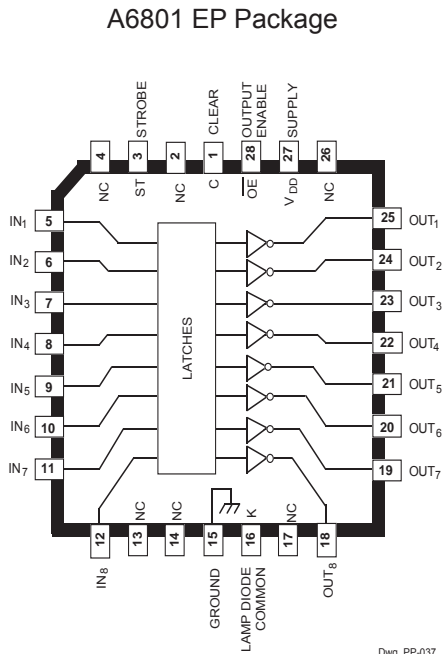
NOTE: Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output off condition regardless of the data or STROBE input levels. A high

OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.



Dwg. PP-014A

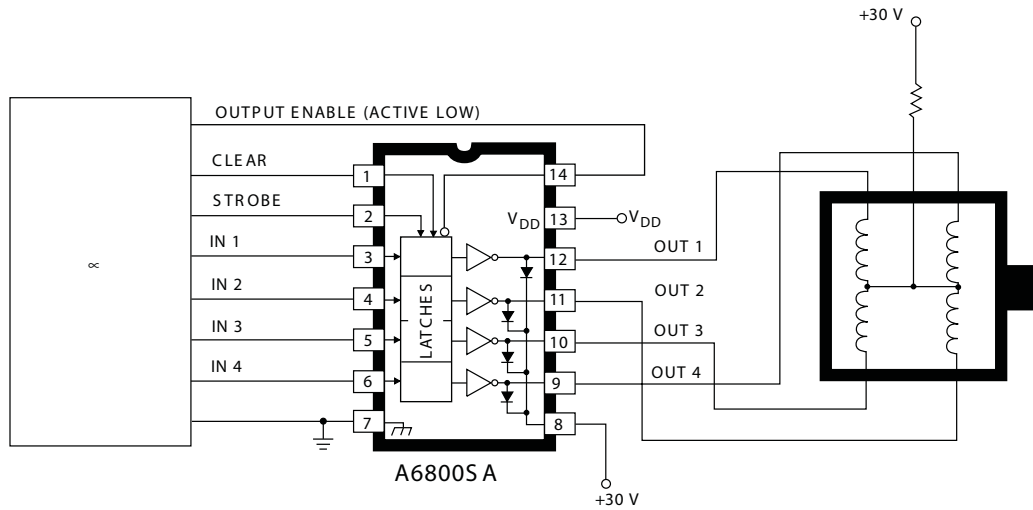
Note: The A6800 SOIC and DIP packages are electrically identical and share a common terminal number assignment.



Dwg. PP-037

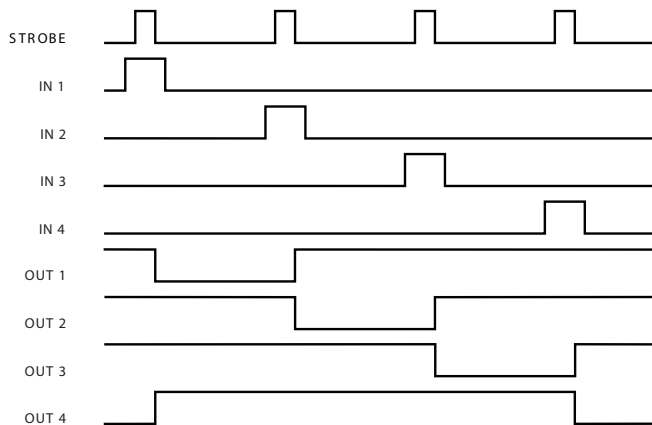
Dwg. PP-015-1

**TYPICAL APPLICATION  
UNIPOLAR STEPPER-MOTOR DRIVE**



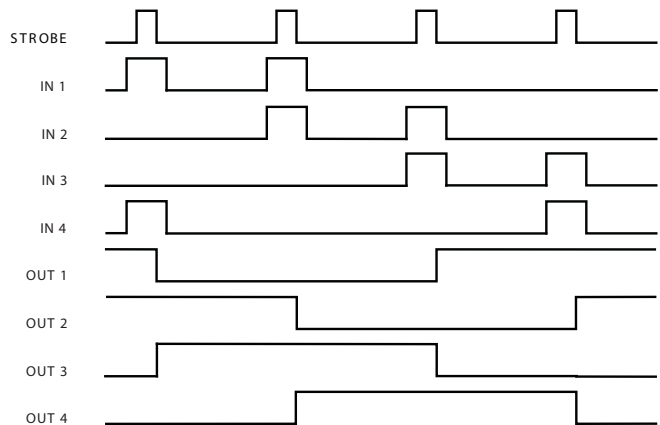
Dwg. No. B-1537

**UNIPOLAR WAVE DRIVE**



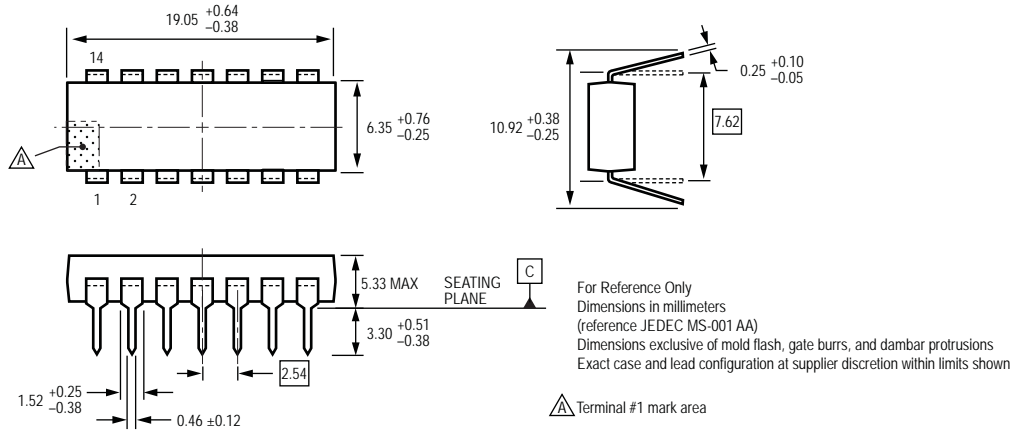
Dwg. GP-060

**UNIPOLAR 2-PHASE DRIVE**



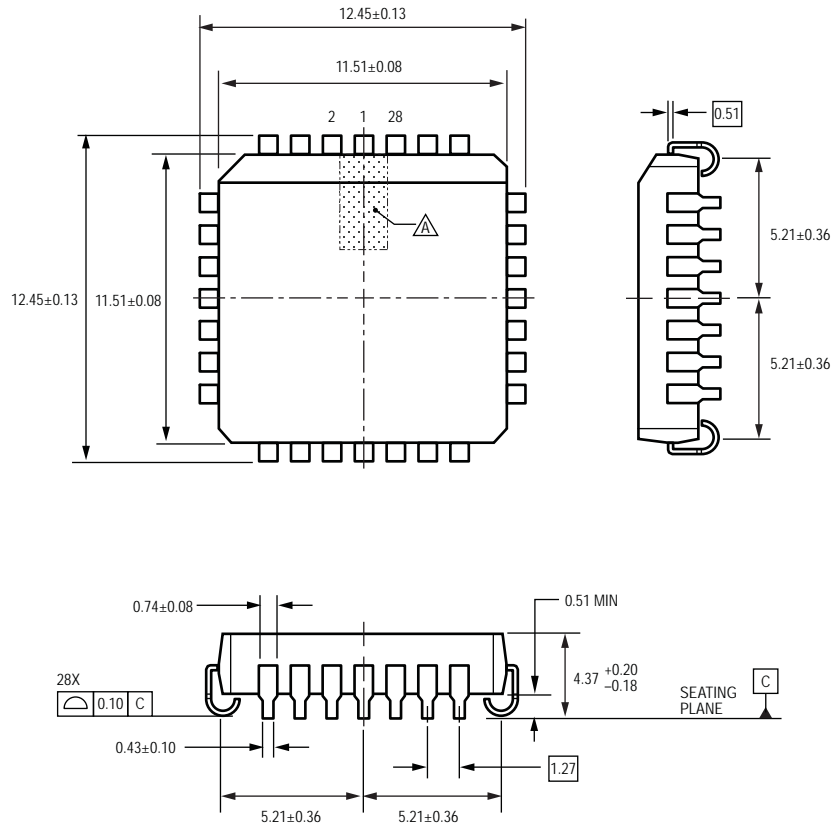
Dwg. GP-060-1

**Package A (A6800) 14-pin DIP**



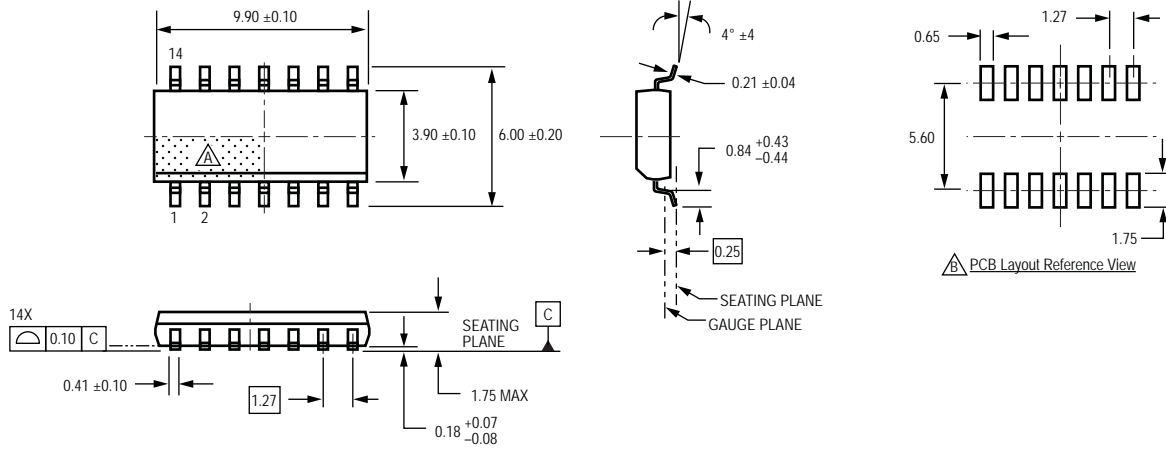


**Package EP (A6801) 28-pin PLCC**



For Reference Only  
(reference JEDEC MS-018 AB)  
Dimensions in millimeters  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown  
△ Terminal #1 mark area

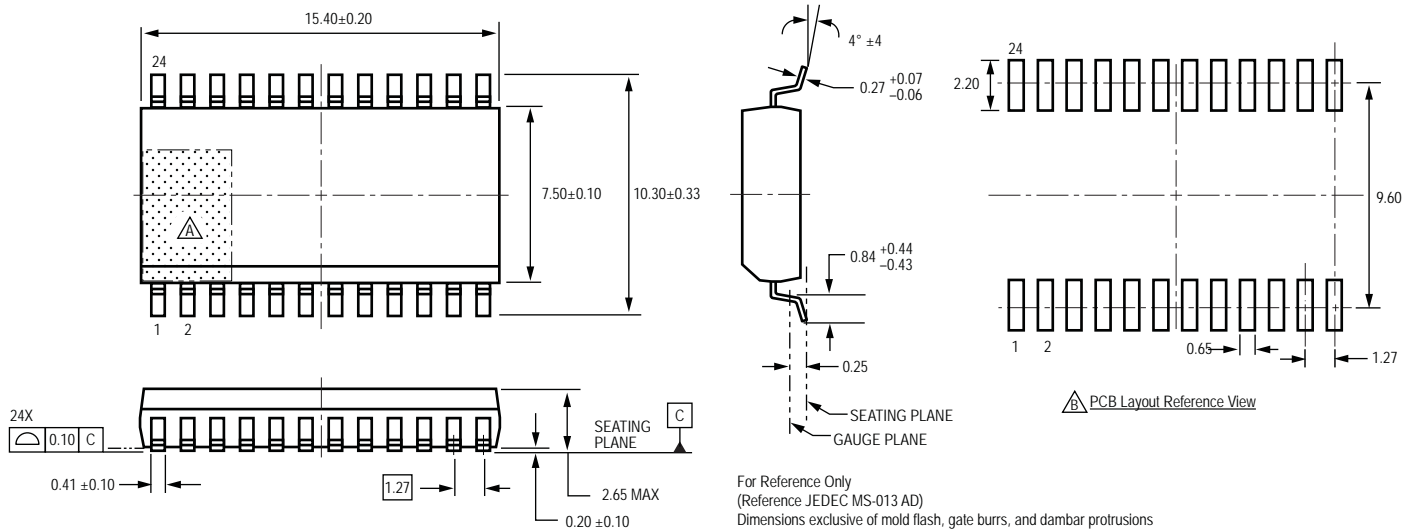
**Package L (A6800) 14-pin SOICN**



For Reference Only  
Dimensions in millimeters  
(reference JEDEC MS-012 AB)  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

△ Terminal #1 mark area  
△ Reference pad layout (reference IPC SOIC127P600X175-14M)  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

**Package LW (A6801) 24-pin SOICW**



For Reference Only  
(Reference JEDEC MS-013 AD)  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

△ Terminal #1 mark area  
△ Reference pad layout (reference IPC SOIC127P1030X265-24M)  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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