Hall-Effect Latch / Bipolar Switch

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- High-speed, 4-phase chopper stabilization
- Low operating voltage down to 3 V
- High sensitivity
- Stable switchpoints
- Robust EMC

Packages:

3-Pin SOT23W (suffix LH)

3-Pin SIP (suffix UA)

Not to scale

DESCRIPTION

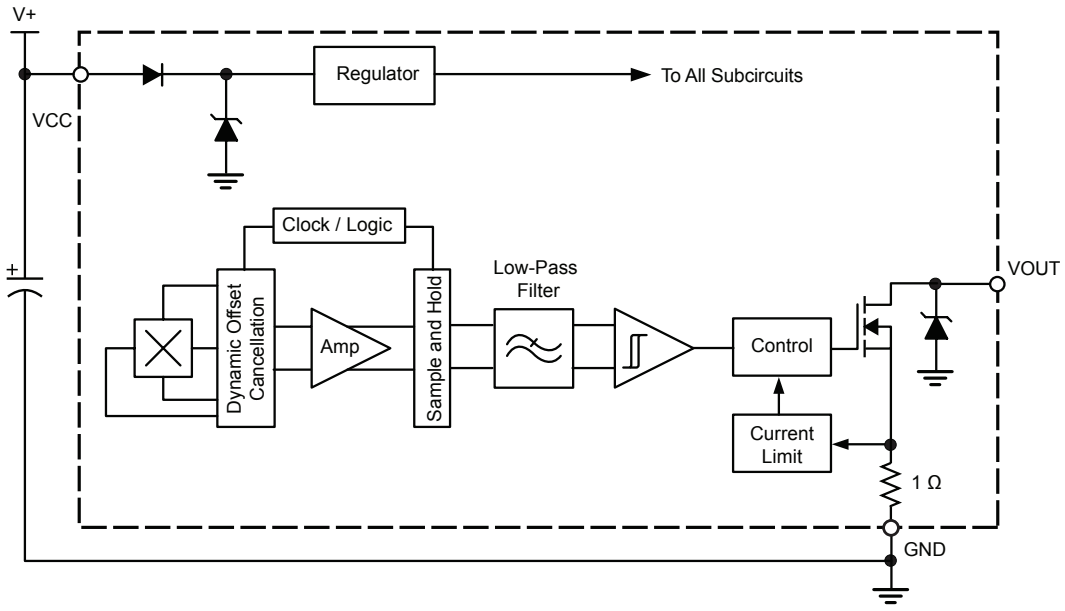
The A1250 Hall-effect sensor IC is a temperature-stable, stress-resistant bipolar switch. This device is the most sensitive Hall-effect device in the Allegro™ bipolar switch family and is intended for ring-magnet sensing. Superior high-temperature performance is made possible through an Allegro patented dynamic offset cancellation that utilizes chopper stabilization. This method reduces the offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

The A1250 includes the following on a single silicon chip: a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short-circuit-protected open-drain output. Advanced BiCMOS wafer fabrication processing takes advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries.

The A1250 Hall-effect bipolar switch turns on in a south polarity magnetic field of sufficient strength and switches off in a north polarity magnetic field of sufficient strength. Because the output state is not defined if the magnetic field is diminished or removed, to ensure that the device switches, Allegro recommends using magnets of both polarities and of sufficient strength in the application.

The A1250 is rated for operation in the ambient temperature

Continued on the next page…



Functional Block Diagram

Description (continued)

range L, –40°C to 150°C. Two package styles provide magnetically optimized solutions for most applications. Each package is lead (Pb) free version, with 100% matte-tin-plated leadframe.

SPECIFICATIONS

Selection Guide

Part Number	Packing*	Mounting	Ambient, T_A (°C)
A1250LLHLT-T	7-in. reel, 3000 pieces/reel	Surface mount	–40 to 150
A1250LLHLX-T	13-in. reel, 10 000 pieces/reel	Surface mount	
A1250LUA-T	Bulk, 500 pieces/bag	SIP through hole	

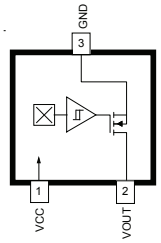
*Contact Allegro for additional packing options.

Absolute Maximum Ratings

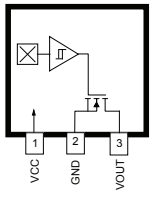
Characteristic	Symbol	Notes	Rating	Unit*
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Off Voltage	V_{OUT}		28	V
Reverse Output Voltage	V_{ROUT}		–0.6	V
Output Current	$I_{OUTSINK}$		Internally limited	A
Reverse Output Current	I_{ROUT}		–10	mA
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

*1 G (gauss) = 0.1 mT (millitesla).

Pin-Out Diagrams and Terminal List Table



Package LH



Package UA

Terminal List Table

Name	Number		Function
	Package LH	Package UA	
VCC	1	1	Device supply
VOUT	2	3	Device output
GND	3	2	Ground

OPERATING CHARACTERISTICS: valid at T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Operating T_J < 165°C	3.0	–	24	V
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 24 V, B < B_{RP}	–	–	10	µA
Output On Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	–	–	500	mV
Output Current Limit	I_{OM}	B > B_{OP}	30	–	60	mA
Power-On Time	t_{PO}	V_{CC} > 3.0 V	–	–	25	µs
Chopping Frequency	f_c		–	160	–	kHz
Output Rise Time[1]	t_r	R_{LOAD} = 820 Ω, C_S = 20 pF	–	–	2	µs
Output Fall Time[1]	t_f	R_{LOAD} = 820 Ω, C_S = 20 pF	–	–	2	µs
Supply Current	I_{CCON}	B > B_{OP}	–	–	4	mA
	I_{CCOFF}	B < B_{RP}	–	–	4	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V	–	–	–2	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 6.5 mA, T_A = 25°C	28	–	–	V
Supply Zener Current	I_Z	V_{CC} = 28 V	–	–	7	mA
MAGNETIC CHARACTERISTICS[2]: valid at T_A = –40°C to 150°C, $T_J \le T_J$(max), unless otherwise noted						
Operate Point	B_{OP}		–10	5	25	G
Release Point	B_{RP}		–25	–5	10	G
Hysteresis	B_{HYS}		5	10	25	G

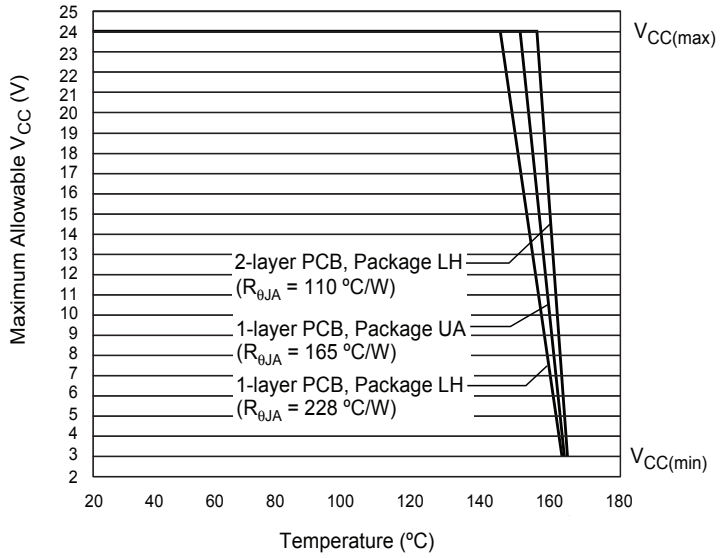
[1]Guaranteed by design.
[2]Magnetic flux density, B, is indicated as negative value for north-polarity fields, and positive for south-polarity fields.

THERMAL CHARACTERISTICS: may require derating at maximum conditions; see application information

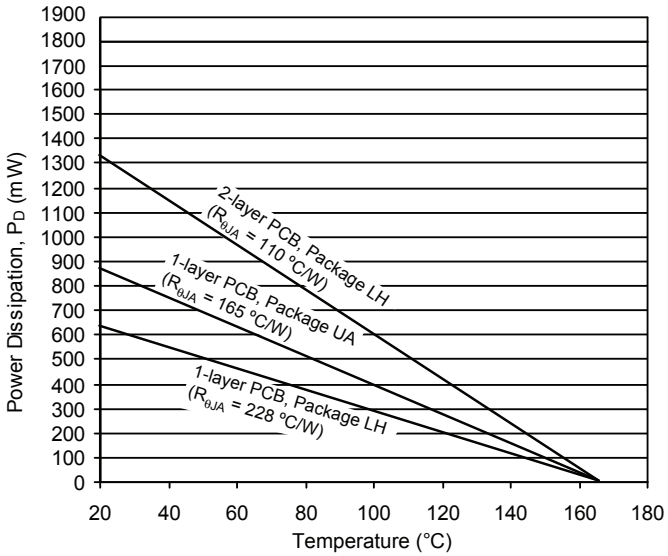
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro Web site.

Power Derating Curve

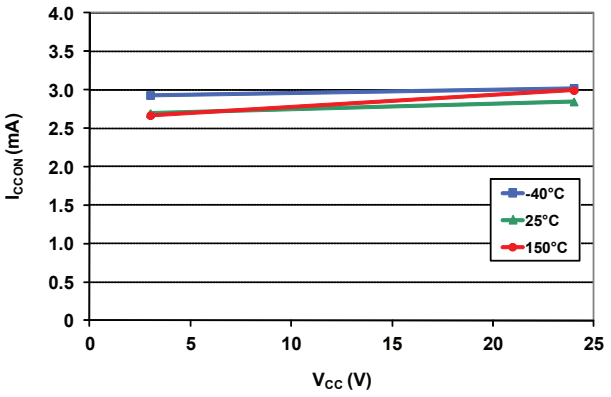


Power Dissipation versus Ambient Temperature

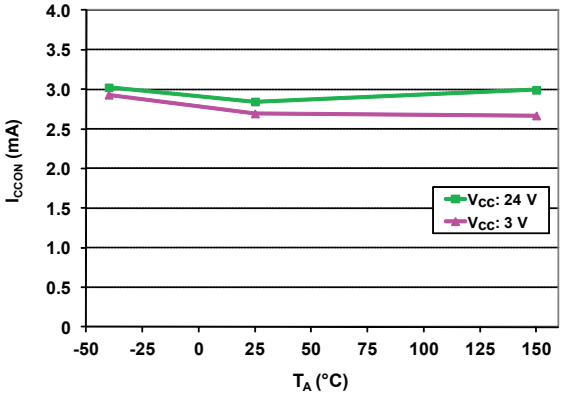


CHARACTERISTIC PERFORMANCE DATA

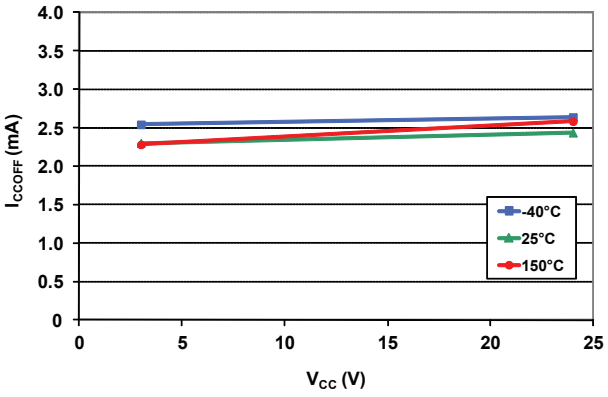
Supply Current (On) versus Supply Voltage



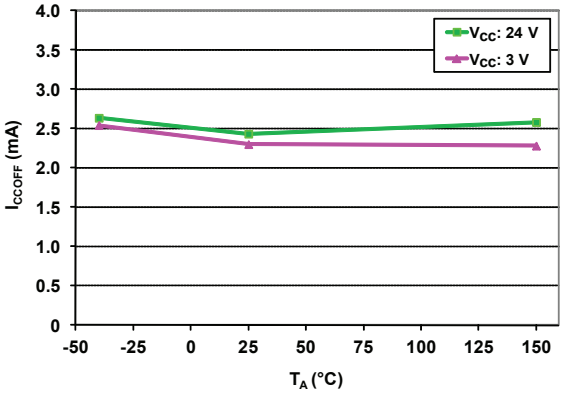
Supply Current (On) versus Ambient Temperature



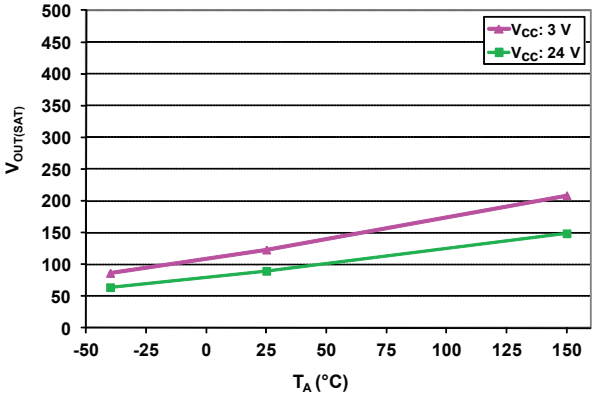
Supply Current (Off) versus Supply Voltage



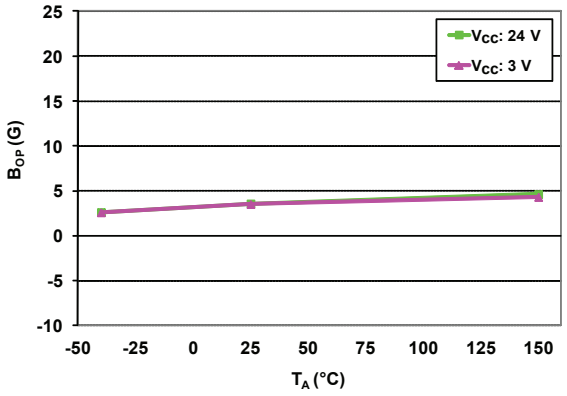
Supply Current (Off) versus Ambient Temperature



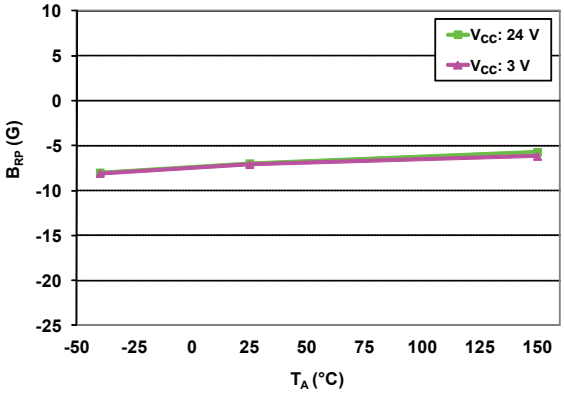
$V_{OUT(SAT)}$ versus Ambient Temperature
I_{OUT} = 20 mA



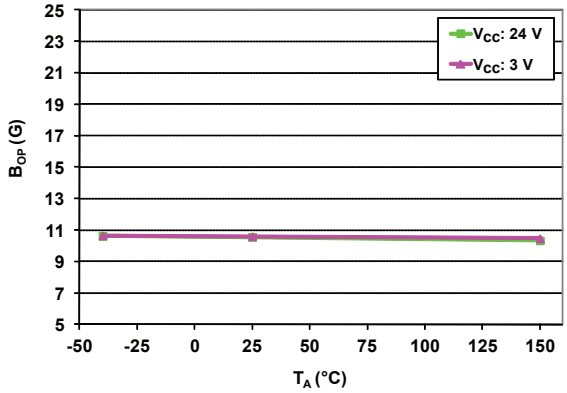
Operate Point versus Ambient Temperature



Release Point versus Ambient Temperature



Hysteresis versus Ambient Temperature



FUNCTIONAL DESCRIPTION

The output of this device switches low (turns on) when a magnetic field perpendicular to the Hall sensor IC exceeds the operate point threshold, B_{OP}. After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of sinking current up to the short circuit current limit I_{OM}, which is a minimum of 30 mA. When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Given the magnetic parameter specifications (refer to Magnetic Characteristics table), bipolar switches will operate in one of three modes, depending on switchpoints. For typical values of B_{OP} and B_{RP}, the device will operate as a latch, as shown in figure 1a. Note that, when the magnetic flux density exceeds a switchpoint, the output will retain its state when the magnetic field is removed. The other two modes of operation are the unipolar switch and the negative switch, shown in panels 1b and 1c, respectively. The unipolar switch type operates only in a south polarity field, and will switch to the high state if the magnetic field is removed. The negative switch operates only in a north polarity field, and will switch to the low state if the magnetic field is removed.

Individual bipolar switch devices exhibit any one of the three switching behaviors: latch, unipolar, or negative switch. Because these devices are not guaranteed to behave as latches, magnetic fields of sufficient magnitude and alternate polarity are required to ensure output switching.

Powering up the device in the hysteresis band, that is in a magnetic field less than B_{OP} and higher than B_{RP}, allows an indeterminate output state. Note that this hysteresis band encompasses zero magnetic field on devices that exhibit latch behaviors. The correct state is determined after the first magnetic excursion beyond B_{OP} or B_{RP}.

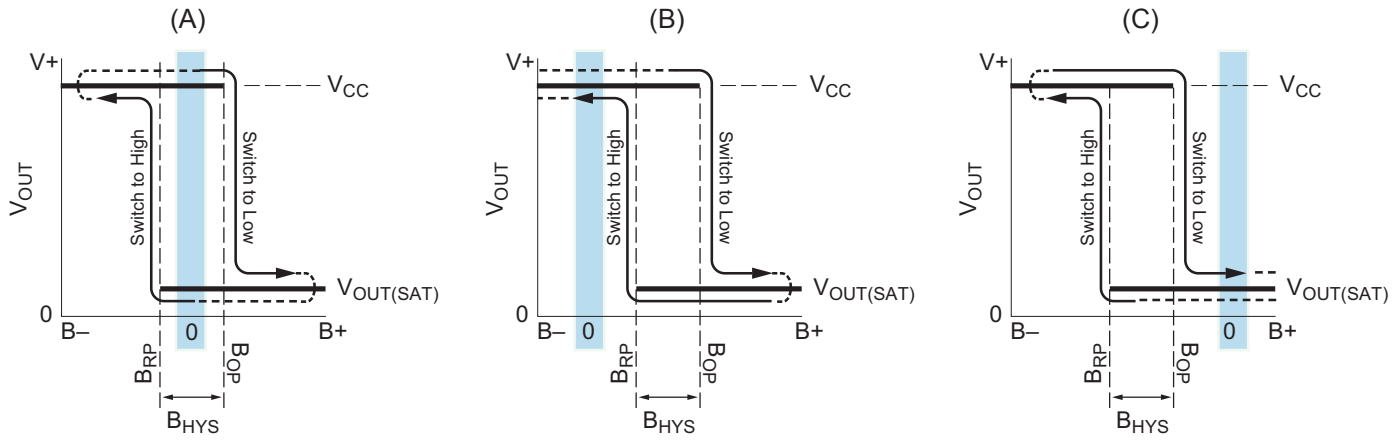


Figure 1: Bipolar Device Output Switching Modes

These behaviors can be exhibited when using a circuit such as that shown in figure 1. Panel A displays the hysteresis when a device exhibits latch mode (note that the B_{HYS} band incorporates B = 0), panel B shows unipolar switch behavior (the B_{HYS} band is more positive than B = 0), and panel C shows negative switch behavior (the B_{HYS} band is more negative than B = 0). Bipolar devices, such as the A1250, can operate in any of the three modes.

APPLICATION INFORMATION

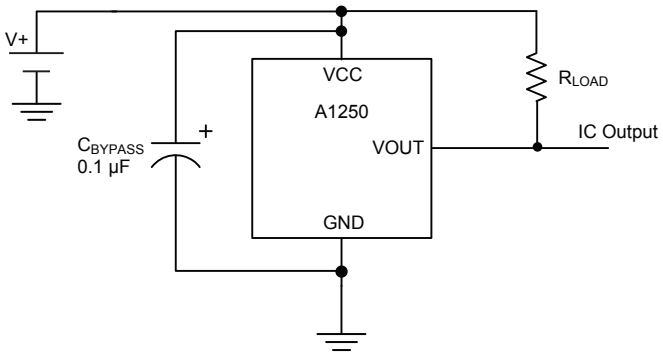


Figure 2: Typical Application Circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a patented technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high frequency sampling clock. For demodulation process, a sample and hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

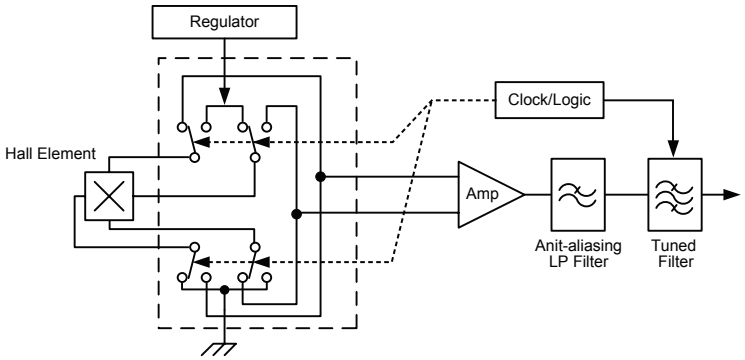


Figure 3: Concept of Chopper Stabilization Technique

POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_J(max)$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{IN} = 12 V, I_{IN} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{IN} \times I_{IN} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level, without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165 °C/W, $T_J(max)$ =165°C, $V_{CC}(max)$ =24 V, and $I_{CC}(max)$ = 4 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 91\ mW \div 4\ mA = 23\ V$$

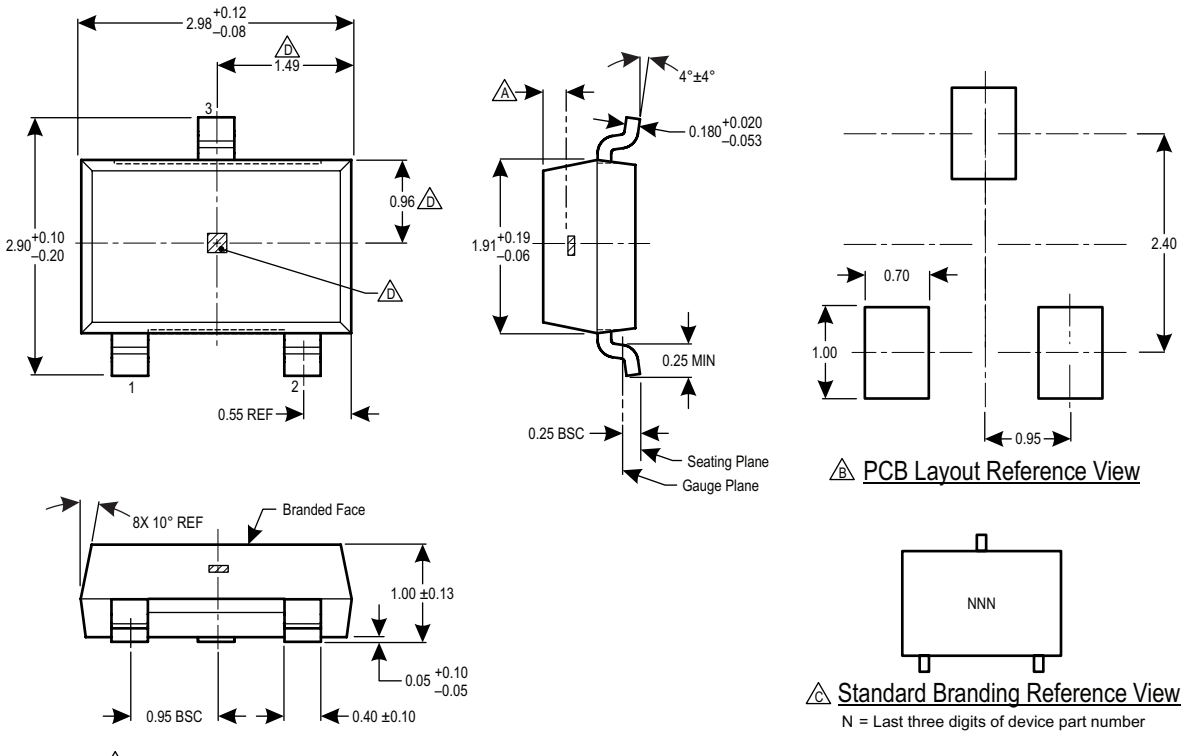
The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC}(est)$.

Compare $V_{CC}(est)$ to $V_{CC}(max)$. If $V_{CC}(est) \leq V_{CC}(max)$, then reliable operation between $V_{CC}(est)$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC}(est) \geq V_{CC}(max)$, then operation between $V_{CC}(est)$ and $V_{CC}(max)$ is reliable under these conditions.

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-2840)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.28 ±0.04 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Figure 4: Package LH, 3-Pin SOT23W

For Reference Only – Not for Tooling Use

(Reference DWG-9013)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

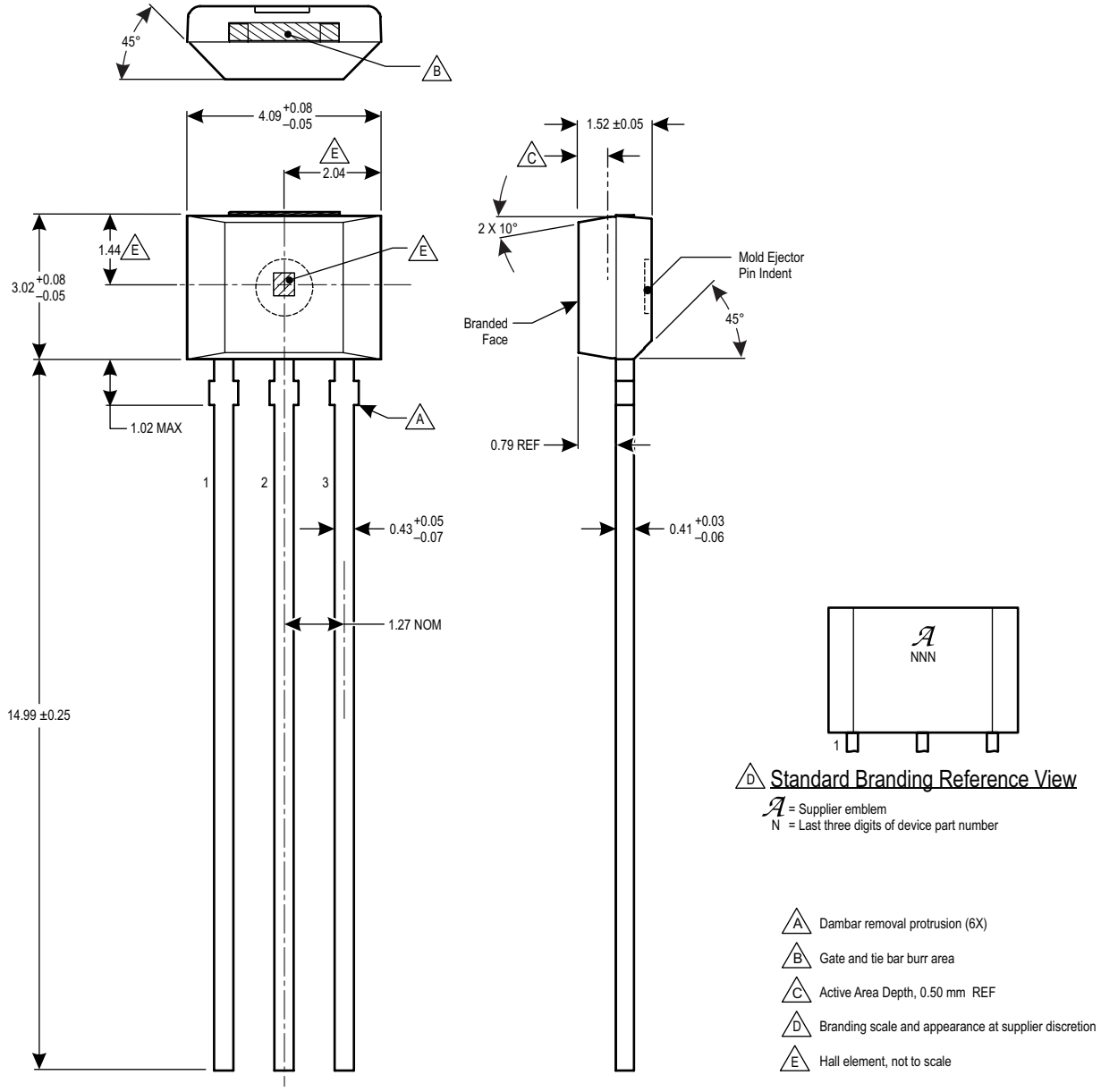


Figure 5: Package UA, 3-Pin SIP

Revision History

Revision	Revision Date	Description of Revision
1	March 22, 2012	Update product selection
2	October 29, 2014	Corrected tolerance on Package Outline Drawing
3	February 4, 2015	Corrected dimension on Package Drawing
4	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits

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