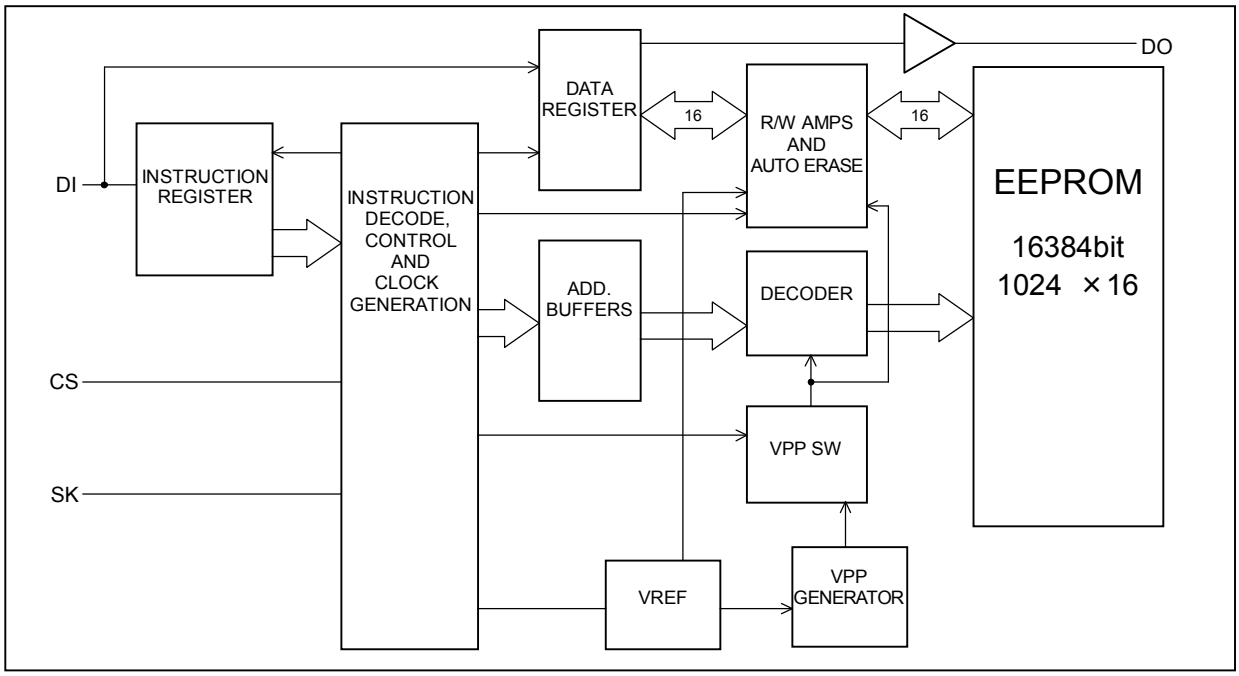
AK93C85A

16Kbit Serial CMOS EEPROM

Features

- ☐ ADVANCED CMOS EEPROM TECHNOLOGY
- ☐ READ/WRITE NON-VOLATILE MEMORY
- ☐ WIDE VCC OPERATION : VCC = 1.8V to 5.5V
- ☐ 16384 bits, 1024 x 16 organization
- ☐ SERIAL INTERFACE
  - Interfaces with popular microcontrollers and standard microprocessors
- ☐ LOW POWER CONSUMPTION
  - 0.4mA Max. Read Operation
  - 0.8μA Max. Standby
- ☐ High Reliability
  - Endurance : 100K cycles
  - Data Retention : 10 years
- ☐ Automatic address increment (READ)
- ☐ Automatic write cycle time-out with auto-ERASE (Max. 8ms: VCC=4.5V to 5.5V)
- ☐ Busy/Ready status signal
- ☐ Software controlled write protection
- ☐ IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package (SSOP)



Block Diagram

General Description

The AK93C85A is a 16384-bit serial CMOS EEPROM divided into 1024 registers of 16 bits each. The AK93C85A has 4 instructions such as READ, WRITE, EWEN and EWDS. Those instructions control the AK93C85A.
The AK93C85A can operate full function under wide operating voltage range from 1.8V to 5.5V. The charge up circuit is integrated for high voltage generation that is used for write operation.
A serial interface of AK93C85A, consisting of chip select (CS), serial clock (SK), data-in (DI) and data-out (DO), can easily be controlled by popular microcontrollers or standard microprocessors. AK93C85A takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin (SK). And at read operation, AK93C85A takes out the read data from a register to data output pin (DO) synchronously with rising edge of SK.
The DO pin is usually in high impedance state. The DO pin outputs "L" or "H" in case of data output or $\overline{\text{Busy}}$/Ready signal output.

・Software controlled write protection
When VCC is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of WRITE instruction is disabled. Before WRITE instruction is executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or VCC is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.

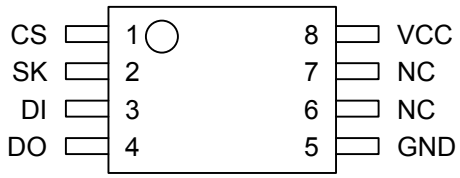
・$\overline{\text{Busy}}$/Ready status signal
After a write instruction, the DO output serves as a $\overline{\text{Busy}}$/Ready status indicator. After the falling edge of the CS initiates the self-timed programming cycle, the DO indicates the $\overline{\text{Busy}}$/Ready status of the chip if the CS is brought high after a minimum of 250ns (tCS). DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.
The $\overline{\text{Busy}}$/Ready status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state.
The $\overline{\text{Busy}}$/Ready signal outputs until a start bit (Logic"1") of the next instruction is given to the part.

■ Type of Products

Model	Memory size	Temp. Range	VCC	Package
AK93C85AM	16K bits	-40°C to +85°C	1.8V to 5.5V	8pin Plastic SSOP

Pin Arrangement

AK93C85AM



8pin SSOP

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
NC	Not Connected *1

*1: Please Open NC pin.

Functional Description

The AK93C85A has 4 instructions such as READ, WRITE, EWEN and EWDS. A valid instruction consists of a Start Bit (Logic"01"), the appropriate Op Code and the desired memory Address location.
The CS pin must be brought low for a minimum of 250ns (tCS) between each instruction when the instruction is continuously executed.

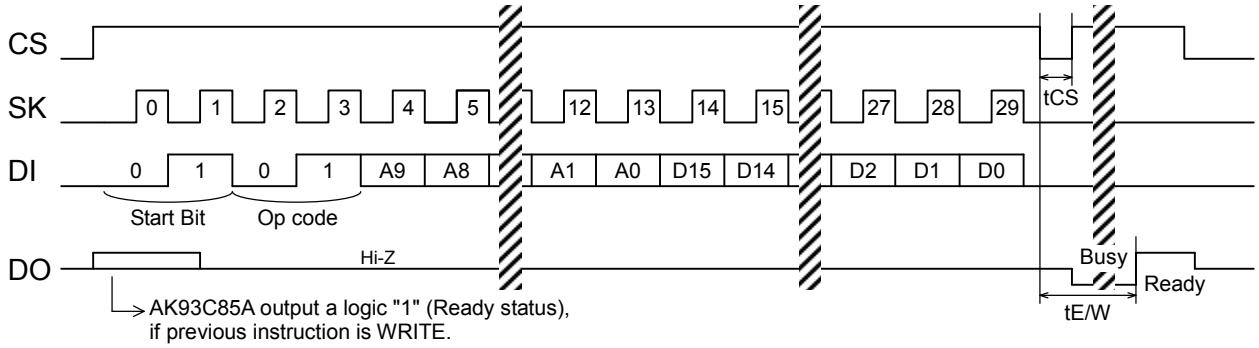
Instruction	Start Bit	Op Code	Address	Data	Comments
READ	01	10	A9-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	01	01	A9-A0	D15-D0	Writes register.
EWEN	01	00	11XXXXXXXX		Write enable must precede all programming modes.
EWDS	01	00	00XXXXXXXX		Disables all programming instructions.
WRAL	01	00	01XXXXXXXX	D15-D0	Writes all registers.

X: Don't care

(Note) ・ The WRAL instruction are used for factory function test only.
User can't use the WRAL instruction.
・ The AK93C85A perceives the start bit in the logic"01" and also "001".

WRITE

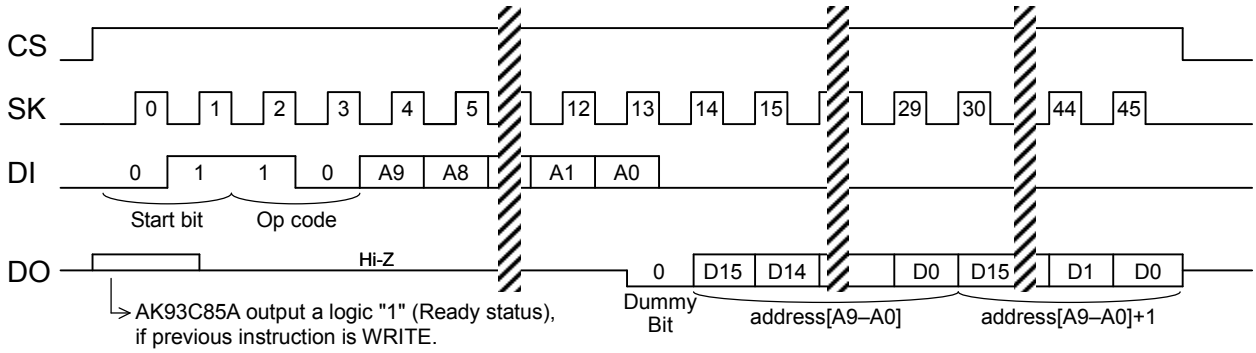
The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the DI pin, the CS pin must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO indicates the Busy/Ready status of the chip if the CS is brought high after a minimum of 250ns (tCS). DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.



WRITE

READ

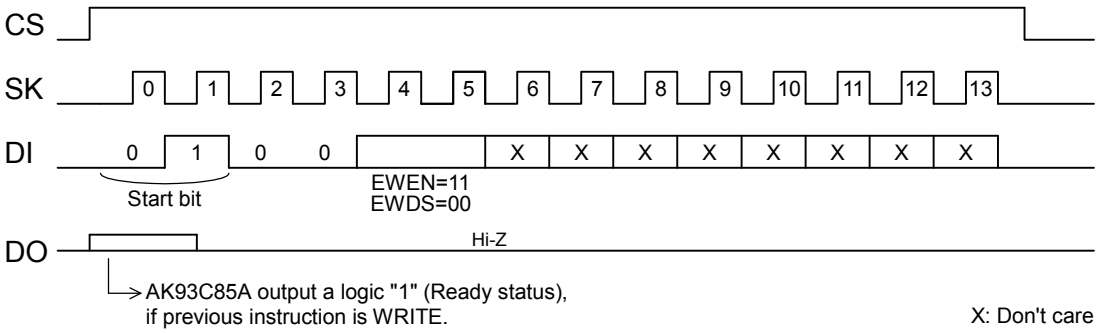
The read instruction is the only instruction which outputs serial data on the DO pin.
Following the Start bit, first Op code and address are decoded, then the data from the selected memory location is available at the DO pin. A dummy bit (logical "0") precedes the 16-bit data from the selected memory location. The output data changes are synchronized with the rising edges of the serial clock (SK).
The data in the next address can be read sequentially by continuing to provide clock. The address automatically cycles to the next higher address after the 16bit data shifted out.
When the highest address is reached ($3FF), the address counter rolls over to address $000 allowing the read cycle to be continued indefinitely.



READ

EWEN / EWDS

When VCC is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of WRITE instruction is disable. Before WRITE instruction is executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or VCC is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.



EWEN / EWDS

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+7.0	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	1.8	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

Electrical Characteristics

(1) D.C. ELECTRICAL CHARACTERISTICS

(1.8V ≤ VCC ≤ 5.5V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V, tSKP=1.0μs, *1		5.5	mA
	ICC2	VCC=1.8V, tSKP=4.0μs, *1		3.0	mA
Current Dissipation (READ, EWEN, EWDS)	ICC3	VCC=5.5V, tSKP=1.0μs, *1		0.4	mA
	ICC4	VCC=1.8V, tSKP=4.0μs, *1		0.1	mA
Current Dissipation (Standby)	I_{CCSB}	VCC=5.5V *2		0.8	μA
Input High Voltage	VIH		0.8 x VCC	VCC + 0.5	V
Input Low Voltage	VIL		-0.1	0.2 x VCC	V
Output High Voltage	VOH1	2.5V ≤ VCC ≤ 5.5V IOH=-0.1mA	0.8 x VCC		V
	VOH2	1.8V ≤ VCC < 2.5V IOH=-0.1mA	0.8 x VCC		V
Output Low Voltage	VOL1	2.5V ≤ VCC ≤ 5.5V IOL=1.0mA		0.4	V
	VOL2	1.8V ≤ VCC < 2.5V IOL=0.1mA		0.4	V
Input Leakage	ILI	VCC=5.5V, VIN=5.5V		±1.0	μA
Output Leakage	ILO	VCC=5.5V, VOUT=5.5V, CS=GND		±1.0	μA

*1 : VIN=VIH/VIL, DO=Open

*2 : VIN=VCC/GND, CS=GND, DO=Open

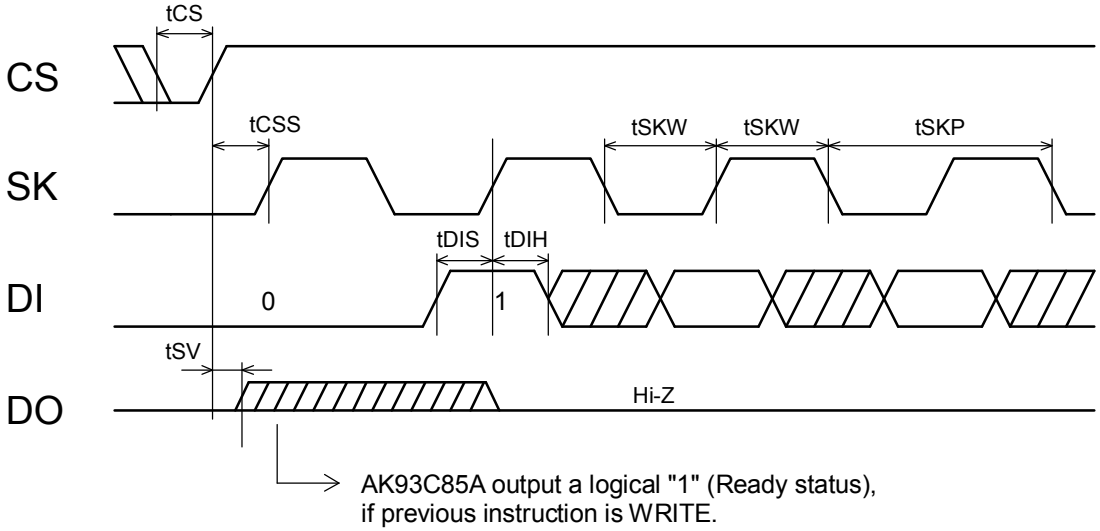
(2) A.C. ELECTRICAL CHARACTERISTICS

(1.8V ≤ VCC ≤ 5.5V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

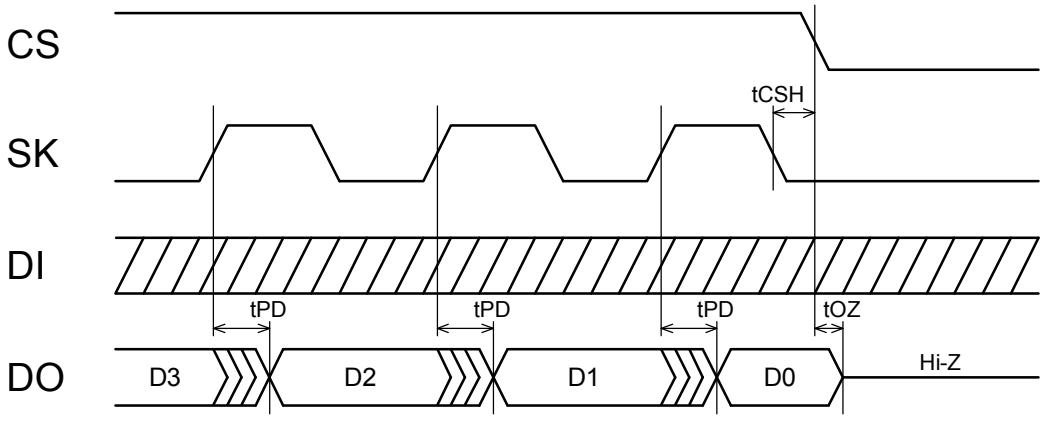
Parameter	Symbol	Condition	Min.	Max.	Unit
SK Cycle Time	tSKP1	4.5V ≤ VCC ≤ 5.5V	1.0		μs
	tSKP2	2.0V ≤ VCC < 4.5V	2.0		μs
	tSKP3	1.8V ≤ VCC < 2.0V	4.0		μs
SK Pulse Width	tSKW1	4.5V ≤ VCC ≤ 5.5V	500		ns
	tSKW2	2.0V ≤ VCC < 4.5V	1.0		μs
	tSKW3	1.8V ≤ VCC < 2.0V	2.0		μs
CS Setup Time	tCSS		100		ns
CS Hold Time	tCSH		0		ns
Data Setup Time	tDIS		200		ns
Data Hold Time	tDIH		200		ns
Output delay *3	tPD1	4.5V ≤ VCC ≤ 5.5V		500	ns
	tPD2	2.0V ≤ VCC < 4.5V		1.0	μs
	tPD3	1.8V ≤ VCC < 2.0V		2.0	μs
Selftimed Programming Time	tE/W1	4.5V ≤ VCC ≤ 5.5V		8	ms
	tE/W2	1.8V ≤ VCC < 4.5V		10	ms
Min CS Low Time	tCS		250		ns
CS to Status Valid1	tSV	CL=100pF		500	ns
CS to Output High-Z	tOZ1	2.0V ≤ VCC ≤ 5.5V		100	ns
	tOZ2	1.8V ≤ VCC < 2.0V		250	ns

*3 : CL=100pF

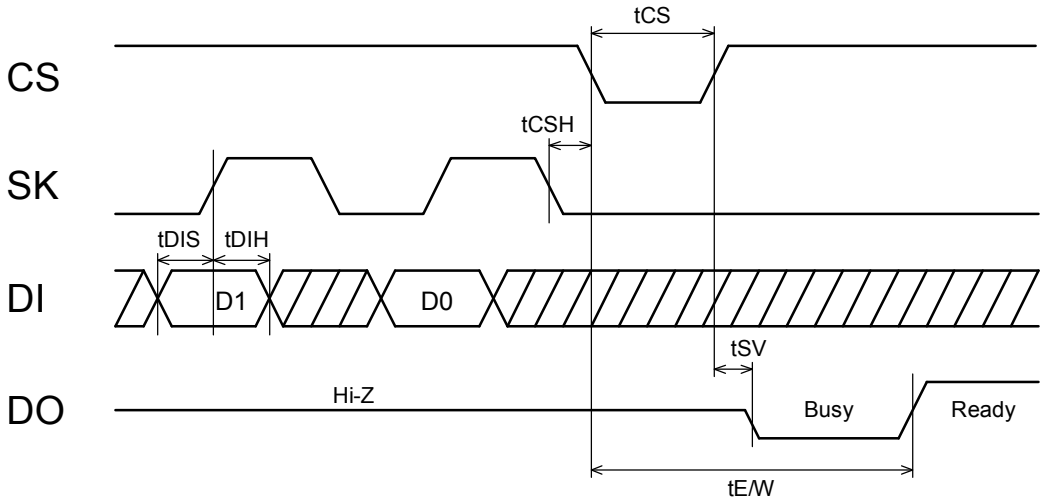
Synchronous Data timing



The Start of Instruction



The End of Instruction



$\overline{\text{Busy}}$/Ready Signal Output

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