AK8996/W

Pressure Sensor Interface IC

The AK8996 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation. It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8996. The AK8996 is available in either a 16-pin QFN package or in wafer form.

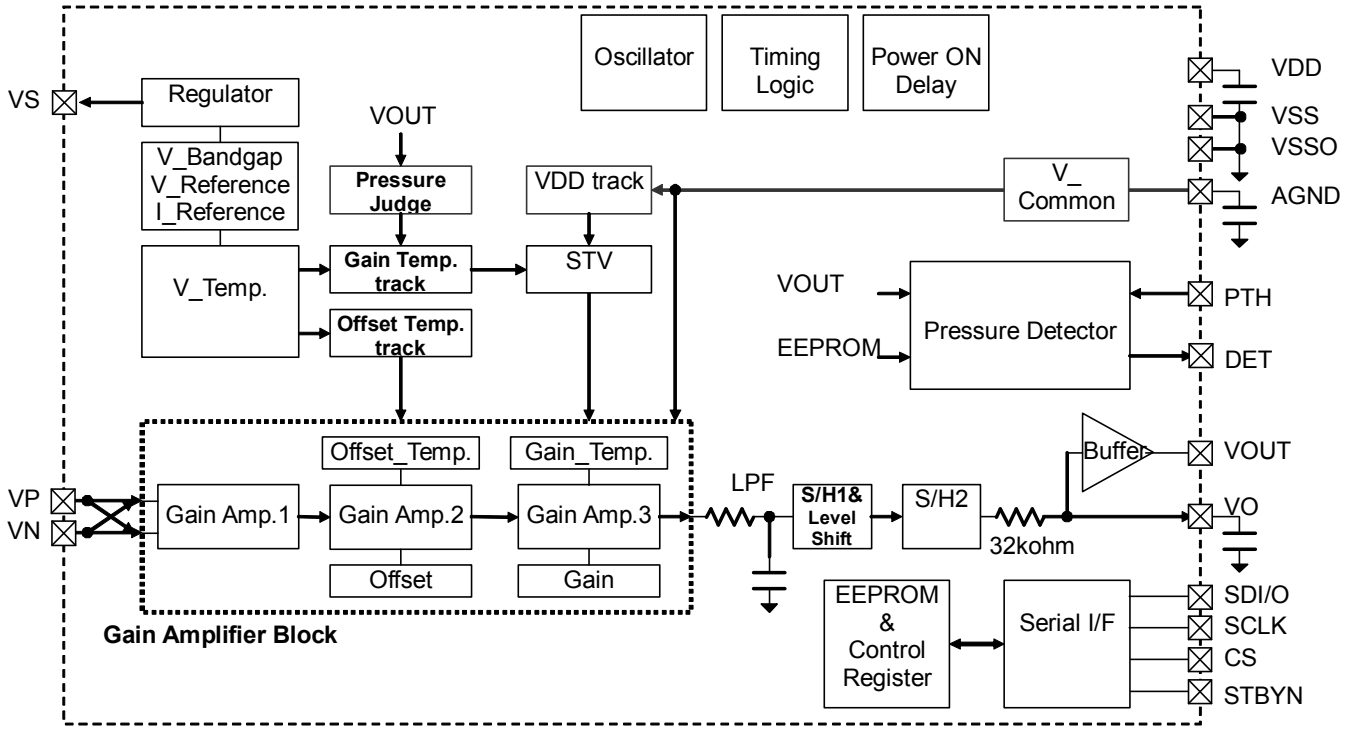
Features

- **Pressure sensor compensation and excitation IC (Analog output)**
- **Low power consumption: 350µA typ. @ 100Hz sampling**
- **Standby function: 1µA max.**
- **Low-voltage operation: 2.2 to 3.6V, 5V±10%**
- **Operating temperature range: -40 to 105ºC**
- **Integrated span voltage switching function (by a factor of 5, typ.)**
  - **Resolution: Gain Amp. 1: 3-bits; Gain Amp. 2:1-bit**
    Adjustment step: factor of 1/step (by a factor of 2 to 9);
    factor of 1/step (by a factor of 1 and 2)
- **Integrated sensor output compensation**
  - **Offset voltage adjustment**
    - **Resolution: Rough: 4-bits; Fine: 7-bits**
    - **Adjustment step: Rough: 7.5%/step; Fine 0.125%/step @VDD: 5.0V**
  - **Offset voltage temperature drift adjustment (1st/2nd order coefficient)**
    - **Resolution: 10-bits; 8-bits**
    - **Adjustment step: 0.196%/step; 0.787%/step**
  - **Output span voltage adjustment**
    - **Resolution: 9-bits**
    - **Adjustment value: 100/[100+0.25*N](%) N: -256 to +255**
  - **Sensitivity temperature drift adjustment (1st/2nd order coefficient)**
    - **Resolution: 10-bits; 8-bits**
    - **Adjustment step: 0.196%/step; 0.787%/step**
- **Integrated output reference voltage switching function**
  - **Resolution: Rough 5-bits; Fine 6-bits**
  - **Adjustment step: 0.0005*VDD/step (0.0785*VDD to 0.9215*VDD) @VO**
- **Integrated criteria adjustment function for determining positive/negative pressure**
  - **Resolution: 10-bits**
  - **Adjustment step: 0.001*VDD/step (0.05*VDD to 0.95*VDD)**
- **Integrated output gain (buffer gain) switching function (by a factor of 4, typ.)**
  - **Resolution: 3-bits**
  - **Adjustment step: factor of 0.5/step (by a factor of 2 to 4)**
- **Integrated sampling frequency switching function: 100Hz, 1kHz, 2kHz, 10.24kHz**
- **Ratiometric voltage output**
- **Integrated constant voltage source for pressure sensor**
  : 2.0V @VDD: 2.2 to 3.6V; 4.0V @VDD: 5.0V±10%

- **Integrated reference voltage & reference current generator**
  - **VREF voltage adjustment control**
    - **Resolution: 3-bits**
    - **Adjustment step: 1%/step**
  - **IREF current adjustment control**
    - **Resolution: 4-bits**
    - **Adjustment step: 2.7%/step typ.**
- **Integrated temperature sensor**
  - **Temperature range: -40 to 105°C**
  - **Temperature sensor output voltage adjustment control**
    - **Resolution: 6-bits**
    - **Adjustment step: 0.2%/step**
- **Integrated timer oscillator for intermittent operation (1024 kHz typ.)**
  - **Oscillating frequency adjustment control**
    - **Resolution: 4-bits**
    - **Adjustment step: 5%/step**
- **Integrated EEPROM for compensation values and control data storage**
  - **Size: 157 bits**
  - **Endurance: 1,000 times or more**
  - **Retention time: 10 years or more @Ta: 105°C**
- **Integrated pressure detection/self-diagnosis function**
- **Supply type: Wafer PKG (UQFN16)**

Product name	Supply Type	Note
AK8996	PKG (UQFN16)	
AK8996W	Wafer	

Block Diagram



Overview

The AK8996 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation. It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8996.

The internal compensation circuit is accomplished through DACs, with 4-bit and 7-bit resolution to adjust offset voltage of the sensor, and the secondary characteristics compensator for the associated temperature drift, coupled with 9-bit resolution to adjust the span voltage and another secondary characteristics compensator for its associated temperature drift. Depending on the application, the internal EEPROM values can be pre-configured to enable adjustment of the reference sensitivity and the output reference voltage. For the adjustment procedure, see the sections on "Adjustment Sequence" and "Functional Description".

Depending on the application, the AK8996's internal EEPROM values can be preconfigured to enable adjustment of the reference sensitivities and output reference voltages. Sampling frequencies can be switched between 100Hz, 1kHz, 2kHz and 10.24kHz using the internal EEPROM data.

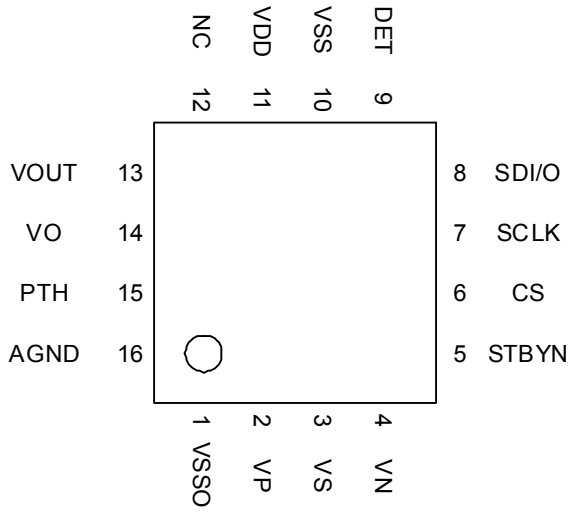
The AK8996 is provided with a pressure detection circuit. If the applied pressure exceeds the defined voltage threshold at the PTH terminal, a high-level signal is output on the DET pin. The threshold can be adjusted by the internal EEPROM data. The AK8996 is also provided with a self-diagnostic function. Upon power-up or at initial operation immediately after exiting standby mode, this self-test feature checks for the required value at the output (VOUT pin), and if an expected value is not available, the output is assumed to be anomalous and a high-level signal is output on the DET pin, in the same manner as with the pressure detection.

Pin Configuration

1. Wafer Configuration

For the detail, please contact your local sales office or authorized distributor.

2. Package Outline (UQFN16)



Adjustment Characteristics

1) Adjustable Sensor Characteristics (Reference Example)

Item	Symbol	Min.	Typ.	Max.	Units	Comments
Drive voltage	Svs1		4		V	
	Svs2		2		V	
Temperature range	Sta	-40		105	°C	
Sensor resistance	Sres1	3	5		kΩ	VDD: 2.2 to 3.6V & 5V±10%
	Sres2	1	2		kΩ	VDD: 2.7 to 3.6V & 5V±10%
Voltage input span range	Sspnin 1	22.22	80	200	mV	VDD: 5V±10% Note)
	Sspnin 2	11.11	40	100	mV	VDD: 2.2 to 3.6V Note)
Voltage span adjustment range	Sspn	100/164	100/100	100/36.25	times	Note)
Offset voltage adjustment range	Soff1	-48		48	mV	VDD: 5V±10% Note)
	Soff2	-24		24	mV	VDD: 2.2 to 3.6V Note)
Sensitivity temp. drift 2nd order coefficient	Sst21	-0.0016		+0.0016		VDD: 5V±10% Note)
	Sst22	-0.0008		+0.0008		VDD: 2.2 to 3.6V Note)
Sensitivity temp. drift 1st order coefficient	Sst11	-0.32		+0.32		VDD: 5V±10% Note)
	Sst12	-0.3		+0.3		VDD: 2.2 to 3.6V Note)
Offset temp. drift 2nd order coefficient	Sot21	-0.0016		+0.0016		VDD: 5V±10% Note)
	Sot22	-0.0008		+0.0008		VDD: 2.2 to 3.6V Note)
Offset temp. drift 1st order coefficient	Sot11	-0.6		+0.6		VDD: 5V±10% Note)
	Sot12	-0.3		+0.3		VDD: 2.2 to 3.6V Note)

Note) Equivalent input values assumed from the output. See 5) Registers Description 5.1.1) Adjustment block register. This adjustment range includes variations in the AK8996.

2) Adjustment Accuracy

Item	Symbol	Min.	Typ. Note2)	Max. Note3)	Units	Comments
Offset adjustment accuracy	Cof		0.063		%FS	
Offset temp. drift adjustment accuracy	Coft		0.101		%FS	
Output span adjustment accuracy	Csn		0.125		%FS	
Sensitivity temp. adjustment accuracy	Csnt		0.003		%FS	
Sensitivity temp. variation step	Csts		0.268		%FS	
Sensitivity supply voltage variation step	Csvs		0.236		%FS	
Final adjustment accuracy Note1)	Call		0.397	1.0	%FS	

Note1) Call=(Cof^2+Coft^2+Csn^2+Csnt^2+Csts^2+Csvs^2)^(1/2)

Note2) Temp.=105ºC, VDD=4.5V, G1=5x, G3=1.25x, BufG=4x, Offset temp. drift 1st/2nd order coefficient=Min./Max., Sensitivity temp. drift 1st/2nd order coefficient=Min.*1/2, VOUT output band-limited (≤500Hz @Fs=10kHz, ≤100Hz@Fs=2kHz, ≤50Hz@Fs=1kHz, ≤5Hz@Fs=100Hz) effective

Note3) Temp.=-40 to 105ºC, VDD=5V±10%, 3.3V±10%, 3.0V±10%, 2.5V±10%, G1/G3/BufG=Min. to Max., Each temperature coefficient=Min. to Max., VOUT output band-limited (≤500Hz @Fs=10kHz, ≤100Hz@Fs=2kHz, ≤50Hz@Fs=1kHz, ≤5Hz@Fs=100Hz) effective

* The calculation of adjustment accuracy is based on our definition as a reference. The accuracy of product depends on your sensor characteristics and adjustment method.

Description of Blocks

Gain Amplifier Block, LPF & S/H1 & Level Shifter, S/H2 & Buffer

The set of these blocks amplifies, compensates and outputs the pressure sensor level with a normal gain ratio of 50:1. This set of blocks intermittently amplifies, compensates, samples and holds the pressure sensor output. The output stage, with an internal resistor of 32kΩ, is band-limited with a combination of external capacitors, providing a low impedance output through a buffer. A percentage designator is used, benchmarked with 4000mVdc output at 100%, reflecting the 50x increase in differential input from 80mVdc.

Block	Functions
Gain Amp. 1 (G1)	A low-noise high-gain amplifier at the front end. The differential signal is increased by a factor of 5 (typically) (with factors of 2 to 9, in single-factor steps).
Gain Amp. 2 Offset_Temp. Offset Offset Temp. track (G2)	The G1 differential output is converted to single-ended with reference to AGND and typically amplified by a factor of 1 (1 or 2). The preloaded compensation data in the EEPROM enables the pressure sensor offset voltage and offset temperature secondary characteristics to be compensated. Offset adj. Resolution: Rough: 4-bits; Fine: 7-bits Adj. step: Rough: 7.5%; Fine: 0.125% @VDD: 5V Offset temp. drift. Resolution: 1st order coeff: 10-bits; 2nd order coeff: 8-bits Adj. step: 1st order coeff: 0.196%; 2nd order coeff: 0.787%
Gain Amp. 3 Gain_Temp. Gain (G3)	Amplifies the G2 output by a factor of 1.25 (typically). The preloaded compensation data in the EEPROM enables the pressure sensor span voltage and sensitivity temperature secondary characteristics to be compensated. Span adj. Resolution: 9-bits Adj. value: 100/[100+0.25*N](%) N: -256 to +255
STV VDD track Gain Temp. track (STV)	Supply voltage and sensitivity temperature variation compensation circuit. Monitors the AGND voltage to detect the magnitude of supply voltage variation; the pressure sensor sensitivity temperature secondary characteristics compensation values are calculated for entry into G3 using the temperature sensor output voltage and preloaded compensation data (EEPROM data). Sensitivity temperature drift Resolution: 1st order coeff: 10-bits; 2nd order coeff: 8-bits Adj. step: 1st order coeff: 0.196%; 2nd order coeff: 0.787%
Pressure Judge	Compares the pressure sensor VOUT pin output voltage to the threshold voltage to define the sensitivity temperature secondary characteristics compensation coefficient. Pressure determination threshold adj. Resolution: 10-bits Adj. step: 0.001*VDD (0.05*VDD – 0.95*VDD) Note that upon powering up and exiting standby (STBYN pin from low to high), the precise pressure cannot be determined until the VOUT pin output settles, depending on the external capacitance value of the VO pin. When the VOUT pin output voltage is more than the output reference voltage, the positive (+) sensitivity temperature secondary characteristic compensation coefficient is selected; but when the VOUT pin output voltage is less than the output reference voltage, the negative (-) sensitivity temperature secondary characteristic compensation coefficient is selected. Note) If the output reference voltage is half of VDD, pressure threshold adjustment is unnecessary. Even if the compensation coefficient +/- is not used, pressure threshold adjustment is required if the output reference voltage is set to a value other than half of VDD.
LPF	Anti-aliasing filter to eliminate the fold-back noise generated in the sample-and-hold circuit (S/H 1&2) in the later stage. The cutoff frequency is fc=60kHz.

Block	Functions
S/H1& Level shift	Doubles the LPF output for the sample and hold. It also modifies the output reference voltage. Output ref. voltage adj. Resolution: Rough: 5-bits; Fine: 6-bits Adj. step: 0.0005*VDD (0.0785*VDD – 0.9215*VDD) Description is with reference to VO pin. Note) If the output reference voltage is half of VDD, output reference voltage adjustment is unnecessary.
S/H2	Sample-and-hold circuit. A 32kΩ resistor is connected to the output stage. The combination with an external capacitor creates the LPF characteristics. Change the external capacitance value according to the desired signal band for detection using the following equation: fc=1/(2*π*32kΩ*C) (Hz) If the application does not require a low-impedance output, the VO pin output can be used as an alternative. In this case, set the EEPROM data to disable the buffer. Disabling the buffer allows for lower power dissipation. However, since the VO pin has a 32kΩ output impedance, connecting a resistive load will cause output voltage inaccuracies. Note also that the gain retained in the buffer cannot be achieved.
Buffer	Buffer to produce a band-limited output with low impedance. Typically provides a fourfold output (2x to 4x, in 0.5 steps). Reprogramming the EEPROM allows the buffer to be disabled for low power dissipation. (See S/H2.)
Timing Logic	Generates timing sync signals for internal operation and sampling frequencies for sensor output signals. Sampling frequencies can be selected from the EEPROM. Sampling frequency (fs): 100Hz (default); 1 kHz; 2kHz; 10.24kHz
Regulator	Constant voltage generator circuit to drive the sensor. The drive voltage can be selected from the EEPROM depending on the supply voltage being used. Drive voltage: 4.0V @VDD: 5V±10% (default); 2.0V @VDD: 2.2 to 3.6V
Pressure Detector	Pressure detection circuit and self-diagnosis circuit. The pressure range can be selected depending on the EEPROM data for the pressure detector. • Pressure above a certain value is detected (determined by threshold). • Pressure below a certain value is detected (determined by inverted threshold). • Pressure above or below a certain value is detected (determined both by a threshold and an inverted threshold). The DET pin goes high when the detected pressure exceeds the threshold. The detection threshold value can be set by entering it via the PTH pin or using the EEPROM data in the AK8996. Note that upon powering up and exiting standby (STBYN pin from low to high) the precise pressure cannot be determined until the VOUT pin output settles, depending on the setup and external capacitance value of the VO pin. The self-diagnostic circuit ensures that the output (VOUT pin) produces a given value by fixing the VP and VN pins at half of VDD upon power-up, or only at initial operation immediately after exiting the standby mode. In the event of any anomalies, signals go high at the DET pin. To reset the self-diagnostic circuit, set the STBYN low or recycle the power. Bear in mind that the self-diagnostic circuit does not detect all of the failure modes of the AK8996.

Reference Section & Others

Block	Functions
V_Bandgap (VBG) V_Reference (VREF) I_Reference (IREF)	Generates the reference voltage or bias current required for each circuit. Adjust the VREF voltage so that it is equivalent to 1.0V. VREF voltage adj. Resolution: 3-bits Adj. step: 1% step Adjust the IREF current so that it is equivalent to 20μA. IREF current adj. Resolution: 4-bits Adj. step: 2.7% steps typically
Oscillator (OSC)	Oscillator to generate timing sync signals for internal operation and sampling frequencies for sensor output signals. Adjust the oscillating frequency to 1024kHz. OSC adj. Resolution: 4-bits Adj. step: 5% steps
V_temp. (VTMP)	Temperature sensor for converting the ambient temperature to voltage. Adjust the temperature sensor output voltage (VTMP voltage) so that it is equivalent to VREF voltage at 25ºC. VTMP voltage adj. Resolution: 6-bits Adj. step: 0.2% (0.67°C) steps
V_Common (VCOM)	Generates analog circuit reference voltage 1/2VDD. Connect 10nF capacitance to this pin for stabilization. Since the output cannot drive current, do not connect a resistive load. The internal power-up circuit causes it to start up within the settling time for stable analog operation (Start Up valid time).
Power ON Delay (PODLY)	Upon power-up or exit from standby mode (low to high at the STBYN pin), this circuit generates the settling time for stable analog operation using the internal Power Up circuit. This circuit oversees the startup time for VREF or IREF and disables the OSC to prevent improper operation. When the settling time for stable analog operation expires, the OSC is enabled. Start up the supply voltage within 200 μsec (0.8*VDD<). If power-up is not started within 200 μsec, the AK8996 may enter the test mode. Note that the AK8996 may not function properly in the test mode (For the description of the function, refer to the Functional Description **9) Note on the AK8996 Power-up**). When recycling the power with the VDD pin and STBYN pin interconnected, it should be monitored to ensure that the supply voltage is below 0.1*VDD to enable the power-on reset.
Serial I/F	Serial interface for accessing EEPROM.
EEPROM & Control Register	EEPROM and control register (volatile memory). Used to store compensation values and measurement modes and to set up the measurement modes for adjustment.

Pin Assignments and Functions

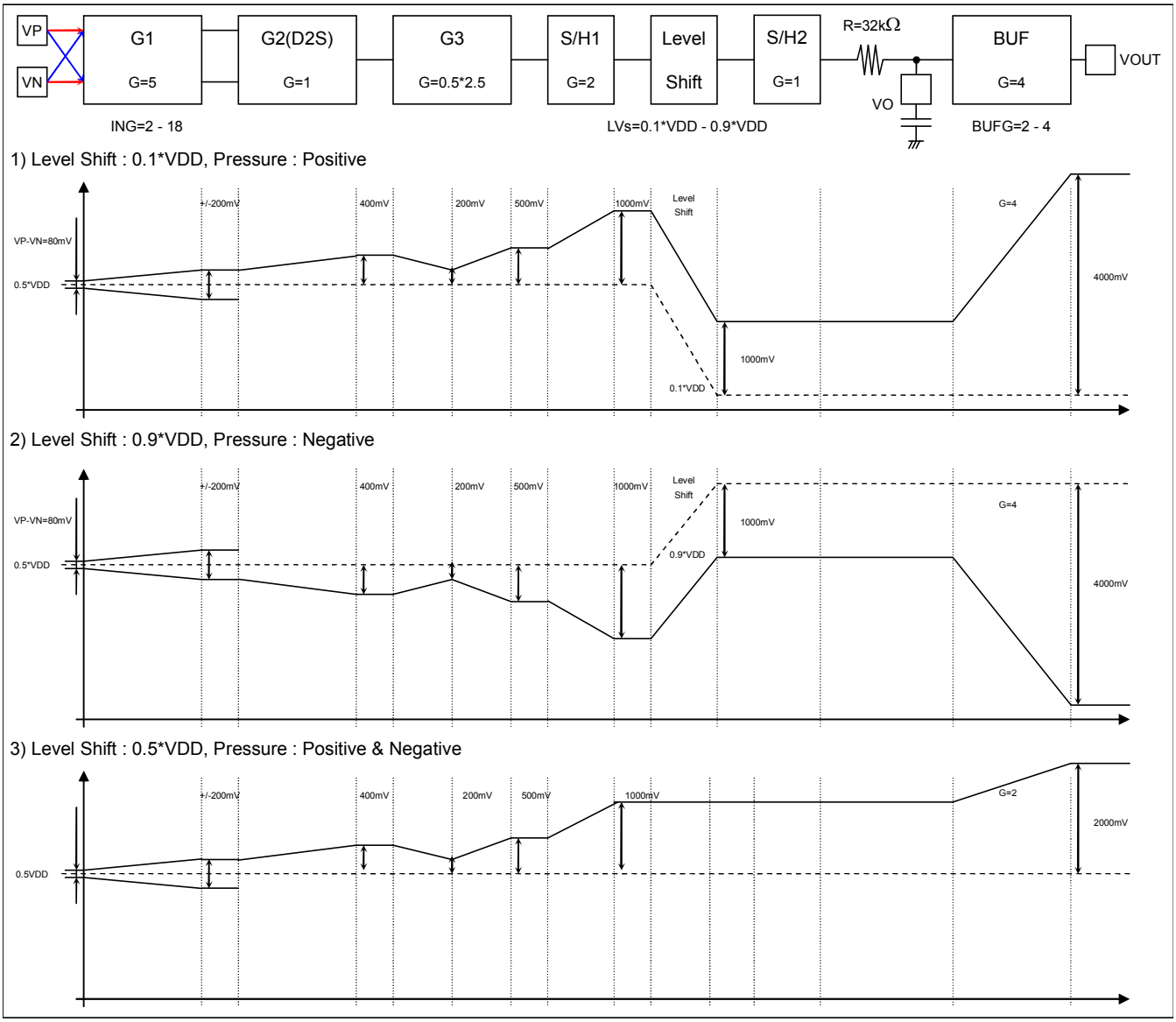
PAD	Name	I/O	C load max.	R load min.	Type	Comments
1	VSSO	O			GND	
2	VP	I			Analog	
3	VS	O	30pF	1kΩ	Analog	VDD > 2.7V
				3kΩ		VDD > 2.2V
4	VN	I			Analog	
5	STBYN	I			CMOS	Schmitt trigger input Connected to VDD when not in use.
6	CS	I			CMOS	Pull-down resistor (100kΩ) included
7	SCLK	I			CMOS	Pull-down resistor (100kΩ) included
8	SDI/O	I/O			CMOS	Pull-down resistor (100kΩ) included
9	DET	O			CMOS	
10	VSS				GND	
11	VDD				Power	
12	NC					Do not connect
13	VOUT	O	50pF	10kΩ	Analog	VDD > 2.7V
				20kΩ		VDD > 2.2V
14	VO	O	3μF		Analog	Due to the internal 32kΩ output resistor, resistive load connection is prohibited
15	PTH	I			Analog	
16	AGND	O			Analog	10nF connection; resistive load connection prohibited

Pin Descriptions

PAD	Name	Functions	Pin conditions			
			STBYN: "L"	DET: "H" EOUT[0]: "L"	DET: "H" EOUT[0]: "H"	Start up Note)
1	VSSO	Reference voltage output pin	-	-	-	-
2	VP	Sensor differential signal input pin (+ve)	Hi-Z			Hi-Z
3	VS	Constant voltage supply pin for sensor drive	Hi-Z			Hi-Z
4	VN	Sensor differential signal input pin (-ve)	Hi-Z			Hi-Z
5	STBYN	Standby pin ("L": Standby)	VSS	VDD	VDD	VDD
6	CS	Chip select pin	-	-	-	-
7	SCLK	Serial clock pin	-	-	-	-
8	SDI/O	Data I/O pin	-	-	-	-
9	DET	Output pin for pressure detection (high at detection) and output pin for abnormal self-diagnostic detection (high at detection)	VSS	VDD	VDD	VSS
10	VSS	Reference voltage pin	-	-	-	-
11	VDD	+ Power supply pin	-	-	-	-
12	NC		-	-	-	-
13	VOUT	Sensor signal pin	Hi-Z		Hi-Z	AGND
14	VO	Capacitance connection pin for sensor signal band-limiting	Hi-Z			AGND
15	PTH	Pin for pressure detection and self-diagnosis threshold input	-	-	-	-
16	AGND	Analog ground with external capacitance for stabilization	Hi-Z			AGND

Note) **See "Operation Sequence."**

Level Diagram



Electrical Characteristics

1) Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Units	Comments
Supply voltage	VDD	-0.3	6.5	V	
Input voltage	VDIN	VSS-0.3	VDD+0.3	V	
Input current	IIN	-10	10	mA	
Output current	IOUT	-10	10	mA	
Storage temp.	TST	-55	125	°C	EEPROM retention characteristics < 105ºC

Note) Operation at or beyond these limits may result in permanent damage to the device.

2) Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units	Comments
Operating temp.	Ta	-40		105	°C	
Supply voltage	VDD1	2.2	3.0	3.6	V	EVD[0]=1
	VDD2	4.5	5.0	5.5	V	EVD[0]=0

3) Supply Voltage Current (See Functional Description)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Min.	Typ. Note1)	Max.	Units	Comments
Supply voltage current 0 note)	IDD0			1	μA	At standby
Supply voltage current 1 note)	IDD1		350	450	μA	Sampling frequency: 100Hz
Supply voltage current 2 note)	IDD2		250	340	μA	Sampling frequency: 100Hz Buffer OFF (EBU[0]=1)
Supply voltage current 3 note)	IDD3		570	680	μA	Sampling frequency: 1kHz
Supply voltage current 4 note)	IDD4		820	980	μA	Sampling frequency: 2kHz
Supply voltage current 5 note)	IDD5		2550	2850	μA	Sampling frequency: 10.24kHz

Note) At the time of measurement, a 3kΩ resistor load is applied to the VS pin, no load is applied to the VO&VOUT pin, and AGND is applied to the VP&VN pin.

Note1) Supply voltage current when VDD = 5.0V (EVD[0]=0).

4) EEPROM Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Min.	Typ.	Max.	Units
EEPROM write voltage	Evdd	2.7			V
EEPROM write temp.	Eta	-40		85	°C
EEPROM endurance	Etime	1000			times
EEPROM data retention time	Ehold	10			years

5) Digital DC Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Units
High level input voltage	VIH	1, 2		0.7*VDD	-	-	V
Low level input voltage	VIL	1, 2		-	-	0.3*VDD	V
High level input current 1	IIH1	1		+10	-	+200	μA
High level input current 2	IIH2	2		-10	-	+10	μA
Low level input current	IIL	1, 2		-10	-	+10	μA
High level output voltage	VOH	3	IOH= -200μA	0.9*VDD	-	-	V
Low level output voltage	VOL	3	IOL= +200μA	-	-	0.1*VDD	V

1 SDI(/O), SCLK, CS (integrated 100kΩ pull-down resistor)
2 STBYN (Schmitt trigger)
3 SD(I/)O, DET

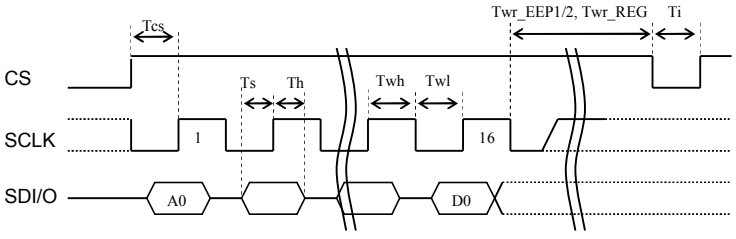
6) Digital AC Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

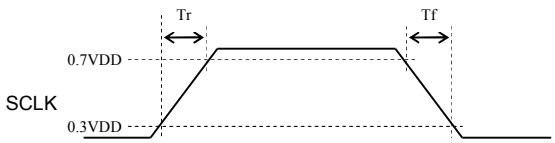
Item	Symbol	Min.	Typ.	Max.	Units
Write time (EEPROM address write)	Twr_EEP1	5		100	msec
Write time (EEPROM batch write)	Twr_EEP1	10		100	msec
Write time (register)	Twr_REG	300			nsec
CS setup time	Tcs	100			nsec
Data setup time	Ts	100			nsec
Data hold time	Th	100			nsec
SCLK high time	Twh	500			nsec
SCLK low time	Twl	500			nsec
SCLK → SDO delay time	Td			200	nsec
Idle time	Ti	100			nsec
SCLK rising time Note)	Tr			10	nsec
SCLK falling time Note)	Tf			10	nsec

Note) Design reference value; no production test performed.

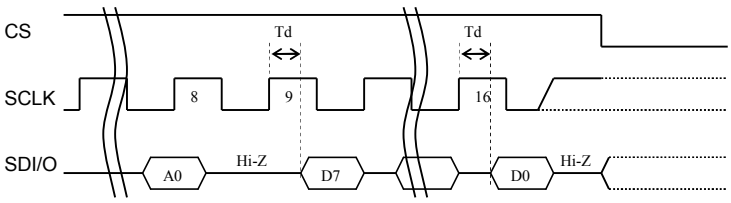
[Serial I/F timing (Write)]



[SCLK Raising/Falling timing]



[Serial I/F timing (Read)]

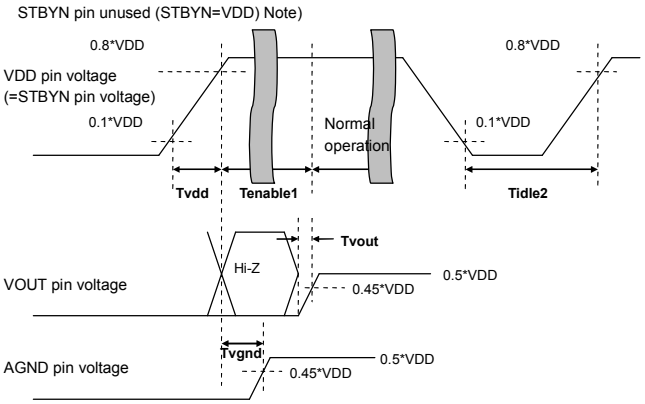


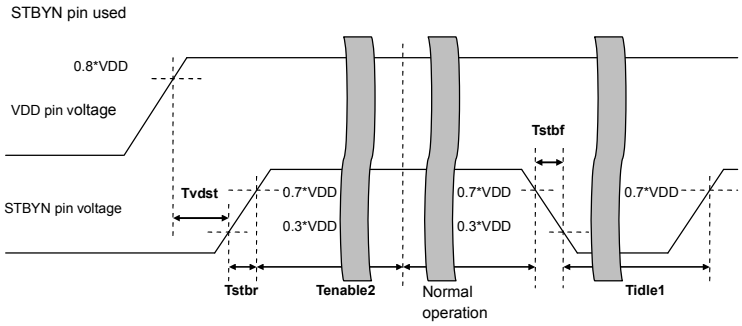
7) Power-Up and Standby Exit Time

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Min.	Typ.	Max.	Units	Comments
Power-up time	Tvdd			200	µsec	See Functional Description **9) Note on the AK8996 Power-up**
Standby exit time	Tvdst	10			nsec	
Standby rise time	Tstbr			10	nsec	
Standby fall time	Tstbf			10	nsec	
Standby valid time	Tidle1	1			msec	
	Tidle2	30			msec	VDD pin voltage<0.1*VDD
VOUT output rise time	Tvout			20	µsec	VO pin external capacitance<0.1µF
AGND output rise time	Tvgnd		150	250	µsec	AGND pin external capacitance: 10nF
Settling time for stable analog operation	Tenable1		280	465	µsec	
	Tenable2		350	495	µsec	

Note) Design reference value; no production test performed.



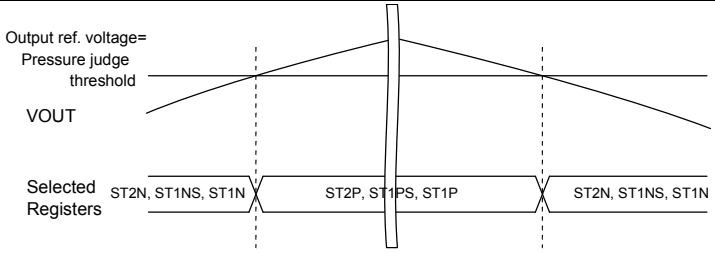


Note) When recycling the power with the VDD and STBYN pins connected, ensure that the supply voltage is below 0.1*VDD to enable the power on reset.

8) Pressure Determination Circuit (Pressure Judge)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

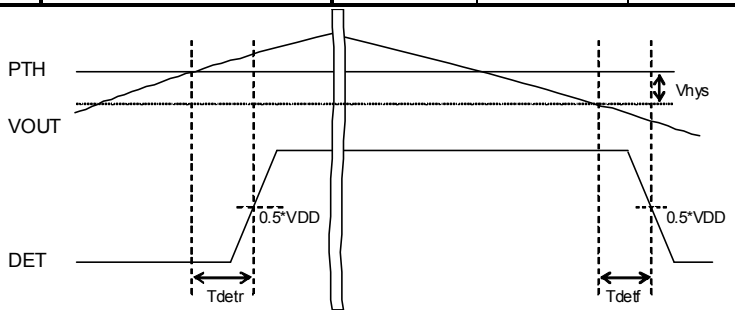
Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Pressure judge threshold	Vjudi	Unadjusted AM[3:0]:9h DET output	0.48*VDD	0.5*VDD	0.52*VDD	V	DET pin
Pressure judge threshold adjustment range	Vjud+	With respect to Vjudi Max: EPJLV[9:0]=23Eh		0.95*VDD		V	DET pin
	Vjud-	With respect to Vjudi Min: EPJLV[9:0]=1C2h		0.05*VDD		V	DET pin
Adj. Step	Vjstp			0.001 *VDD		V	DET pin



9) Pressure Detector

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Pressure detection threshold External input range	Vdeto5+	EINT1[1:0]=01 EINT2[0]=0 VDD=5V±5%	0.5*VDD		0.95*VDD	V	
	Vdeto3+	EINT1[1:0]=01 EINT2[0]=0 EVD[0]=1 VDD=2.2 - 3.6V	0.5*VDD		0.90*VDD		
Pressure detection threshold Internal set value	Vdeti	Unadjusted AM[3:0]:5h DET out EINT1[1:0]=01 EINT2[0]=1	0.72*VDD	0.74*VDD	0.76*VDD	V	
Pressure detection threshold Internal set value Adjust. width	Vdet5+	With respect to Vdeti Max: EPT[3:0]=7h VDD=V±5%		0.95*VDD		V	
	Vdet3+	EINT1[1:0]=01 EINT2[0]=0 EVD[0]=1 EPT[3:0]=6,7h prohibited VDD=2.2 - 3.6V		0.89*VDD			
	Vdet-	With respect to Vdeti Min: EPT[3:0]=8h		0.50*VDD		V	
Adjust. step	Vdstp			0.03*VDD		V	
Hysteresis voltage	Vhysi	Unadjusted AM[3:0]:7h DET out EINT1[1:0]=01	0.008 *VDD	0.020 *VDD	0.032 *VDD	V	
Hysteresis voltage Adjust. width	Vhys+	With respect to Vhysi Max: EHYS[2:0]=0h		0.0		V	
	Vhys-	With respect to Vhysi Min: EHYS[2:0]=7h		-0.0175 *VDD		V	
Adjust. step	Vhstp			-0.0025 *VDD		V	
Pressure detection time	Tdetr	EINT1[1:0]=01		450	600	µsec	
Pressure non-detection time	Tdetf	EINT1[1:0]=01		450	600	µsec	
Pressure detector Disable time Adjust. width	Tasdis+	EAS[2:0]=7h ESF[1:0]=3h EINT1[1:0]=01		12.5		msec	
		0.1		msec			



10) Self-Diagnostic Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Self-diagnostic normal operation judgment range	Vself	EINT1[1:0]=10	0.48*VDD -0.1		0.52*VDD +0.1	V	
Self-diagnostic detection time	Tself	EINT1[1:0]=10		450	600	µsec	

11) Analog Characteristics

11-1) Reference Section

11-1-1) Reference Section Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
VREF voltage	Vr0	Unadjusted AM[3:0]:1h DET out	0.97	1.0	1.04	V	
VREF adj. width	Vr+	With respect to Vr0 Max: EVR[2:0]=3h		+30		mV	
	Vr-	With respect to Vr0 Min: EVR[2:0]=4h		-40		mV	
VREF adj. step	Vrstp			10		mV	
VS voltage	VS51	After VREF adj. VS pin out Load resistance: 3kΩ	3.88	4.00	4.12	V	
	VS52	Load resistance: 1kΩ	3.88	4.00	4.12		VDD>2.7V
	VS31	After VREF adj. VS pin out Load resistance: 3kΩ	1.94	2.00	2.06	V	
	VS32	Load resistance: 1kΩ	1.94	2.00	2.06		VDD>2.7V
IREF current	Ir0	Unadjusted AM[3:0]:2h DET out	16.15	20	24.98	µA	
IREF adj. width	Ir+	With respect to Ir0 Max: EIR[3:0]=7h		+4.81		µA	
	Ir-	With respect to Ir0 Min: EIR[3:0]=8h		-3.40		µA	
IREF adj. step	Irstp			0.547		µA	
OSC freq.	Fr0	Unadjusted AM[3:0]:3h DET out	768	1024	1288	kHz	
OSC adj. width	Fr+	With respect to Fr0 Max: EFR[3:0]=4h		204.8		kHz	
	Fr-	With respect to Fr0 Min: EFR[3:0]=Ch		-204.8		kHz	
OSC adj. step	Frstp			51.2		kHz	

11-1-1) Reference Section Characteristics (Continued)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
VTMP voltage	Vt0	Unadj. (Temp = 25°C) AM[3:0]:4h DET out	0.936	1.0	1.062	V	
VTMP adj. width	Vt0+	With respect to Vt0 Max: ETM[5:0]=1Fh		+62		mV	
	Vt0-	With respect to Vt0 Min: ETM[5:0]=20h		-64		mV	
VTMP adj. step	Vt0stp			2.0		mV	
VTMP temp variation	Vt	Temp = -40 to 105°C		3.0		mV/°C	Note)
AGND voltage	Vag		0.5*VDD -0.06	0.5*VDD	0.5*VDD +0.06	V	

Note) Design reference value; no production test performed.

11-1-2) Reference Section (packaged version only) Characteristics (note)

Unless otherwise specified, VDD = 4.5 to 5.5V, Temperature = -40 to 105ºC

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
VREF voltage	Vr0P	AM[3:0]:1h DET out	0.99	1.0	1.01	V	After adj.
VS voltage	VS51P	Load resistance: 3kΩ	3.88	4.00	4.12	V	After adj.
	VS52P	Load resistance: 1kΩ	3.88	4.00	4.12		After adj.
IREF current	Ir0P	AM[3:0]:2h DET out	18	20	22	µA	After adj.
OSC freq.	Fr0P	AM[3:0]:3h DET out	921.6	1024	1126.4	kHz	After adj.
VTMP voltage	Vt0P	AM[3:0]:4h DET out	0.994	1.0	1.006	V	After adj. @25°C

Note) Factory default adjustment is referenced to 5V mode (EVD[0]=0). If 3V mode (EVD[0]=1) is used, readjustment is required

11-2) Gain Amplifier and Other Blocks

Unless otherwise specified, the following requirements apply.

- Reference Section is complete with adjustment.
- For supply voltage of 5V (3V), the level diagram includes G1 gain of 5x, Level shift 0.1*VDD and BUFF gain of 4x (see level diagram 1) and the output voltage 4000mV (2000mV) is set as 100% based on a differential input of 80mV (40mV).

11-2-1) Overall Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Std. gain	Gtyp	VP/VN → VOUT		50		times	
Input common voltage	Vicom		0.45VS	0.5*VS	0.55VS	V	
Output common voltage	Vcom0	VP/VN → VOUT VP=VN=0.5*VS		0.1*VDD		V	
Max. output range	Vmax+	VP/VN → VOUT	0.9*VDD			V	
	Vmax-	VP-VN=VSS or VDD			0.1*VDD	V	
Non-input noise	Nout	VP/VN → VOUT VP=VN=Open VO external capacitance: 10nF			1,000	µVrms	@1Hz - 100kHz Note)

Note) Value for 50x nominal gain. Design reference value; no production test performed.

11-2-2) G1/2 Gain Adjustment Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode							
Unadjusted G1/2 output voltage	Vg10	VP-VN=80mV VDD=5V±5% EIG[2:0]=0h, EIG[3]=0	145	160	175	mV	
	Vg02	VP-VN=40mV VDD=2.2 - 3.6V EIG[2:0]=0h, EIG[3]=0 EVD[0]=1	73.0	80	87.0	mV	
G1 adjustment range	G1sc+	EIG[2:0]=7h		9		times	
	G1sc-	EIG[2:0]=0h		2		times	
Adj. step	G1sc stp			1		times	
G2 adj.	G2sc+	EIG[3]=1		2		times	
	G2sc-	EIG[3]=0		1		times	

11-2-3) Offset Voltage Adjustment Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode							
Unadjusted output voltage	Vo01	VDD=5V±5%	0.5*VDD –30	0.5*VDD	0.5*VDD +30	mV	
	Vo02	VDD=2.2-3.6V EVD[0]=1	0.5*VDD –15	0.5*VDD	0.5*VDD +15	mV	
Offset rough adj. DAC adj. range	Ocmp+	EOC[10]=0h EOC[9:7]=7h		+52.5		%	
	Ocmn+	EOC[10]=1h EOC[9:7]=7h		-52.5		%	
Adj. step	Ocm stp			7.5		%	
Offset fine adj. DAC adj. range	Ocl+	EOC[10]=0h EOC[6:0]=3Fh		+7.875		%	
	Ocl-	EOC[10]=1h EOC[6:0]=3Fh		-7.875		%	
Adj. step	Ocl stp			0.125		%	

11-2-4) Span Voltage Adjustment Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage adjustment							
Unadjusted Span voltage	Vs01	VP-VN=80 mV@5V	480	500	520	mV	
	Vs02	VP-VN=40 mV@3V EVD[0]=1	240	250	260	mV	
Span adj. range	Sc+	ESC[8:0]=0FFh		100/36.25		times	
	Sc-	ESC[8:0]=100h		100/164		times	
Adj. Step	Sc stp	N=-256 - +255		100/(100+0.25*N)		times	

11-2-5) Offset Temperature Drift & Sensitivity Temperature Drift Adjustment Circuit

11-2-5-1) Quadratic Function Generator (a*Temp^2+b*Temp+c)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
2nd order coeff. a Adj. range 1	A2nd5+	VDD=5V±5%		+0.0016			
	A2nd5-			-0.0016			
Adj. step 1	A2nd5 stp			1.260E-5			
2nd order coeff. a Adj. range 2	A2nd3+	VDD=2.2 - 3.6V		+0.0008			
	A2nd3-			-0.0008			
Adj. step 2	A2nd3 stp			0.630E-5			

Note) Design reference value; no production test performed.

11-2-5-2) Offset Linear Function Generator (d*Temp+e)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. d Adj. range 1	D2ndO5+	VDD=5V±5%		+0.60			
	D2ndO5-			-0.60			
Adj. step 1	D2ndO5 stp			0.0012			
1st order coeff. d Adj. range 2	D2ndO3+	VDD=2.2 - 3.6V		+0.30			
	D2ndO3-			-0.30			
Adj. step 2	D2ndO3 stp			0.00060			

Note) Design reference value; no production test performed.

11-2-5-3) Sensitivity Linear Function Generator (d*Temp+e)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. d Adj. range 1	D2ndS5+	VDD=5V±5%		+0.32			
	D2ndS5-			-0.32			
Adj. step 1	D2ndS5 stp			0.000626			
1st order coeff. d Adj. range 2	D2ndS3+	VDD=2.2 - 3.6V		+0.30			
	D2ndS3-			-0.30			
Adj. step 2	D2ndS3 stp			0.00060			

Note) Design reference value; no production test performed.

11-2-6) Supply Voltage & Temperature Sensitivity Variation Adjustment Circuit (ST & SV)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Sensitivity variation characteristics to supply voltage	SV1	Unadjusted SV circuit initial operation			5.0	%	With respect to target value
	SV2	SV circuit 2nd operation		±0.25		%	With respect to SV1
Sensitivity variation characteristics to operating temperature	ST1	Unadjusted ST initial operation			5.0	%	With respect to target value
	ST2	ST circuit 2nd operation		±0.25		%	With respect to ST1

11-2-7) LPF, S/H1&2, & Buffer

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
LPF freq. response	Fc1		40	60	80	kHz	
S/H1&2 gain	SHG		1.935	2	2.065	times	
S/H1&2 out pre-adj. error	SHerr		-20	0	20	mV	
S/H2 output resistance post-adj. error	Rout		24.6	32	39.4	kΩ	
BUF gain adj. width	Bufg+	EOG[2:0]=4h		4		times	
	Bufg-	EOG[2:0]=0h		2		times	
Adj. step	Bufgstp			0.5		times	10kΩ
BUF output (VOUT) drive characteristics	Rbuf1+	Load resistance: 20 kΩ	0.9*VDD			V	
	Rbuf1-				0.1*VDD	V	
	Rbuf2+	Load resistance: 10 kΩ	0.9*VDD			V	VDD>2.7V
	Rbuf2-				0.1*VDD	V	VDD>2.7V

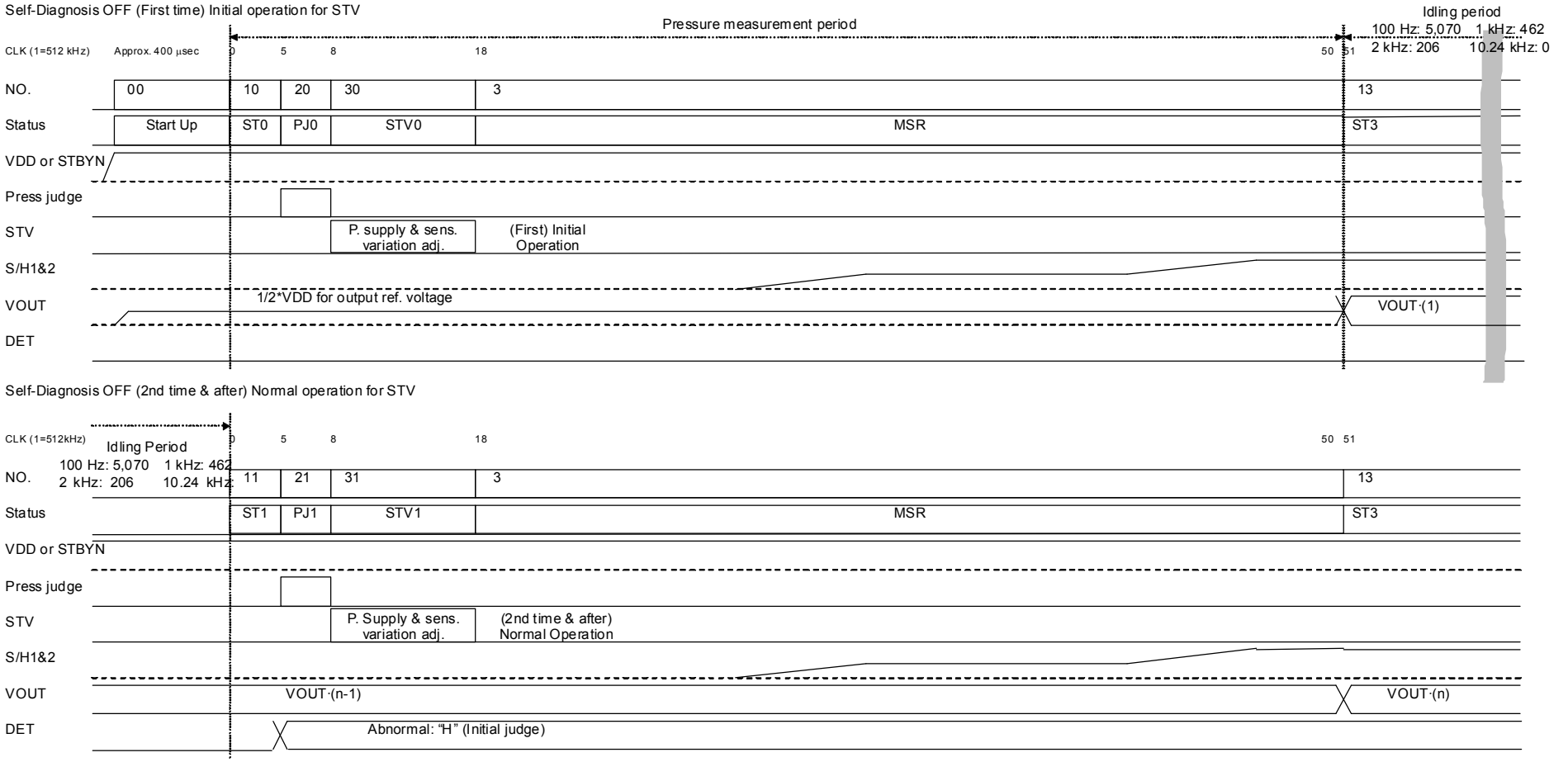
11-2-8) Level shift

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Output reference voltage Rough adj. width (Level shift)	Vlv0	Unadjusted AM[3:0]:9h VS input → VO out	0.5*VDD –0.02	0.5*VDD	0.5*VDD +0.02	V	VO pin
	Vlvr+	Vlv0 reference Max: ELV[10:6]=1Fh		0.890 *VDD		V	VO pin
	Vlvr-	Vlvo reference Min: ELV[10:6]=0Fh		0.110 *VDD		V	VO pin
	Vlrstp			0.026 *VDD		V	VO pin
Output reference voltage Fine adj. width (Level shift)	Vlvf+	Vlv0 reference Max: ELV[10]=1h, ELV[5:0]=3Fh		0.0315 *VDD		V	VO pin
	Vlvf-	Vlv0 reference Min: ELV[10]=0h, ELV[5:0]=3Fh		-0.0315 *VDD		V	VO pin
	Vlfstp			0.0005 *VDD		V	VO pin

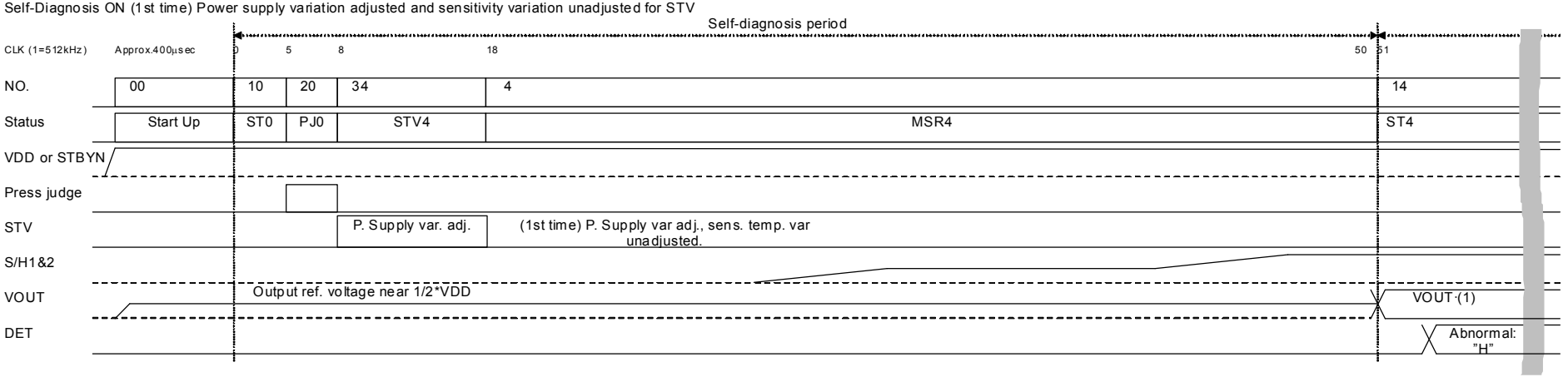
Operation Sequence

1. Normal Operation Timing (Pressure Detector Valid)

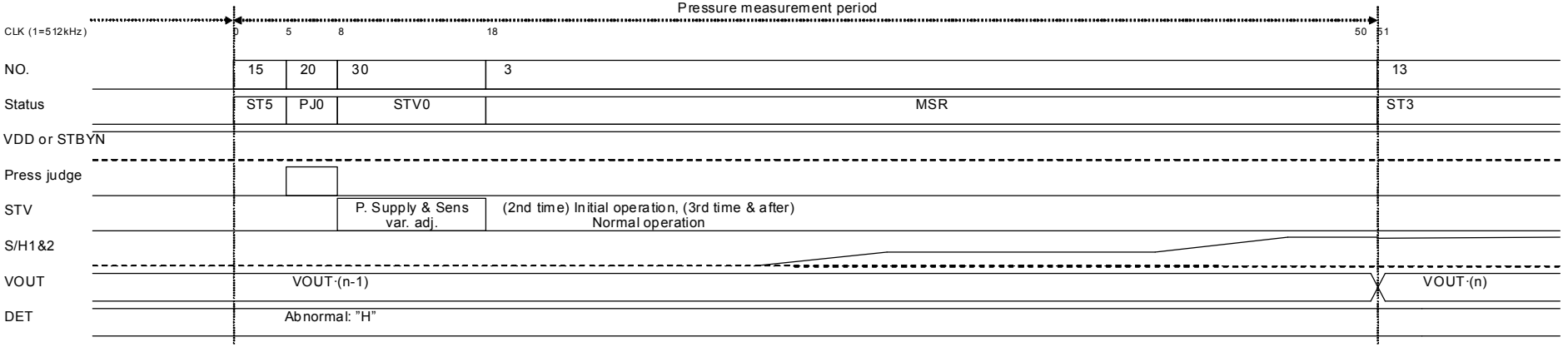


2. Operation Timing when the Self-Diagnosis Circuit is Valid (Pressure Detector Valid)

Self-Diagnosis ON (1st time) Power supply variation adjusted and sensitivity variation unadjusted for STV



Self-Diagnosis ON (2nd time) Initial operation for STV



3. Description of Operation Timing Status

3.1 Normal Operation Timing

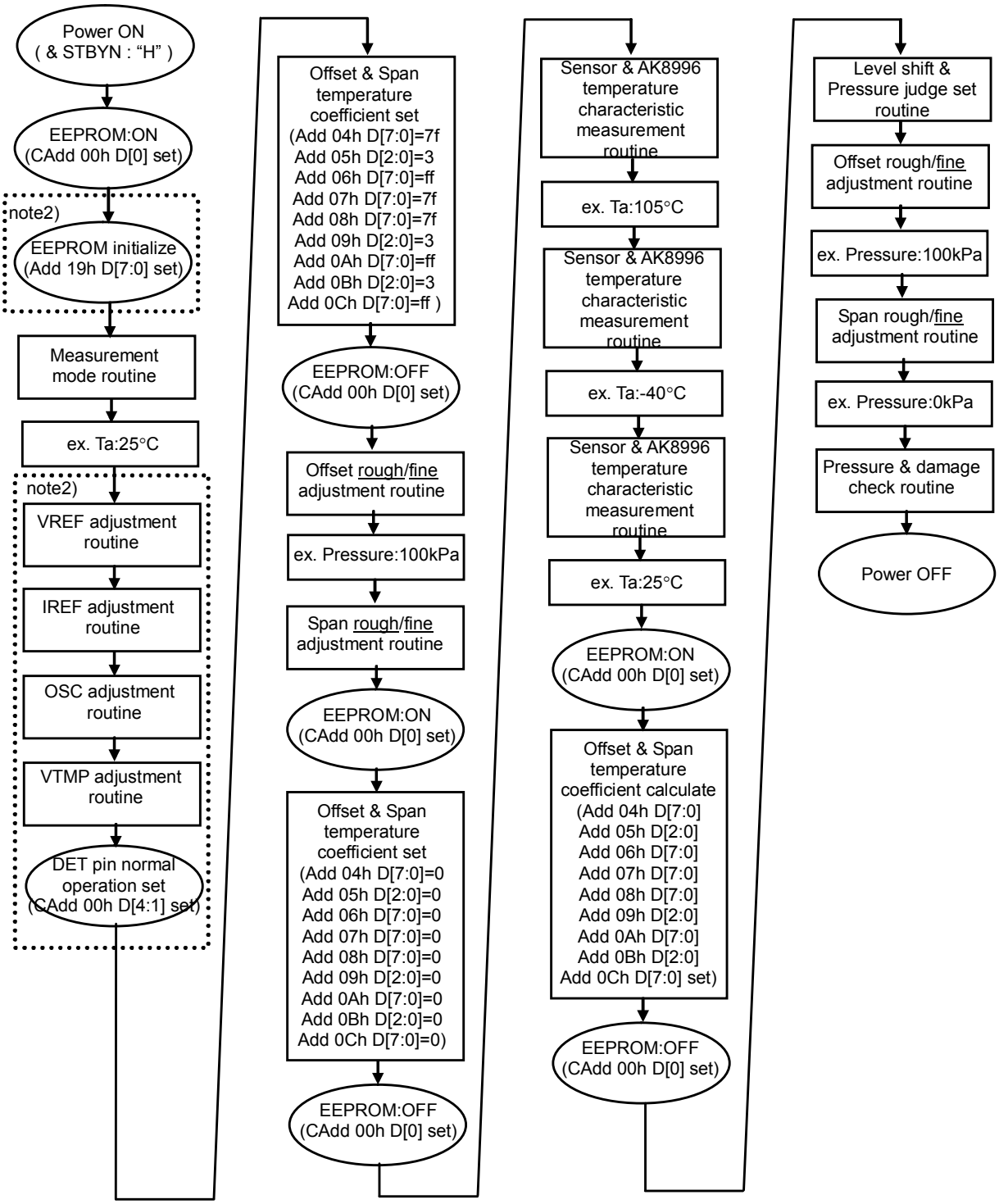
No.	State	CLK	Operations
00	Start Up		Analog circuit settling time for stable operation. Analog reference circuits as VREF & IREF start up and configured output reference voltage is provided at VOUT pin.
10	ST0		Clock count start Analog circuit startup
20	PJ0	CLK=5	Pressure judge circuit not in operation
30	STV0	CLK=8	STV initial operation
3	MSR	CLK=18	Output pressure (VP-VN) to VOUT
13	ST3	CLK=51	Idling With fs=10.24kHz setup, no idling and in continuous operation. Idling period 100Hz 5,070 CLK 1kHz 482 CLK 2kHz 206 CLK 10.24kHz 0 CLK
11	ST1	CLK1=51 or 256 or 512 or 5120	Pressure detection operation and analog circuit startup
21	PJ1	CLK=5+CLK1	Pressure judge circuit operation (Positive/negative pressure determination)
31	STV1	CLK=8+CLK1	STV normal operation
:	:	:	:

3.2 Self-Diagnostic Circuit in Operation

No.	State	Trigger	Operations
00	Start Up		Analog circuit settling time for stable operation. Analog reference circuits VREF & IREF start up and configured output reference voltage is provided at VOUT pin.
10	ST0		Clock count start Analog circuit startup
20	PJ0	CLK=5	Pressure judge circuit not in operation
34	STV4	CLK=8	SV initial operation (ST not in operation)
4	MSR4	CLK=18	VP&VN pin fixed to 1/2*VS; given value output to VOUT
14	ST4	CLK=51	Self-diagnostic circuit operation & idling Back to normal operation on completing self-diagnosis in 50 CLK.
15	ST5	CLK=100	Analog circuit startup
20	PJ0	CLK=105	Pressure judge circuit not in operation
30	STV0	CLK=108	STV initial operation
3	MSR	CLK=118	Output pressure (VP-VN=0V) to VOUT
:	:	:	:(Same as operation after ST3 in 3.1 Normal Operation Timing)

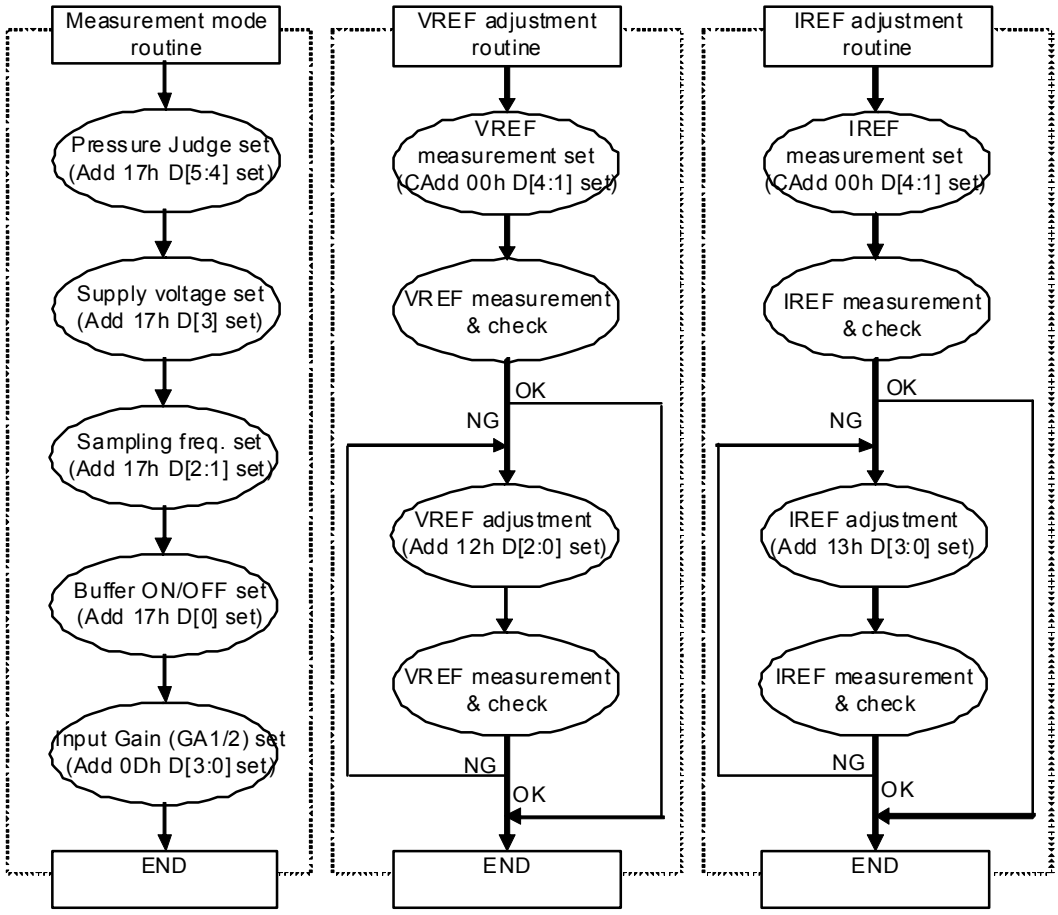
Adjustment Sequence

■ Main Routine



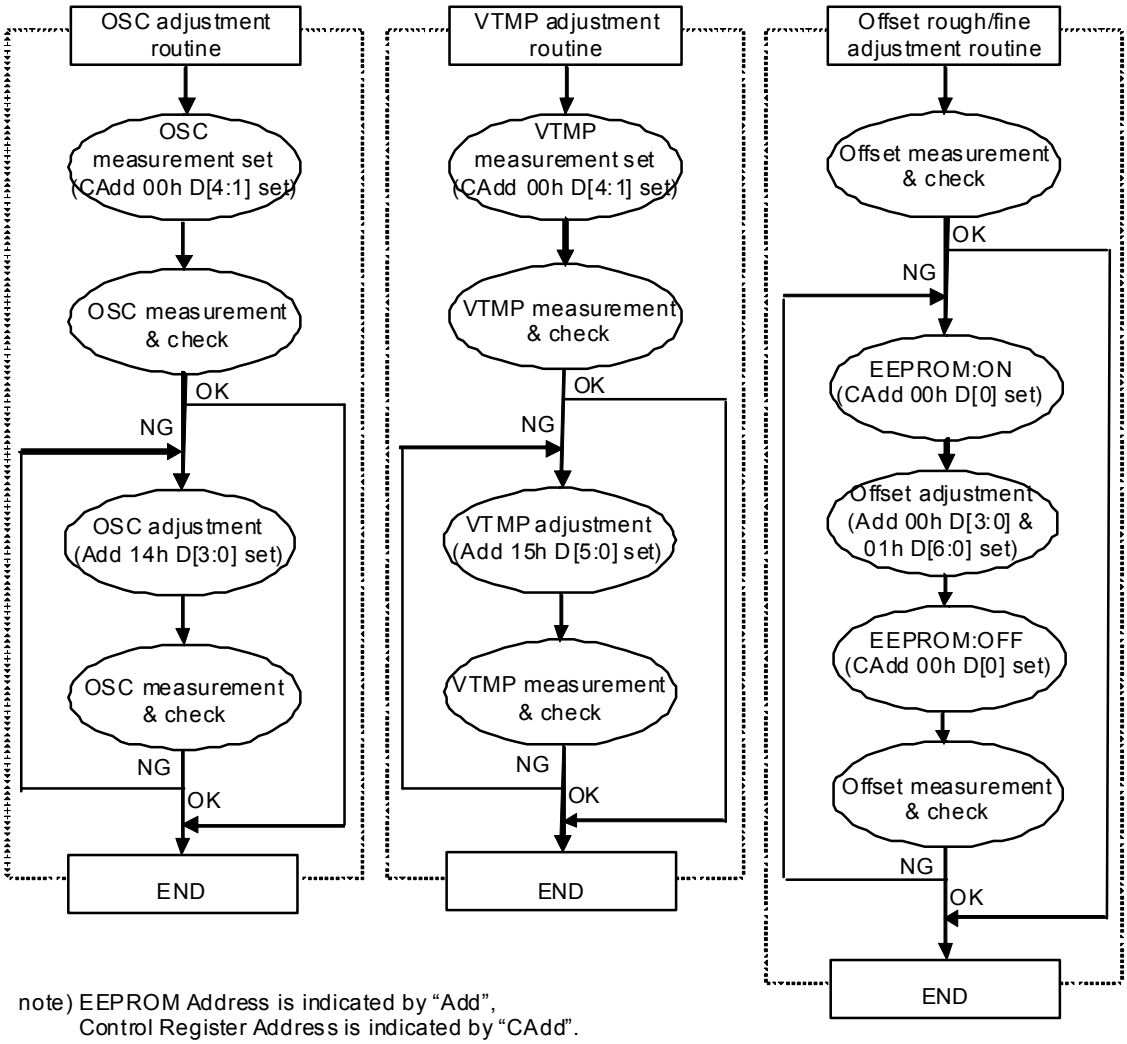
note) EEPROM Address is indicated by "Add",
Control Register Address is indicated by "CAdd".
note2) In case of Package, each items are unused.

■ Sub Routine



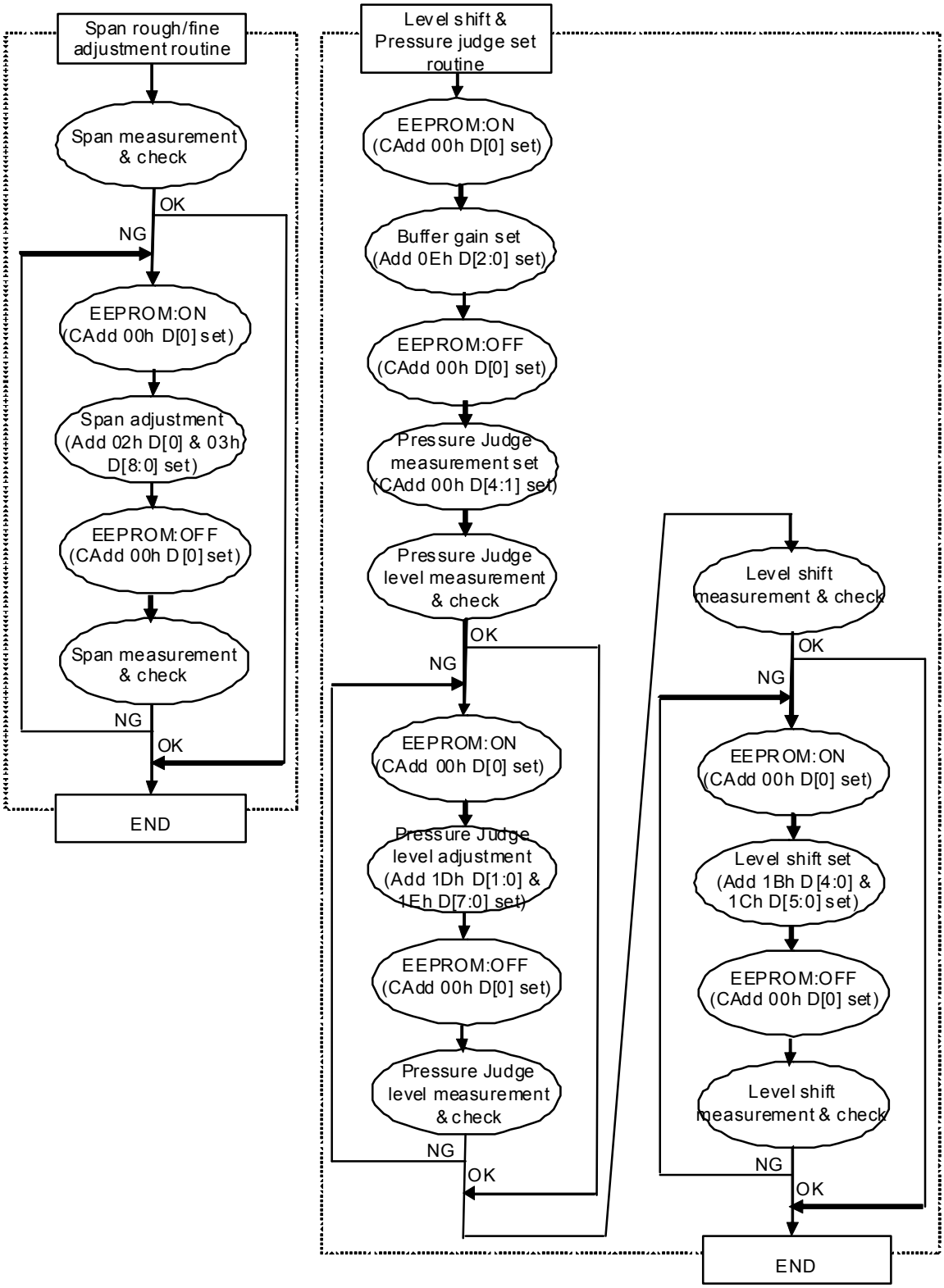
note) EEPROM Address is indicated by "Add",
Control Register Address is indicated by "CAdd".

■ Sub Routine



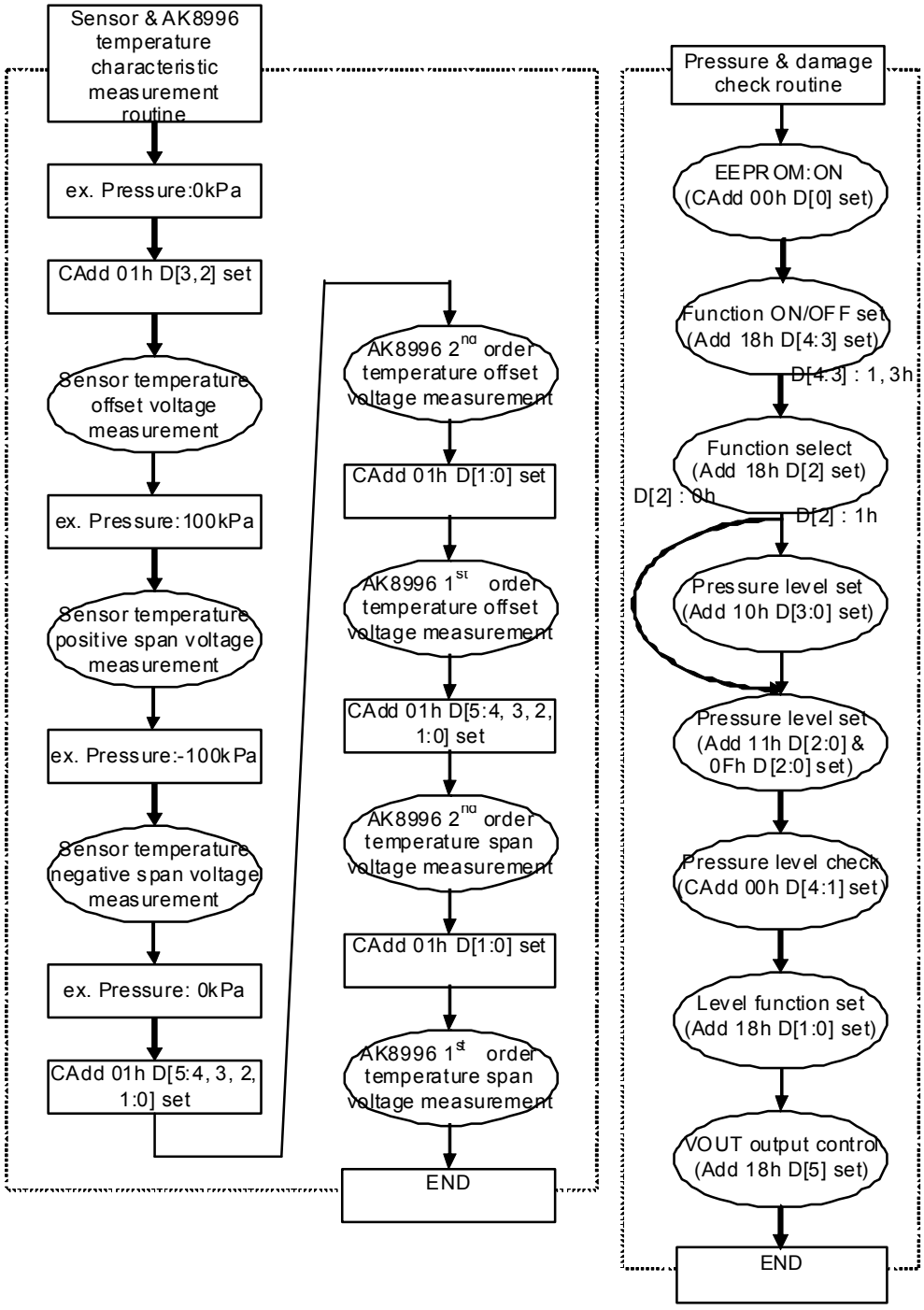
note) EEPROM Address is indicated by "Add",
Control Register Address is indicated by "CAdd".

■ Sub Routine



note) EEPROM Address is indicated by “Add”,
Control Register Address is indicated by “CAdd”.

■ Sub Routine



note) EEPROM Address is indicated by “Add”,
Control Register Address is indicated by “CAdd”.

Functional Description

1) Adjustment Procedure Description (Example)

The adjustment procedure for the AK8996 follows (See "**Adjustment Sequence**.").

Note) When shipped in package form, the adjustments for the items 1-4 below have been completed. It is necessary to read the data (items 1-4 below) from a chip first and after initializing the EEPROM, rewrite the readout data. Note that depending on the required accuracy and implementation status, there could be some cases where items 1-4 should be readjusted. The factory default adjustment is with reference to 5V mode (EVD[0]=0).If 3V mode (EVD[0]=1) is used, readjustment is required. The EEPROM register address is referred to as "address," while the control register (volatile memory) address is referred to as "C address."

1. VREF Adjustment (completed when shipped in package form)

The reference voltage is adjusted to 1.0V. Adjusting the VREF voltage also means adjustment of the sensor drive voltage (VS).
Configuring the adjustment mode 1 register (C address: 00h data AM[3:0]:1h) allows the VREF voltage to be output at the DET pin (See recommended connection examples for components).

2. IREF Adjustment (completed when shipped in package form)

The reference current is adjusted to 20.0μA.
Configuring the adjustment mode 1 register (C address: 00h data AM[3:0]:2h) allows the IREF voltage to be output at the DET pin (See recommended connection examples for components).

3. OSC Adjustment (completed when shipped in package form)

The intermittent operation control clock is adjusted to 1024kHz.
Configuring the adjustment mode 1 register (C address: 00h data AM[3:0]:3h) allows the OSC output to be output at the DET pin (See recommended connection examples for components).

4. VTMP Adjustment (completed when shipped in package form)

Temperature sensor output (VTMP) voltage is adjusted to match the VREF voltage.
Configuring the adjustment mode 1 register (C address: 00h data AM[3:0]:4h) allows the VTMP voltage to be output at the DET pin (See recommended connection examples for components).
Since a quadratic function generator is used to compensate for the sensor characteristics, the VTMP output should be matched with the VREF voltage.

5. Offset Voltage Adjustment

The offset voltage for the pressure sensor is adjusted, including the AK8996 internal error.
The offset voltage is adjusted using the offset voltage rough adjustment register (Address: 00h data EOC[10:7]) and offset voltage fine adjustment register (Address: 01h data EOC[6:0]).
Since the offset voltage temperature drift is to be compensated for afterwards, the complete adjustment cannot be performed. Final readjustment is required including the level shift voltage error (See Section 11).

■ Offset Voltage Adjustment Example

EOC[10]: Offset voltage rough adjustment sign bit
If unadjusted output is more than 0.5*VDD, set EOC[10]=0.
If unadjusted output is less than 0.5*VDD, set EOC[10]=1.
EOC[9:7]: Offset voltage rough adjustment: Adjust in 300mV steps (@VDD: 5V).
When EOC[10] = 0, adjust within -150 to +150mV (0.5*VDD reference).
When EOC[10] = 1, adjust within -150 to +150mV (0.5*VDD reference).
EOC[6]: Offset voltage fine adjustment sign bit
If unadjusted output is more than 0.5*VDD, set EOC[6]=0.
If unadjusted output is less than 0.5*VDD, set EOC[6]=1.
EOC[5:0]: Offset voltage fine adjustment: Adjust in 5mV steps (@VDD: 5V). For example,
When EOC[6] = 0 and the rough adjustment result is -150mV, set 30 dec = 1E hex.
When EOC[6] = 1 and the rough adjustment result is +150mV, set 30 dec = 1E hex.

Fine-tune the offset to within ±2.5mV (@VDD: 5V).

6. Output Span Voltage Adjustment

The output span voltage for the connected pressure sensor is adjusted, including the AK8996 inherent error.
The output span voltage is adjusted using the output span voltage adjustment register (Address: 02h data ESC[8], address: 03h data ESC[7:0]).
Since the sensitivity temperature drift is to be compensated for afterwards, the complete adjustment cannot be performed. Final readjustment is required, including the level shift voltage error (See Section 12).

■ Output Span Voltage Adjustment Example

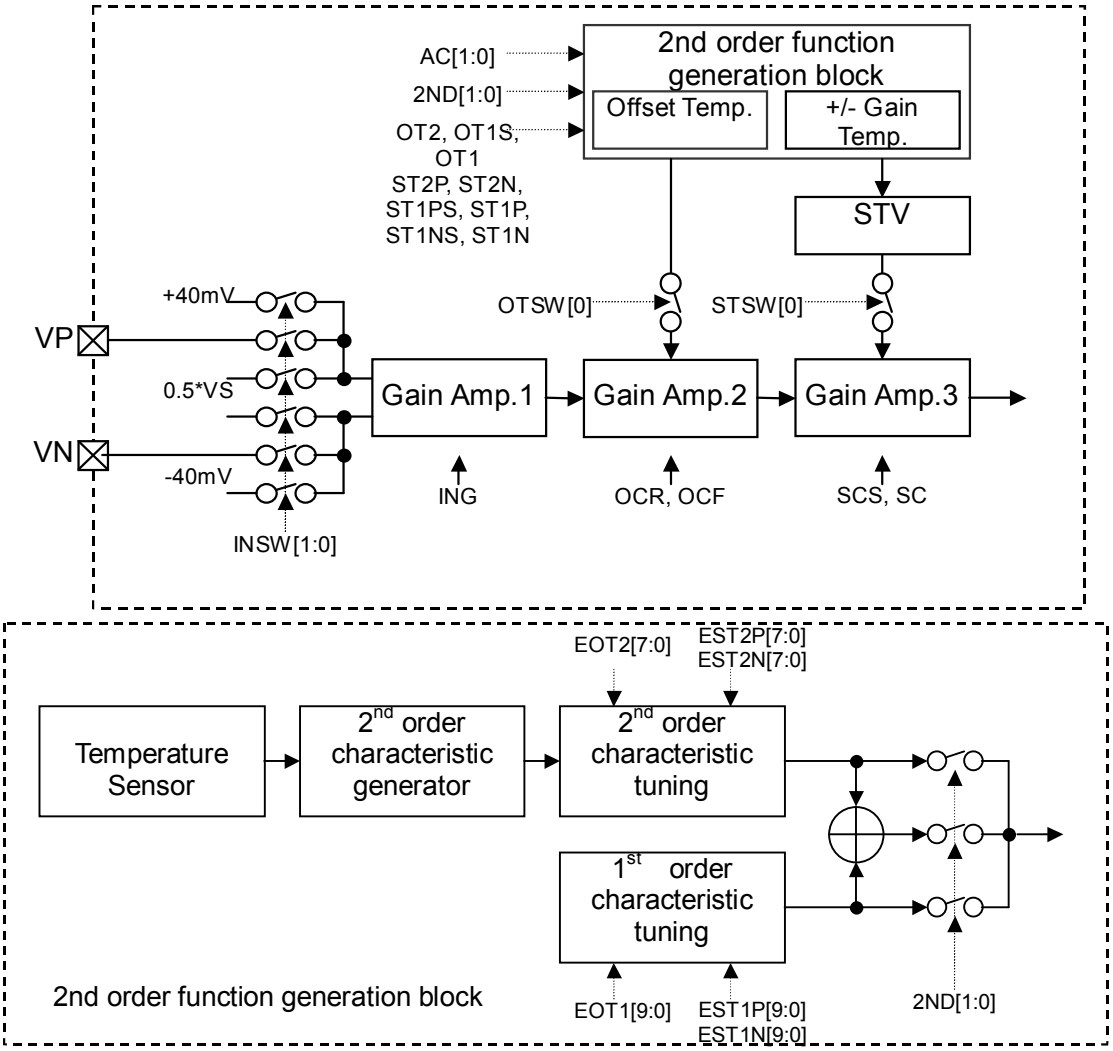
When the output is 2400mV (@VDD: 5V), set ESC[8:0] = 160 dec.
2400 [mV]*100/60 = 4000 [mV]
When the output is 5600mV (@VDD: 5V), set ESC[8:0] = -160 dec.
5600 [mV]*100/140 = 4000 [mV]

Fine-tune the above output span voltage error so that it is within ±5mV (@VDD: 5V).

7. Secondary Characteristics Adjustment for Pressure Sensor & AK8996 Offset and Sensitivity Temperature

Specific procedures for adjusting the pressure sensor's temperature drift (secondary characteristics) follow the sequence illustrated on this page.

Note) For enhanced adjustment accuracy, make an adjustment for both maximum operation temperature and minimum operation temperature.



Secondary temperature characteristics for pressure sensor offset and sensitivity as shown in this equation can be cancelled out with the AK8996's corresponding characteristics.

Secondary temperature characteristics for pressure sensor offset and sensitivity Vsen (T):

Vsen (T) = αT^2+βT+γ

Secondary temperature characteristics for AK8996 offset and sensitivity Vic (T):

Vic = [(g*a)T^2+(g*b)T+(g*c)]+[dT+e]=(g*a)T^2+(g*b+d)T+(g*c+e)

Quadratic function Linear function

In order to cancel the secondary temperature characteristics, the following measurements should be conducted for at least three different temperatures (e.g., 25ºC, -40ºC, +105ºC).

7.1 Pressure Sensor Offset Temperature Drift Measurement

Configure adjustment mode 2 register (C address: 01h data INSW[1:0]:0h, data OTSW[0]:1h, data STSW[0]:1h).
Measure the VOUT pin voltage at a pressure of 0kPa.

7.2 Pressure Sensor Sensitivity Temperature Drift Measurement

Configure adjustment mode 2 register (C address: 01h data INSW[1:0]:0h, data OTSW[0]:1h, data STSW[0]:1h).
Measure the VOUT pin voltage (Vp72) at pressure e.g., +100kPa.
As necessary, measure the VOUT pin voltage at pressure e.g., -100kPa.

7.3 AK8996 Offset Secondary Temperature Characteristics Measurement (g*aT^2+g*bT+g*c)

Configure adjustment mode 2 register (C address: 01h data INSW[1:0]:1h, data OTSW[0]:0h, data STSW[0]:1h, 2ND[1:0]:1h).
Measure the VOUT pin voltage.

7.4 AK8996 Offset Primary Temperature Characteristics Measurement (dT + e)

Configure adjustment mode 2 register (C address: 01h data INSW[1:0]:1h, data OTSW[0]:0h, data STSW[0]:1h, 2ND[1:0]:2h).
Measure the VOUT pin voltage.

7.5 AK8996 Sensitivity Secondary Temperature Characteristics Measurement (g*aT^2+g*bT+g*c)

Configure adjustment mode 2 register (C address: 01h data INSW[1:0]:2h, data OTSW[0]:1h, data STSW[0]:0h, 2ND[1:0]:1h).
Measure the VOUT pin voltage.

7.6 AK8996 Sensitivity Primary Temperature Characteristics Measurement (dT + e)

Configure adjustment mode 2 register (C address: 01h data INSW[1:0]:2h, data OTSW[0]:1h, data STSW[0]:0h, 2ND[1:0]:2h).
Measure the VOUT pin voltage.

8. Calculating the Secondary Characteristics from the Section 7 Measurement Results

Calculate α off, β off and γ off values from the pressure sensor offset temperature measurement results.
Calculate α ga, β ga, and γ ga values from the pressure sensor sensitivity temperature measurement results.
Values for g*a, g*b+d and g*c+e are known from the AK8996 temperature drift measurement results.
Zero order coefficient γ and g*c + e are already adjusted in Sections 5 and 6, so no further adjustment is required here.

For offset and sensitivity,
Make an adjustment to achieve α = g*a.
Make an adjustment to achieve β = g*b + d.

Explanations for "Calculating Sensitivity Temperature Characteristics 2nd Order Coefficients", "Offset Temperature Secondary Characteristics Calculation Example" and "Sensitivity Temperature Secondary Characteristics Calculation Example." are described in the following section.

■ Calculating Sensitivity Temperature Characteristics 2nd Order Coefficients

The difference between the values measured at the VOUT pin for three temperature points and the reference values at the reference voltage (Vbase = 0.8 V) is calculated to obtain the following coefficients for the sensitivity:

Sensor: α ga, β ga, γ ga

AK8996: a, b, c (quadratic function output), d, e (linear function output)

For example, assume:

Sensitivity temperature drift measurement result for a sensor alone:

Vsenc (25ºC), Vsenn (low temp), Vsenp (high temp)

Sensitivity temperature drift measurement result for AK8996:

Vicc2 (25ºC), Vicn2 (low temp), Vicp2 (high temp) quadratic function

Vicc1 (25ºC), Vicn1 (low temp), Vicp1 (high temp) linear function

Note) These values are for the span from which the offset voltages are subtracted for each temperature.

1) The gain values (gc, gn, gp) for compensating the sensitivity temperature drift are obtained from the sensitivity temperature drift results of a sensor alone:

gc=Vsenc/Vsenc=1, gn=Vsenc/Vsenn, gp=Vsenc/Vsenp

For the gain values (gc, gn, gp) obtained, find the voltage that should be output from the AK8996 quadratic function generator.

Vsenc1=Vbase/gc, Vsenn1=Vbase/gn, Vsenp1=Vbase/gp

Vbase: AK8996's quadratic function generator reference voltage (Vbase = 0.8V)

Find the coefficients (α ga, β ga, γ ga) as the secondary characteristics of the sensitivity temperature drift of a sensor alone from the voltages for Vsenc1, Vsenn1 and Vsenp1.

2) From the AK8996's sensitivity temperature drift measurement result, find the gain values (gicc2, gicn2, gicp2) which are compensated for by the quadratic function generator.

Depicted in this example is the AK8996's quadratic function sensitivity temperature drift measurement result (same is also true with that of a linear function).

gicc2=Vicc2/Vicc2=1, gicn2=Vicn2/Vicc2, gicp2=Vicp2/Vicc2

For the gain values (gicc2, gicn2, gicp2) obtained, find the voltage which is output from the AK8996 quadratic function generator.

Vicc21=Vbase/gicc2, Vicn21=Vbase/gicn2, Vicp21=Vbase/gicp2

Vbase: AK8996's quadratic function generator reference voltage (Vbase = 0.8V)

Find the coefficients (a, b, c) as the secondary characteristics of the AK8996's sensitivity temperature drift from the voltages for Vicc21, Vicn21 and Vicp21. In the same way, find the coefficients (d, e) as the primary characteristics of the AK8996's sensitivity temperature drift from the voltages for Vicc11, Vicn11 and Vicp11.

Specific calculation examples are described here.

■ Offset Temperature Secondary Characteristics Calculation Example (See **5) Register Description** in **"Serial Interface Description"** Section)

Assume the AK8996's secondary characteristics (quadratic function and linear function) as:

Vic=[(g*a)T^2+(g*b)T+(g*c)]+[dT+e]=(g*a)T^2+(g*b+d)T+(g*c+e)

Quadratic function Linear function

For example, the contents of an adjustment register corresponding to the sensor's secondary characteristics is measured by:

Assume the secondary characteristic of the measured sensor is Vsen = 0.0003T^2 - 0.0237T+ 0.0. If the temperature secondary characteristic of the measured AK8996's offset voltage is Vic2=0.0016T^2 - 0.16T + 0.0 and the primary characteristic is Vic1=0.6T + 0.0, set the coefficient so that the sensor's secondary characteristic is canceled out (i.e., AK8996's secondary characteristic becomes Vic=-0.0003T^2 + 0.0237T - 0.0).

EOT2[7]: Second-order coefficient adjustment sign bit for the offset voltage temperature drift
To make the measured AK8996's second-order coefficient (g*a) positive, EOT[7]=0.
To make the measured AK8996's second-order coefficient (g*a) negative, EOT[7]=1.
In this example, set "1" because the second-order coefficient (g*a) is -0.0003.

EOT2[6:0]: Second-order coefficient adjustment bit for the offset voltage temperature drift
Adjust the coefficient in 0.7874% steps.
For example, set EOT2[6:0]=103dec and g*a=-0.000302 for the measured AK8996's second-order coefficient (g*a). That is, the AK8996's secondary characteristic is Vic2=-0.000302T^2 + 0.0302T - 0.0.
0.000302=0.0016*|1-0.7874/100*103|
0.0302=0.16*|1-0.7874/100*103|

Next, adjust the first-order coefficient so that the AK8996's first-order coefficient (g*b + d) equals +0.0237.

EOT1[9]: First-order coefficient adjustment sign bit for the offset voltage temperature drift
Set EOT[9]=0 if the adjustment first-order coefficient d is for addition.
Set EOT[9]=1 if the adjustment first-order coefficient d is for subtraction.
In this example, set "1" because the first-order coefficient (g*b + d) is subtracted from +0.0302 after secondary characteristic adjustment.

EOT1[8:0]: First-order coefficient adjustment bit for the offset voltage temperature drift
Since the first-order coefficient is +0.0237 (=0.0302-0.0065), set EOT1[8:0]=456dec and d=-0.00646. That is, the AK8996's primary characteristic is Vic1=-0.00646T+0.0.
0.00646=0.6*|1-0.1957/100*456|

Now the adjustment of the second-order and first-order coefficients is completed with the adjustment (Vic=0.0003T^2-0.0237T+0.0). The zero order coefficient is, ideally, 0.0, but it could remain as an offset voltage. If that is the case, fine-tune according to the offset voltage fine adjustment procedure after finishing the offset and sensitivity temperature drift adjustment.

■ Sensitivity Temperature Secondary Characteristics Calculation Example (See **5) Register Description** in the **"Serial Interface Description"** section)

Assume the AK8996's secondary characteristics (quadratic function and linear function) as:

Vic=[(g*a)T^2+(g*b)T+(g*c)]+[dT+e]=(g*a)T^2+(g*b+d)T+(g*c+e)

Quadratic function Linear function

For example, the content of the adjustment register corresponds to the sensor's secondary characteristic in the positive pressure is measured by:

Assume the secondary characteristic of the measured sensor is Vsen = 0.00051T^2 - 0.2345T + 0.0. If the secondary characteristic of the measured AK8996's sensitivity temperature is Vic2=0.0016T^2 - 0.16T + 0.0 and the primary characteristic is Vic1=0.32T + 0.0, set the coefficient to match the sensor's secondary characteristic (i.e., AK8996's secondary characteristic becomes Vic= 0.00051T^2 - 0.2345T + 0.0).

ST2P[7]: Second-order coefficient adjustment sign bit for the sensitivity temperature secondary characteristics
Set EST2P[7]=0 to make the measured AK8996's second-order coefficient (g*a) positive.
Set EST2P[7]=1 to make the measured AK8996's second-order coefficient (g*a) negative.
In this example, set "0" because the second-order coefficient (g*a) is 0.00051.

ST2P[6:0]: Coefficient adjustment bit for sensitivity temperature secondary characteristics
Adjust the coefficient in 0.7874% steps.
For example, set EST2P[6:0]=123dec and g*a=0.0005039 for the measured AK8996's second-order coefficient (g*a). That is, the AK8996's secondary characteristic is Vic2 = 0.0005039T^2 - 0.05039T + 0.0.
0.0005039=0.0016*|1-0.7874/100*123|
0.05039=0.16*|1-0.7874/100*123|

Next, adjust the first-order coefficient so that the AK8996's first-order coefficient (g*b + d) equals -0.2345.

ST1P[9]: First-order coefficient adjustment sign bit for the sensitivity temperature secondary characteristics
Set EST1P[9]=0 if the adjustment first-order coefficient d is for addition.
Set EST1P[9]=1 if the adjustment first-order coefficient d is for subtraction.
In this example, set "1" because the first-order coefficient (g*b + d) is subtracted from -0.05039 after secondary characteristics adjustment.

ST1P[8:0] : First-order coefficient adjustment bit for the sensitivity temperature secondary characteristics
Since a first-order coefficient is -0.2345 (=-0.05039-0.18411), set EST1P[8:0]=354dec and d=-0.18434. That is, the AK8996's primary characteristic is Vic1=-0.18434T+0.0.

Now the adjustment of the second-order and first-order coefficients is completed with the adjustment (Vic=0.00051T^2-0.2345T+0.0). The zero order coefficient is, ideally, 0.0, but it could remain as a span voltage. If that is the case, fine-tune according to the span voltage adjustment procedure after finishing the offset and sensitivity temperature drift adjustment.

9. Offset Voltage Fine Adjustment

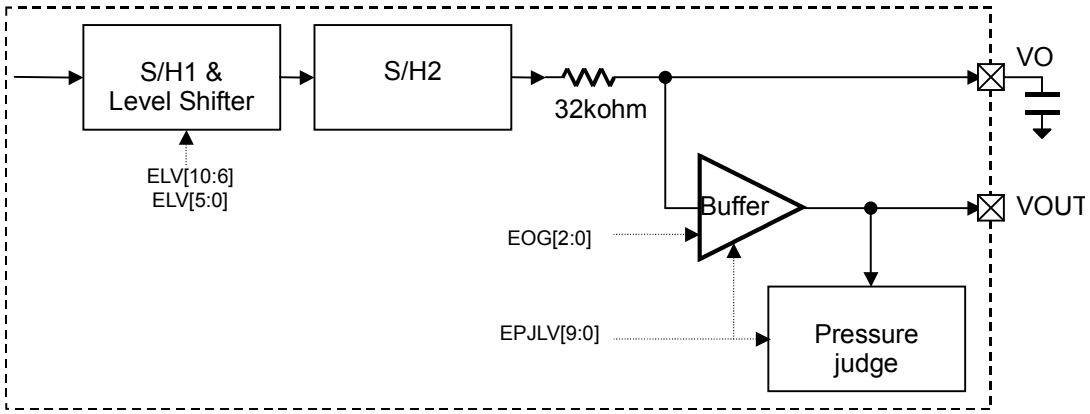
Adjusts the error caused when the offset voltage temperature drift are compensated for. Offset voltage is adjusted using the offset voltage rough adjustment register (Address: 00h data EOC[10:7]) and offset voltage fine adjustment register (Address: 01h data EOC[6:0]).

10. BUFF Gain Adjustment

Adjusts the output buffer gain. The output buffer gain is adjusted using the BUF gain adjustment register (Address: 0Eh data EOG[2:0]).

11. Pressure Determination Threshold and Output Reference Voltage Adjustment

Specific adjustment procedures for the output reference voltage are shown based on this block diagram.



Adjust the pressure determination threshold values (adjust the pressure determination threshold value first, followed by the output reference voltage). Pressure determination threshold values are adjusted using the pressure judgment threshold adjustment registers 1 and 2 (Address: 1D, 1Eh data: EPJLV[9:0]).

As shown in the diagram, the buffer circuit and pressure judgment circuit are tuned for the pressure determination threshold adjustments. Thus, the VO pin voltage after the pressure determination threshold adjustment is almost equal to 2.5V (@VDD: 5V) as a result of the offset voltage adjustment in Section 5. So, after adjusting the pressure determination threshold, some pressure determination threshold values may cause the VOUT pin voltage to get stuck at the supply voltage. For example, if the pressure determination threshold is adjusted to 1.0V with a supply voltage of 5V EOG[2:0]=4hex (set to 4x), the VOUT pin voltage is 1.0 + 4*(2.5 - 1.0) = 7.0V, stuck at the supply voltage.

Adjust the output reference voltage. The output reference voltage is adjusted using the register for the output reference voltage's rough and fine adjustments (Address: 1B, 1Ch data: ELV[10:0]).
First, calculate the adjustment value for the output reference voltage rough adjustment (ELV[10:6]). Specifically, since it is known that the VO pin voltage is 2.5V (@VDD: 5V) and the buffer reference voltage is the pressure determination threshold, calculate so that the difference between the two values is as small as possible. Next, adjust the VOUT pin voltage to the desired output reference voltage using the output reference voltage fine adjustment (ELV[5:0]).

12. Output Span Voltage Fine Adjustment

Adjusts the error caused when the sensitivity temperature drift is compensated for. The output span voltage is adjusted using the output span voltage adjustment register (Address: 02h data ESC[8], address: 03h data ESC[7:0]).

2) Finding the VO Pin External Capacitance (Cap)

This section explains how the VO pin external capacitance is defined. The requirements for determining the VO pin external capacitance value are, the stabilization time of the VOUT pin output voltage on power-up and after exiting the standby mode (STBYN pin "L" to "H") and SINAD (Signal/[Noise + Distortion]).

1. VOUT Pin Output Voltage Stabilization Time

Note that depending on the VO pin external capacitance values, the measurement values (VOUT pin voltage) may contain errors upon power-up or after exiting STBYN. Stabilization time is not dependent on the sampling clock.

Here is an example with the aid of a diagram and tables. "99.5% Settling time (③+④ in the figure)" in the table below represents the time required for the voltage to settle to the output reference voltage X (0.5*VDD in this case) during the period ③ in the figure and the voltage to settle down to 99.5% of the output voltage Y (0.1*VDD in this case) according to the pressure applied during the period (③+④ in the figure). Note)
Under the conditions where the VO pin has an external capacitance of 3µF (sampling frequency 100Hz), the VOUT pin voltage will settle down to 16.4% (0.0815*VDD with respect to the expected 0.5*VDD value) of the output reference voltage during the period ③ in the figure. The period ③ in the figure is fixed to 0.3 msec.

Settling factor A=(1-e^(-0.3[msec]/(560[Ω]*3[µF]))*100=16.4[%]

Subsequently, the output voltage will settle to 99.5% according to the pressure during period ④ in the figure. During period ④ in the figure below, the output will settle down to from 0.0815*VDD to 99.5% of 0.1*VDD in 345.2 msec.

Settling factor B=(0.995*0.1*VDD-0.164*0.5*VDD)/(0.1*VDD-0.164*0.5*VDD)*100=97.2[%]
Settling time D (period ④ in the figure) =-32[kΩ]*3[µF]*ln(1-B/100)=345.2 [msec]

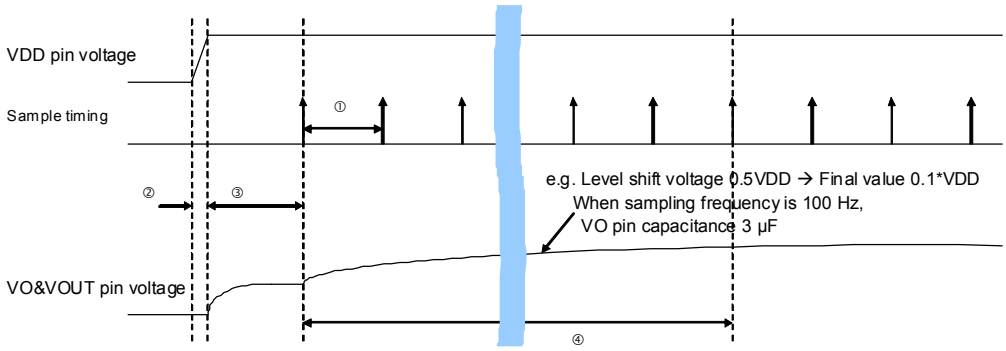
Therefore, the settling time up to 99.5% (period ③+④ in the figure) will be as follows:

99.5% settling time (period ③+④ in the figure) = 0.3 [msec] + D = 345.5 [msec]

Referring to the previous calculation example, determine the stabilization time based on actual requirements:

Prerequisites: Output reference voltage: X
Output voltage (VOUT pin): Y
VO pin external capacitance: Cap (Cap[µF] typ., Cap*1.1[µF] worst)
Internal resistance 1: Res1 (560[Ω] typ., 689.5[Ω] worst)
VO pin internal resistance 2: Res2 (32[kΩ] typ., 39.4[kΩ] worst)
Item C: Y>A*X C=99.5[%]; Y<A*X C=100.5[%]
Period ③ in the figure: Time (0.3[msec] typ., 0.2 or 0.5[msec] worst)

Settling factor A=(1-e^(-Time/(Res1*Cap)))*100
Settling factor B=(C[%]/100*Y-A/100*X)/(Y-A/100*X)*100
Settling time D (period ④ in the figure) =-Res2*Cap*ln(1-B/100)
99.5% settling time (period ③+④ in the figure) = Time + D



① - ④ Reference designators
①: Sampling timing; this diagram represents 100 Hz (10 msec).
②: Power-up rise time (Tvdd), specified as less than 200 µs.
③: Settling time for stable analog operation (Tenable 1, 2).
Specified as either less than 465µs or 495µs depending on whether STBYN pin is used or not.
④: Pressure signal detection time. On power-up or after exiting the STBYN mode, this signal rapidly settles down to the reference voltage.
This time finally settles down depending on the VO pin external capacitance and the internal 32kΩ resistance dependant time constant.
In this case, this period is typically 345.2 msec as shown in the table below.

VO pin Ext. cap	Cutoff Freq. (typical)	Fig ③Time (fixed)		99.5% Settling time (Fig ④)		99.5% Settling time (Fig ③+④)	
		Typical case	Worst case Note)	Typical case	Worst case Note)	Typical case	Worst case Note)
3µF	1.658Hz	0.3 msec	0.2 msec	345.2 msec	617.9 msec	345.5 msec	618.1 msec
1µF	4.974Hz	0.3 msec	0.5 msec	171.8 msec	244.6 msec	172.1 msec	245.1 msec
100nF	49.74Hz	0.3 msec	0.5 msec	21.37 msec	28.96 msec	21.67 msec	29.46 msec
10nF	497.4Hz	0.3 msec	0.5 msec	2.139 msec	2.897 msec	2.439 msec	3.397 msec
1nF	4.97kHz	0.3 msec	0.5 msec	0.214 msec	0.290 msec	0.514 msec	0.790 msec
500pF	9.95kHz	0.3 msec	0.5 msec	0.107 msec	0.145 msec	0.407 msec	0.645 msec

Note) Worst case for external capacitance ±10% and lot variations.

Note)
The output reference voltage X (VO pin output) that is settled to during the period ③ in the diagram, which is dependent on the output reference voltage rough & fine adjustment register (Address: 1B, 1Ch data: ELV[10:0]), is given by:

ELVR[9: 6]			VO pin		Comments
Dec	Hex	Bin	ELVR[10]=0 (*VDD)	ELVR[10]=1 (*VDD)	
0	0	0000	0.5	0.5	Default
1	1	0001	0.4	0.5	
2	2	0010	0.4	0.5	
3	3	0011	0.4	0.5	
4	4	0100	0.4	0.6	
5	5	0101	0.3	0.6	
6	6	0110	0.3	0.6	
7	7	0111	0.3	0.6	
8	8	1000	0.3	0.7	
9	9	1001	0.2	0.7	
10	A	1010	0.2	0.7	
11	B	1011	0.2	0.7	
12	C	1100	0.2	0.8	
13	D	1101	0.1	0.8	
14	E	1110	0.1	0.8	
15	F	1111	0.1	0.8	

2. VOUT pin SINAD

Summarized in this table is the relationship between the VO pin's external capacitance and SINAD. Note that the SINAD should be 46dB or larger if 0.5% FS adjustment accuracy is required.

Sampling Freq.	VO pin Ext. cap	Cutoff Freq. (typical)	SINAD characteristics	
			Typical case	Worst case Note)
100Hz	5μF	0.995Hz	49.59dB	46.39dB
	3μF	1.658Hz	45.15dB	41.95dB
	1μF	4.974Hz	35.61dB	32.41dB
	100nF	49.74Hz	15.73dB	12.66dB
1kHz	1μF	4.974Hz	55.61dB	52.41dB
	100nF	49.74Hz	35.61dB	32.41dB
	10nF	497.4Hz	15.73dB	12.66dB
10.24kHz	100nF	49.74Hz	55.82dB	52.62dB
	10nF	497.4Hz	35.82dB	32.62dB
	1nF	4.97kHz	15.93dB	12.85dB
	500pF	9.95kHz	10.23dB	7.46dB

Note) Worst case for external capacitance ±10% and lot variations.

As mentioned in Sections "1. VOUT pin output voltage stabilization time" and "2. VOUT pin SINAD", the VO pin external capacitance value should be reduced to decrease the measurement time. For increased SINAD, the VO pin external capacitance value should be greater.

On determining the VO pin external capacitance value, the various conditions should be thoroughly reviewed according to the application requirements.

3) Pressure Detection & Determination Circuit Operation at Power-Up and Standby Exit (STBYN pin "L" to "H")

Use caution when operating the pressure detection and pressure determination circuits on power-up and after exiting the standby mode (STBYN pin "L" to "H").

1. Pressure detection circuit operation

For proper operation of the pressure detection circuit, it is necessary to settle the VOUT pin output voltage to within ±0.5% of the output reference voltage configured in the "Settling time for stable analog operation" (See "Operation Sequence" Section).

The VOUT pin output voltage settles in the time constant determined by the 32kΩ internal resistance and VO pin external capacitance. To understand settling time, see **2) Finding the VO pin external capacitance (Cap)**. If the Cap value is 0.1µF or less, the VOUT pin output voltage settles to within ±0.5% of the output reference voltage, while with the use of capacitance greater than 0.1µF, errors may be detected because it does not settle to within ±0.5%.

In order to avoid this problem, the pressure detector should be left disabled for a short time at power-up and at exiting the STBYN mode. Calculate the disable time based on **2) Finding the VO pin external capacitance (Cap).** There is a simplified equation to determine the worst-case value:

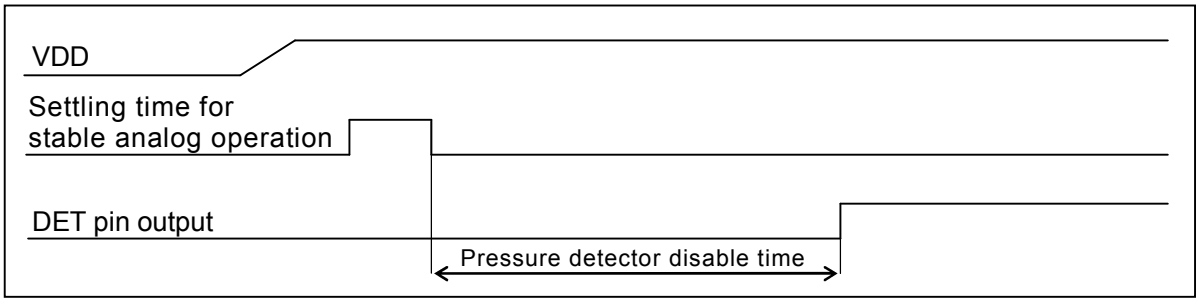
Disable time = -39400[Ω] * 1.1*C[F] |* ln (1-0.995)

2. Pressure Detection Circuit Disable Time

Pressure detection circuit Disable time is the time from exit of the settling time for stable analog operation to the pressure detection output. Pressure detection circuit Disable time with pressure detection valid and both pressure detection and self-diagnosis valid is shown below.

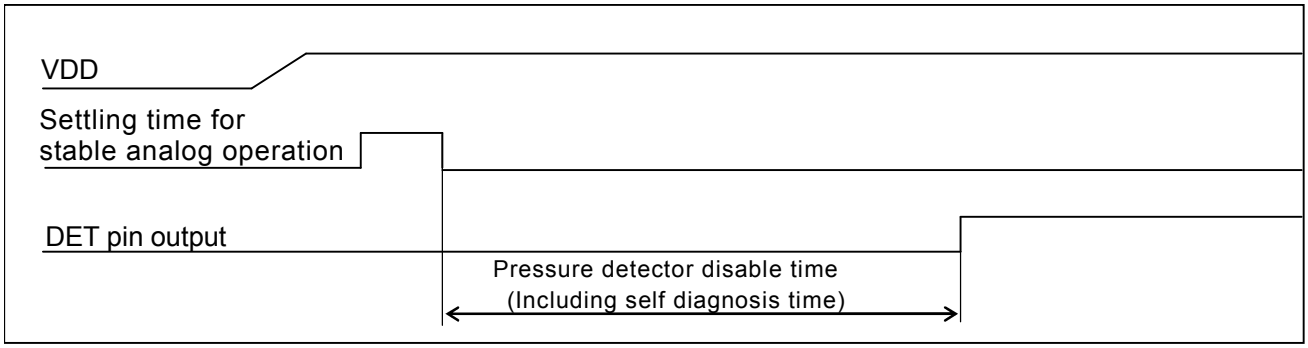
2.1 Pressure detection valid (EINT1[1:0]=1h)

EAS[2: 0]			Pressure Detector Disable Time (msec)				Comments
Dec	Hex	Bin	fs: 100Hz	fs: 1kHz	fs: 2kHz	fs: 10kHz	
0	0	000	10	1.0	0.5	0.1	Default
1	1	001	10	1.0	0.5	0.2	
2	2	010	20	2.0	1.0	0.4	
3	3	011	60	6.0	3.0	0.8	
4	4	100	140	14.0	7.0	1.6	
5	5	101	300	30.0	15.0	3.1	
6	6	110	620	62.0	31.0	6.3	
7	7	111	1260	126.0	63.0	12.5	



2.2 Pressure detection & self diagnosis valid (EINT1[1:0]=3h)

EAS[2: 0]			Pressure Detector Disable Time (msec)				Comments
Dec	Hex	Bin	fs: 100Hz	fs: 1kHz	fs: 2kHz	fs: 10kHz	
0	0	000	10.2	1.2	0.7	0.3	Default
1	1	001	10.2	1.2	0.7	0.3	
2	2	010	40.2	4.2	2.2	0.6	
3	3	011	80.2	8.2	4.2	1.0	
4	4	100	160.2	16.2	8.2	1.8	
5	5	101	320.2	32.2	16.2	3.3	
6	6	110	640.2	64.2	32.2	6.5	
7	7	111	1280.2	128.2	64.2	12.7	



3. Pressure determination circuit operation

The settling time for the VOUT pin voltage is, as with the pressure detector, determined by the 32kΩ internal resistor and VO pin external capacitance C. Current specifications (C≤0.1μF) do not cause any problem with the pressure determination results, whereas misinterpretation may occur in the pressure determination circuit if a capacitance of more than 0.1μF is used. These matters should be carefully considered before use.

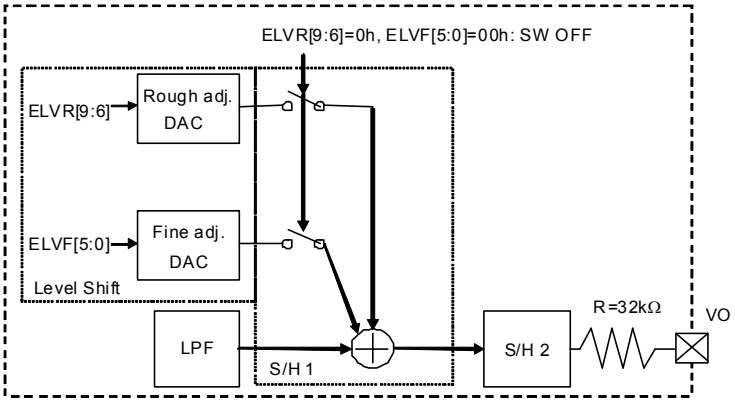
4) Power Consumption

Current values described in 3) Power Consumption in the Electrical Characteristics are those for the average current. The maximum current is shown in the table below. Use a power supply with sufficient supply capacity by referring to this table:

	Unit	VDD: 3.6V	VDD: 5.5V	Note
Max. Current	mA	2.4	3.5	Reference value for design

5) Note on the Use of Output Reference Voltage Switching Circuit (Level Shift)

S/H1 & Level Shift circuit is configured as shown here:



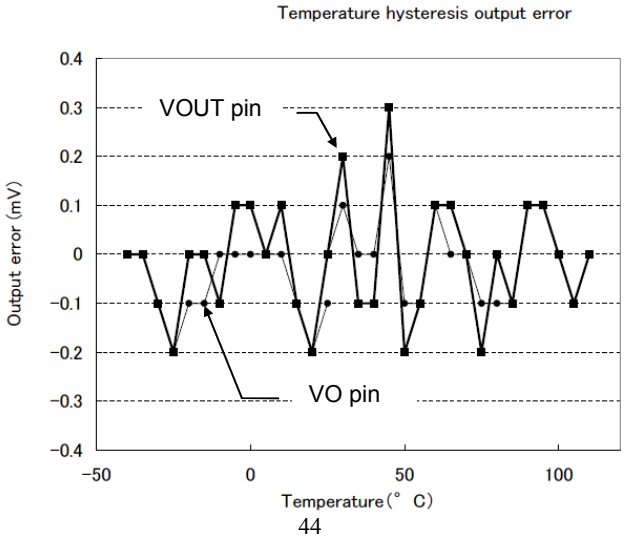
From this diagram, the switching operation inside the S/H1 differs between the code setup for ELVR[9:6]=0h, ELVF[5:0]=00h (register LVR, LVF Address 1Bh, 1Ch) and otherwise. If the data is set up as shown, both switches are turned off, while in other situations they are turned on.
In some circumstances, an adjustment step for the fine adjustment DAC on the VO pin or VOUT pin cannot maintain the monotonicity between the ELVF[5:0]=00h and the other codes. Use adequate care, especially when the output reference voltage is set around 0.5VDD.

6) Data Reproducibility at Measuring the Temperature Drift

AK8996 temperature drift data reproducibility experiments have been conducted. The experimental result shown here indicates that the AK8996 temperature drift data reproducibility is within ±0.3 mV. Note that the experimental result shown here is for reference:
Experiment conditions

Supply voltage:	5V
Input voltage:	40 mV (=VP-VN)
Output reference voltage:	0.5*VDD
Gain:	25 times
VO pin external capacitance:	10nF
Environmental temperature sweep:	25°C → -40°C → 25°C → 125°C → 25°C
Measurement pin:	VO pin, VOUT pin

Experiment result: The graph shows that the resulting variations are within ±0.3mV.



7) Offset Temperature Primary Characteristics (Compensation Procedure)

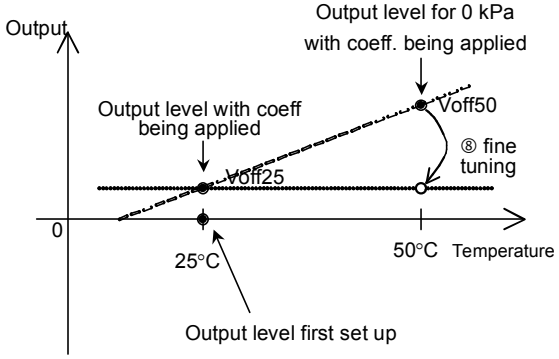
If the offset temperature drift first order coefficient is left over after adjustment of the sensor characteristics, follow the readjustment procedure. Ensure that this procedure is conducted before **9. Offset Voltage Fine Adjustment**.

Readjustment Procedure (See the figure below)

1. On the most recent setup of the adjustment temperature (e.g., at 50ºC), calculate the coefficient to be applied to the AK8996.
2. After setup, measure the VOUT pin voltage (Voff50) with the pressure set to 0kPa.
3. Store the measured value in the memory (e.g., address 16 hex EUE[7:0]).
4. Restore the temperature to 25ºC (last adjustment phase).
5. Measure the VOUT pin voltage (Voff25) with the pressure set to 0kPa.

The adjustment procedure is normally completed with the adjustments of the offset voltage, pressure determination threshold, output reference voltage and output span voltage fine adjustment. If, however, offset temperature characteristic first-order coefficient needs to be adjusted, the following adjustments should be performed first:

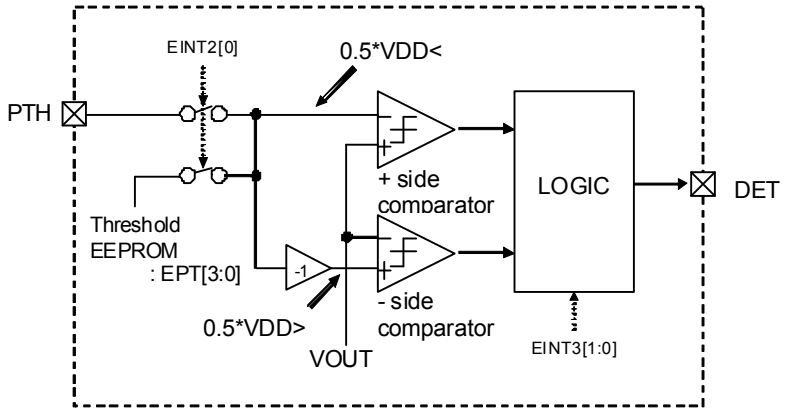
6. Calculate the remaining offset temperature characteristic first-order coefficients.
   Remaining offset temperature characteristic 1st order coeff. =
   (Voff50-Voff25)/(50-25)[mV/ºC]···(A)
7. Calculate a gradient per step from the offset temperature drift first-order coefficient (e.g., 0.04[mV/ºC]).
   Adjustment code = (A)/0.04
8. Apply the calculated adjustment code to the OT1 register (address 06 hex).



8) Pressure Detector's Detection Threshold

Information about the setup of the pressure detector's detection threshold and the setup range of the detection threshold based on the mode setup is summarized.

Block diagram of the pressure detector:



The pressure detector's detection threshold can be set up, as shown in the block diagram, either through the external input (PTH pin) or internal setup (EEPROM setup EPT[3:0]). Selecting the external input or internal setup can be performed using the EEPROM (EINT2[0]).

As shown in the block diagram, the pressure detector's detection threshold is limited by the setup range depending on the mode setup. Setup range limitations are summarized here; use care when using the pressure detector.

EINT3 [1:0]	Symbol	Mode setup	Detection threshold setup range
00	INT<	Detect pressure above threshold	0.5*VDD~0.95*VDD @VDD: 5V
01	INT>	Detect pressure below threshold	0.05*VDD~0.5*VDD @VDD: 5V
10	INT><	Detect pressure either above or below threshold	~(0.5*VDD~0.95*VDD), (0.05*VDD~0.5*VDD)~ @VDD: 5V
11	INT<>	Detect pressure within a certain range	(0.5*VDD~0.95*VDD) ~(0.05*VDD~0.5*VDD) @VDD: 5V

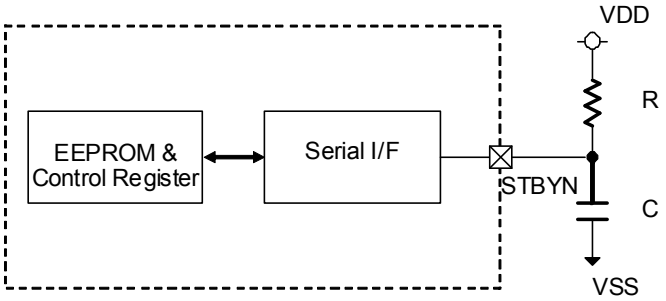
For example, if EINT3[1:0]: 0hex is set, the detection threshold range is, as shown in the table, 0.5*VDD to 0.95*VDD @VDD: 5V. This means that setup below 0.5*VDD cannot be achieved, so due consideration must be given when using it.

9) Note on the AK8996 Power-up

When applying the power to the AK8996, use caution to the following.
On power up the AK8996, keep the rise time below 200µs (0.1*VDD -> 0.8*VDD). If the rise time on power up exceeds 200µs, this section may enter the test mode. The AK8996 may not function properly in the test mode. To exit from the test mode, reset at the STBYN pin or recycle the power.
If the AK8996 cannot be powered up in less than 200µs, connect the STBYN pin to the resistor (R) and capacitor (C) as shown below. Determine the resistance (R) and capacitance (C) values so that the STBYN pin voltage is 0.3*VDD or less when the supply voltage reaches the VDD to ensure the AK8996 digital circuit is reset on power up.
The following equation is used to calculate the resistance (R) and capacitance (C) values.

$$Vstbyn = VDD * [1-exp(-t/R*C)]$$

Vstbyn : STBYN pin voltage
t : Time required to reach Vstbyn voltage



10) Note on the pressure detection circuit hysteresis voltage setup

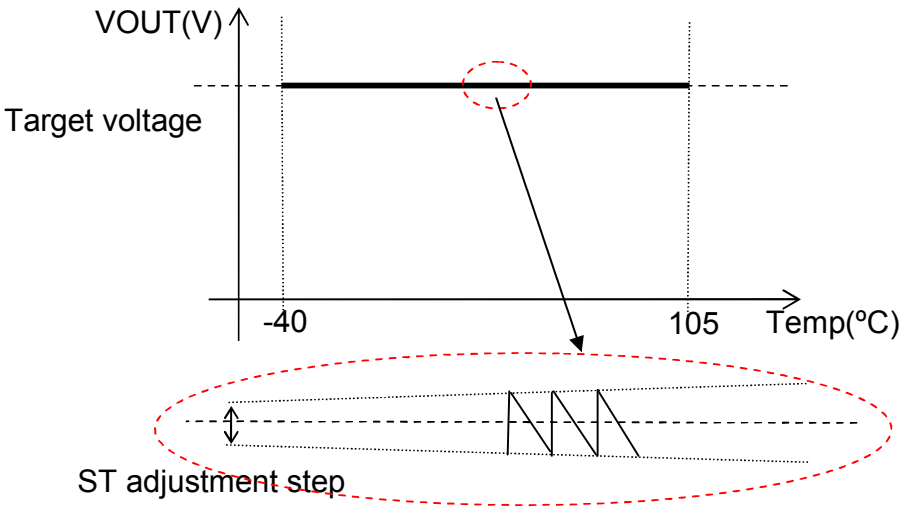
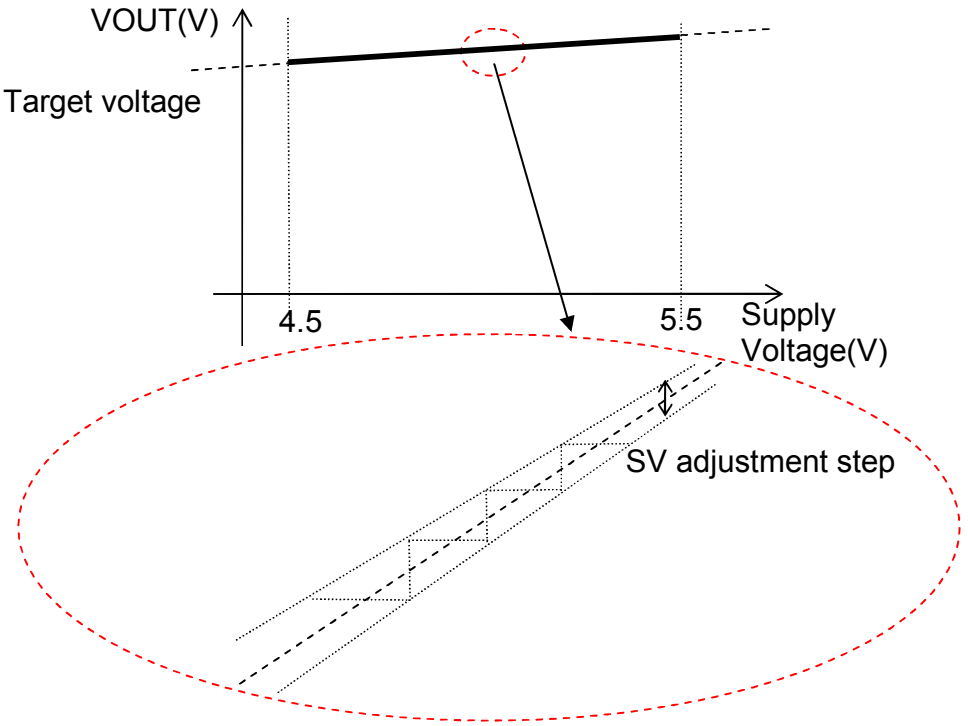
Use caution to the following when setting up the pressure detection circuit hysteresis voltage.
The hysteresis voltage is normally used as negative with respect to the pressure detection threshold value reference. If, however, the hysteresis voltage is set to a low value (e.g. 0.0025*VDD), the hysteresis voltage may be positive with respect to the pressure detection threshold reference. In that case, the pressure detection circuit may not function properly.
To avoid the above situations, be sure to adjust the hysteresis voltage in the adjustment phase before using the pressure detection circuit hysteresis voltage. Also note that the hysteresis voltage varies with the supply voltage.
The hysteresis voltages for four different supply voltages (2.5V, 3.0V, 3.3V, 5V) are shown in the table below. Regions in the table where hysteresis voltage is likely to be inverted are shaded in red and the regions the voltage is the least likely to be inverted are shaded in blue. Note that the table in the below is for reference purpose only; do not use it as being guaranteed.

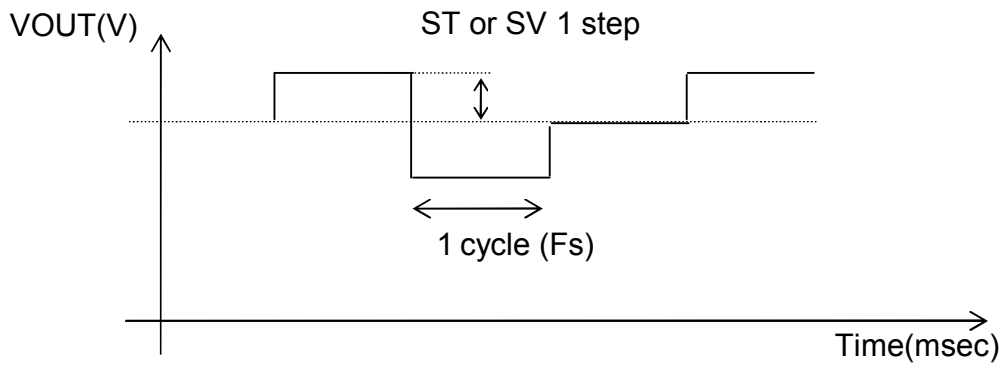
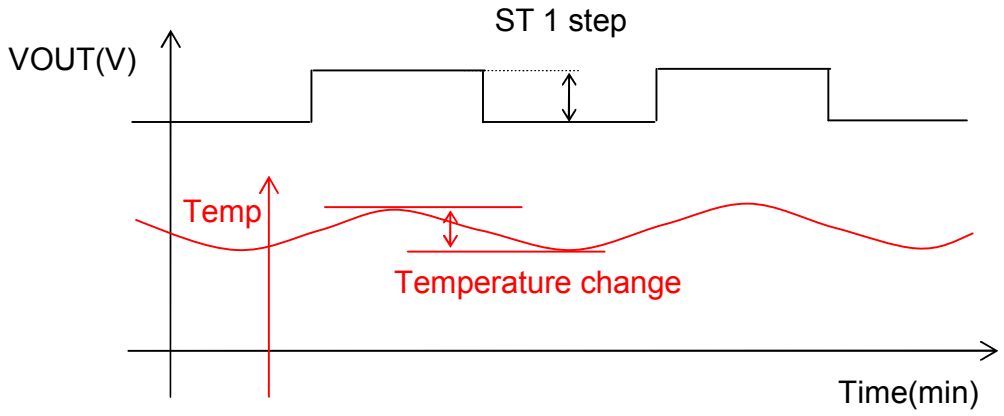
Address : 11 hex D[2:0]=EHYS[2:0]

EHYS[2:0]			VDD	Hysteresis voltage (mV)				units
Dec	Hex	Bin	Reference	VDD:2.5V	VDD:3V	VDD:3.3V	VDD:5V	
0	0	000	0.0200*VDD	-50.00	-60.00	-66.00	-100.0	mV
1	1	001	0.0175*VDD	-43.75	-52.50	-57.75	-87.5	mV
2	2	010	0.0150*VDD	-37.50	-45.00	-49.50	-75.0	mV
3	3	011	0.0125*VDD	-31.25	-37.50	-41.25	-62.5	mV
4	4	100	0.0100*VDD	-25.00	-30.00	-33.00	-50.0	mV
5	5	101	0.0075*VDD	-18.75	-22.50	-24.75	-37.5	mV
6	6	110	0.0050*VDD	-12.50	-15.00	-16.50	-25.0	mV
7	7	111	0.0025*VDD	-6.25	-7.50	-8.25	-12.5	mV

11) VOUT Output

The AK8996 VOUT output shows four kinds of output waveforms below according to the condition. Please use the AK8996 understanding of those output waveforms may come.

No	Item	Content
1	Description	**Sensitivity temperature variation characteristic (ST operation) :** When temperature changes, VOUT output shows sawtooth waveform within ST adjustment step, according to the pressure applied.
	Output Waveform	
2	Description	**Sensitivity supply voltage variation characteristic (SV operation) :** When supply voltage changes, VOUT output shows stepwise waveform within SV adjustment step , according to the pressure applied.
	Output Waveform	

No	Item	Content
3	Description	**VOUT output time change 1 :** When the band is not limited, a VOUT output shows stepwise change for every sampling period in the following figures. Since its change occurs for every sampling period, it can be reduced by using bandwidth shaping filter.
	Output Waveform	
4	Description	**VOUT output time change 2 :** When temperature changes slowly to compare with the band-limited time, a VOUT output shows stepwise change with temperature change in the following figures. For example, it occurs when the temperature in a thermostat chamber changes slowly.
	Output Waveform	

Serial Interface Description

The AK8996 writes data to and reads data from the EEPROM and control register (volatile memory) through a three-wire synchronous serial interface, consisting of SCLK, SDI/O and CS. The serial interface circuit in its input standby state detects the CS high signal and captures data from SDI/O in sync with the rising edge of the SCLK, and outputs data from SDI/O synchronous with the rising edge of SCLK. Input data contains three instruction bits (12 - 10), five address bits (A4 - A0) and eight data bits (D7 - D0). Provide the data in the order of I2 → I0 → A4 → A0 → D7 → D0.

On the WRITE instruction, allow 5msec or more write time for EEPROM and 300nsec or more write time for the control register (see Twr in 6) Digital AC Characteristics in the Electrical Characteristics section). For the READ instruction, data is written up to 8CLK for SCLK (any values are acceptable because the data is ignored) and the data output starting at the rising edge of 9CLK is read out.

1) Data Configuration

Configuration of data written to or read out through the serial interface is shown below. There are 16 specific bits of data in total comprised of three instruction bits, five address bits and eight data bits.

Instruction			Address					Data							
I2	I1	I0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

←Data input direction

2) Description of Instructions

Instruction codes are summarized below.

Code Note)			Instruction	Description
I2	I1	I0		
1	1	0	EEPROM read (Read Mode)	Reads out the data written in the EEPROM
1	0	1	EEPROM write (Write Mode)	Writes data to the EEPROM. Write time (from 16th SCLK rising edge to CS falling edge) requires 5msec or more.
			EEPROM batch write (Write Mode)	If the 19h address is written, input data is written to all addresses. Write time (from 16th SCLK rising edge to CS falling edge) requires 10msec or more.
0	1	0	Control reg. read (Read Mode)	Reads out the data written in the control register.
0	0	1	Control reg. write (Write Mode)	Writes the data to the control register. Write time (from 16th SCLK rising edge to CS falling edge) requires 300nsec or more.

Note) Instructions other than this are prohibited.

3) Register Map

3.1) EEPROM Register Map

Name	Content	Address (hex)	Data Note 1) D7	D6	D5	D4	D3	D2	D1	D0
OCR	Offset voltage rough adj.	00h					EOC[10]	EOC[9]	EOC[8]	EOC[7]
							0	0	0	0
OCF	Offset voltage fine adj.	01h		EOC[6]	EOC[5]	EOC[4]	EOC[3]	EOC[2]	EOC[1]	EOC[0]
				0	0	0	0	0	0	0
SCS	Output span voltage adj.	02h								ESC[8]
										0
SC	Output span voltage adj.	03h	ESC[7]	ESC[6]	ESC[5]	ESC[4]	ESC[3]	ESC[2]	ESC[1]	ESC[0]
			0	0	0	0	0	0	0	0
OT2	Offset voltage temp. drift adj. (2nd order coeff.)	04h	EOT2[7]	EOT2[6]	EOT2[5]	EOT2[4]	EOT2[3]	EOT2[2]	EOT2[1]	EOT2[0]
			0	0	0	0	0	0	0	0
OT1S	Offset voltage temp. drift adj. (1st order coeff.)	05h							EOT1[9]	EOT1[8]
									0	0
OT1	Offset voltage temp. drift adj. (1st order coeff.)	06h	EOT1[7]	EOT1[6]	EOT1[5]	EOT1[4]	EOT1[3]	EOT1[2]	EOT1[1]	EOT1[0]
			0	0	0	0	0	0	0	0
ST2P	Sens. temp. drift adj. (2nd order coeff. +ve)	07h	EST2P[7]	EST2P[6]	EST2P[5]	EST2P[4]	EST2P[3]	EST2P[2]	EST2P[1]	EST2P[0]
			0	0	0	0	0	0	0	0
ST2N	Sens. temp. drift adj. (2nd order coeff. -ve)	08h	EST2N[7]	EST2N[6]	EST2N[5]	EST2N[4]	EST2N[3]	EST2N[2]	EST2N[1]	EST2N[0]
			0	0	0	0	0	0	0	0
ST1PS	Sens. temp. drift adj. (1st order coeff. +ve)	09h							EST1P[9]	EST1P[8]
									0	0
ST1P	Sens. temp. drift adj. (1st order coeff. +ve)	0Ah	EST1P[7]	EST1P[6]	EST1P[5]	EST1P[4]	EST1P[3]	EST1P[2]	EST1P[1]	EST1P[0]
			0	0	0	0	0	0	0	0
ST1NS	Sens. temp. drift adj. (1st order coeff. -ve)	0Bh							EST1N[9]	EST1N[8]
									0	0
ST1N	Sens. temp. drift adj. (1st order coeff. -ve)	0Ch	EST1N[7]	EST1N[6]	EST1N[5]	EST1N[4]	EST1N[3]	EST1N[2]	EST1N[1]	EST1N[0]
			0	0	0	0	0	0	0	0
ING	Input gain adj.	0Dh					EIG[3]	EIG[2]	EIG[1]	EIG[0]
							0	0	0	0
BUFG	BUF gain adj.	0Eh						EOG[2]	EOG[1]	EOG[0]
								0	0	0
AS	Pressure detector disable time adj.	0Fh						EAS[2]	EAS[1]	EAS[0]
								0	0	0
PTH	Pressure detector threshold	10h					EPT[3]	EPT[2]	EPT[1]	EPT[0]
							0	0	0	0
HYS	Pressure detector comparator hysteresis voltage adj.	11h						EHYS[2]	EHYS[1]	EHYS[0]
								0	0	0
VREF *	VREF voltage adj.	12h						EVR[2]	EVR[1]	EVR[0]
								0	0	0
IREF *	IREF current adj.	13h					EIR[3]	EIR[2]	EIR[1]	EIR[0]
							0	0	0	0
OSC *	OSC frequency adj.	14h					EFR[3]	EFR[2]	EFR[1]	EFR[0]
							0	0	0	0
VTMP *	VTMP adj.	15h			ETM[5]	ETM[4]	ETM[3]	ETM[2]	ETM[1]	ETM[0]
					0	0	0	0	0	0

UE	Customer data write use	16h	EUE[7]	EUE[6]	EUE[5]	EUE[4]	EUE[3]	EUE[2]	EUE[1]	EUE[0]
			0	0	0	0	0	0	0	0
MM	Measurement mode	17h			EAC[1]	EAC[0]	EVD[0]	ESF[1]	ESF[0]	EBU[0]
					0	0	0	0	0	0
INT	Pressure detection & self-diagnosis mode	18h			EOUT[0]	EINT1[1]	EINT1[0]	EINT2[0]	EINT3[1]	EINT3[0]
					0	0	0	0	0	0
AW	EEPROM batch write mode	19h	EAW[7]	EAW[6]	EAW[5]	EAW 4]	EAW[3]	EAW[2]	EAW[1]	EAW[0]
			-	-	-	-	-	-	-	-
	Reserved	1Ah								
LVR	Out reference voltage rough adj. (Level shift rough)	1Bh				ELV[10]	ELV[9]	ELV[8]	ELV[7]	ELV[6]
						0	0	0	0	0
LVF	Out reference voltage fine adj. (Level shift fine)	1Ch			ELV[5]	ELV[4]	ELV[3]	ELV[2]	ELV[1]	ELV[0]
					0	0	0	0	0	0
PJLV2	Pressure judge threshold adj. 2	1Dh							EPJLV[9]	EPJLV[8]
									0	0
PJLV1	Pressure judge threshold adj. 1	1Eh	EPJLV[7]	EPJLV[6]	EPJLV[5]	EPJLV[4]	EPJLV[3]	EPJLV[2]	EPJLV[1]	EPJLV[0]
			0	0	0	0	0	0	0	0
	Reserved	1Fh								

Note 1) Lower line of each data represents the factory settings written to EEPROM.
Note 2) Access to addresses other than the above is prohibited.
Note 3) Write "0" to the unused D[7:0].
Note 4) For a packaged device, registers marked with * are adjusted before shipment.
Therefore, defaults are not "0".

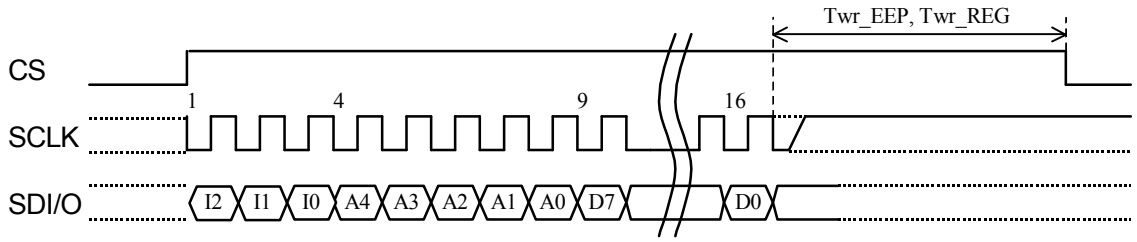
3.2) Control Register (Volatile Memory) Map

Name	Content	Address (hex)	Data Note 1) D7	D6	D5	D4	D3	D2	D1	D0
CM1	Adjustment mode 1	00h		AC[1]	AC[0]	AM[3]	AM[2]	AM[1]	AM[0]	AEPEN[0]
				0	0	0	0	0	0	0
CM2	Adjustment mode 2	01h			INSW[1]	INSW[0]	OTSW[0]	STSW[0]	2ND[1]	2ND[0]
					0	0	0	0	0	0
	Reserved	02h – 1Fh								

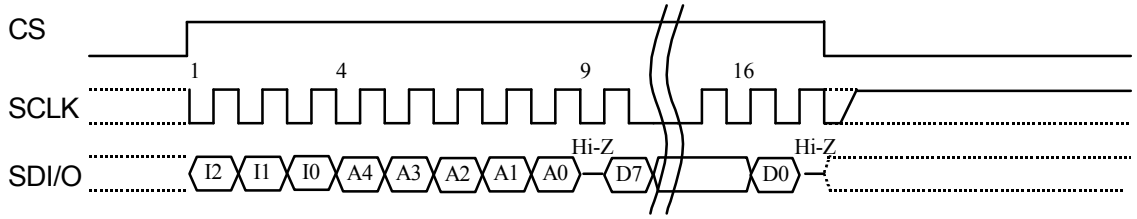
Note 1) Lower line of each data represents the control register data at power-up and STBYN "L".
Note 2) Access to addresses other than the above is prohibited.
Note 3) Write "0" to the unused D[7:0].

4) Serial Interface Timing Diagram

[WRITE Mode]



[READ Mode]



5) Register Description

5.1) Description of EEPROM Register

5.1.1) Adjustment Section Register

Offset and span adjustment should be made after mode setup and adjustment of the reference generator section including VREF, IREF, OSC and VTMP.

***** CAUTION *****
At the time of adjustment, set the EEPROM control mode to EEPROM Always Operating mode (Control register Address 01 hex AEPEN[0]:1).

a) Offset voltage adjustment (Register names: OCR, OCF)

Rough adjustment should be performed first, followed by a fine adjustment for the offset voltage. The content of the adjustment registers are shown here.

a-1) Offset voltage rough adjustment (OCR)

The offset voltage is coarsely tuned.
The offset adjustment voltage varies ratiometrically with respect to the supply voltage.
The ratio in the table below is benchmarked to a VOUT output of 4000 mV (@VDD: 5V) as 100% (ratio = (Offset voltage @VDD: 5V)/4000[mV]*100[%]).

Address: 00 hex D[3:0]=ECO[10:7]

EOC[9: 7]			Ratio	VDD: 3V		VDD: 5V		Comments
Dec	Hex	Bin	(%)	EOC [10]=0 (mV)	EOC [10]=1 (mV)	EOC [10]=0 (mV)	EOC [10]=1 (mV)	
0	0	000	0.00	0	0	0	0	Default
1	1	001	7.50	150	-150	300	-300	
2	2	010	15.00	300	-300	600	-600	
3	3	011	22.50	450	-450	900	-900	
4	4	100	30.00	600	-600	1200	-1200	
5	5	101	37.50	750	-750	1500	-1500	
6	6	110	45.00	900	-900	1800	-1800	
7	7	111	52.50	1050	-1050	2100	-2100	

a-2) Offset voltage fine adjustment (OCF)

The offset voltage is fine-tuned.
The offset adjustment voltage varies ratiometrically with respect to the supply voltage.
The ratio in the table below is benchmarked to a VOUT output of 4000mV (@VDD: 5V) as 100% (ratio = (Offset voltage @VDD: 5V)/4000[mV]*100[%]).

Address: 01 hex D[6:0]=ECO[6:0]

EOC [5:0]			Ratio	VDD: 3V		VDD: 5V		Comments
Dec	Hex	Bin	(%)	EOC [6]=0 (mV)	EOC [6]=1 (mV)	EOC [6]=0 (mV)	EOC [6]=1 (mV)	
0	00	000000	0.0000	0	0	0	0	Default
1	01	000001	0.1250	2.5	-2.5	5	-5	
:	:	:		:	:	:	:	
10	0A	001010	1.2500	25.0	-25.0	50	-50	
11	0B	001001	1.3750	27.5	-27.5	55	-55	
:	:	:		:	:	:	:	
20	14	010100	2.5000	50.0	-50.0	100	-100	
21	15	010101	2.6250	52.5	-52.5	105	-105	
:	:	:		:	:	:	:	
30	1E	011110	3.7500	75.0	-75.0	150	-150	
31	1F	011111	3.8750	77.5	-7.5	155	-155	
:	:	:		:	:	:	:	
40	28	101000	5.0000	100.0	-100.0	200	-200	
41	29	101001	5.1250	102.5	-102.5	205	-205	
:	:	:		:	:	:	:	
50	32	110010	6.2500	125.0	-125.0	250	-250	
51	33	110011	6.3750	127.5	-127.5	255	-255	
:	:	:		:	:	:	:	
62	3E	111110	7.7500	155.0	-155.0	310	-310	
63	3F	111111	7.8750	157.5	-157.5	315	-315	

b) Output span voltage adjustment (Register names: SCS, SC)

Adjusts the span voltage.
The magnification factor in this table represents an adjustment factor benchmarked to a VOUT output of 4000mV (@VDD: 5V) as 1 (factor) = 100[%]/100[%].
The output and sensitivity describes the adjustable output voltages with the assumed reference output (2V@VDD: 3V, 4V@VDD: 5V) when ESC[8:0] = 0 dec.

Address: 02 hex - 03 hex D[8:0]=ESC[8:0]

ESC[8:0]			Magnification	VDD: 3V		VDD: 5V		Comments
Dec	Hex	Bin	(Factor)	Output (mV)	Sens. (Factor)	Output (mV)	Sens. (Factor)	
-256	100	100000000	100/164.00	1220	30.488	2439	30.488	
-255	101	100000001	100/163.75	1221	30.534	2443	30.534	
:	:	:	:	:	:	:	:	
-160	160	101100000	100/140.00	1429	35.714	2857	35.714	
-159	161	101100001	100/139.75	1431	35.778	2862	35.778	
:	:	:	:	:	:	:	:	
-41	1D7	111010111	100/110.25	1814	45.351	3628	45.351	
-40	1D8	111011000	100/110.00	1818	45.455	3636	45.455	
:	:	:	:	:	:	:	:	
-2	1FE	111111110	100/100.50	1990	49.751	3980	49.751	
-1	1FF	111111111	100/100.25	1995	49.875	3990	49.875	
0	000	000000000	100/100.00	2000	50.000	4000	50.000	Default
1	001	000000001	100/99.75	2005	50.125	4010	50.125	
2	002	000000010	100/99.50	2010	50.251	4020	50.251	
:	:	:	:	:	:	:	:	
40	028	000101000	100/90.00	2222	55.556	4444	55.556	
41	029	000101001	100/89.75	2228	55.710	4457	55.710	
:	:	:	:	:	:	:	:	
159	09F	010011111	100/60.25	3320	82.988	6639	82.988	
160	0A0	010100000	100/60.00	3333	83.333	6667	83.333	
:	:	:	:	:	:	:	:	
254	0FE	011111110	100/36.50	5479	136.99	10959	136.99	
255	0FF	011111111	100/36.25	5517	137.93	11034	137.93	

c) Offset voltage temperature drift adjustment

Adjusts the offset voltage temperature secondary characteristics inherent to a sensor and the AK8996. After performing the offset voltage adjustment at 25ºC, use the register's offset voltage temperature characteristic coefficients for adjustment so that the absolute values of the AK8996's coefficient are matched to those of the sensor's coefficient. (See 1) Adjustment Procedure Description in "Functional Description" in the "Adjustment Sequence" section)

c-1) Offset voltage temperature drift 2nd order coefficient adjustment (Register name: OT2)

Address: 04 hex D[7:0]=EOT2[7:0]

EOT2[6:0]			Ratio	EOT2[7]:0	EOT2[7]:1	Comments
Dec	Hex	Bin	(%)	VDD: 5V / 3V	VDD: 5V / 3V	
0	00	0000000	100.000	0.00160000 /0.00080000	-0.00160000 /-0.00080000	Default
1	01	0000001	99.213	0.0015874 /0.0007937	-0.0015874 /-0.0007937	
…..						
16	10	0010000	87.402	0.00139842 /0.00069921	-0.00139842 /-0.00069921	
…..						
32	20	0100000	74.803	0.00119685 /0.000598425	-0.00119685 /-0.000598425	
…..						
64	40	1000000	49.606	0.0007937 /0.00039685	-0.0007937 /-0.00039685	
…..						
126	3E	1111110	0.7874	0.0000126 /0.000006299	-0.0000126 /-0.000006299	
127	3F	1111111	0.0	0.0	0.0	

c-2) Offset voltage temperature drift 1st order coefficient adjustment (Register names: OT1S, OT1)

Address: 05 hex - 06 hex D[9:0]=EOT1[9:0]

EOT1[8:0]			Ratio	EOT1[9]:0	EOT1[9]:1	Comments
Dec	Hex	Bin	(%)	VDD: 5V / 3V	VDD: 5V / 3V	
0	000	000000000	100.000	0.6000 /0.3000	-0.6000 /-0.3000	Default
1	001	000000001	99.804	0.5988 /0.2994	-0.5988 /-0.2994	
…..						
64	030	001000000	87.4755	0.5249 /0.2624	-0.5249 /-0.2624	
…..						
128	040	010000000	74.9511	0.4497 /0.2249	-0.4497 /-0.2249	
…..						
256	100	100000000	49.9022	0.2994 /0.1497	-0.2994 /-0.1497	
…..						
510	1FE	111111110	0.1957	0.001174 /0.0005871	-0.001174 /-0.0005871	
511	1FF	111111111	0.0	0.0	0.0	

d) Sensitivity temperature drift adjustment (Register names: ST2P, ST2N, ST1PS, ST1P, ST1NS, ST1N)

Adjusts the sensitivity temperature secondary characteristics inherent to a sensor and the AK8996. After performing the span voltage adjustment at 25ºC, use the register's sensitivity temperature drift coefficients for adjustment so that the absolute values of the AK8996's coefficient are matched to those of the sensor's coefficient. (See 1) Adjustment Procedure Description in "Functional Description" in the "Adjustment Sequence" section)

d-1) Sensitivity temperature drift 2nd order coefficient adjustment (Register names: ST2P, ST2N)

Address: 07 hex D[7:0]=EST2P[7:0], 08 hex D[7:0]=EST2N[7:0]

EST2P/N2[6:0]			Ratio	EST2P/N[7]:0	EST2P/N[7]:1	Comments
Dec	Hex	Bin	(%)	VDD: 5V / 3V	VDD: 5V / 3V	
0	00	0000000	100.000	0.00160000 /0.00080000	-0.00160000 /-0.00080000	Default
1	01	0000001	99.213	0.0015874 /0.0007937	-0.0015874 /-0.0007937	
.....						
16	10	0010000	87.402	0.00139842 /0.00069921	-0.00139842 /-0.00069921	
.....						
32	20	0100000	74.803	0.00119685 /0.000598425	-0.00119685 /-0.000598425	
.....						
64	40	1000000	49.606	0.0007937 /0.00039685	-0.0007937 /-0.00039685	
.....						
126	3E	1111110	0.7874	0.0000126 /0.000006299	-0.0000126 /-0.000006299	
127	3F	1111111	0.0	0.0	0.0	

d-2) Sensitivity temperature drift 1st order coefficient adjustment (Register names: ST1PS, ST1P, ST1NS, ST1N)

Address: 09 hex – 0A hex D[9:0]=EST1P[9:0], 0B hex – 0C hex D[9:0]=EST1N[9:0]

EST1P/N1[8:0]			Ratio	EST1P/N[9]:0	EST1P/N[9]:1	Comments
Dec	Hex	Bin	(%)	VDD: 5V / 3V	VDD: 5V / 3V	
0	000	000000000	100.000	0.32 /0.30	-0.32 /-0.30	Default
1	001	000000001	99.804	0.3194 /0.2994	-0.3194 /-0.2994	
…..						
64	030	001000000	87.4755	0.2799 /0.2624	-0.2799 /-0.2624	
…..						
128	040	010000000	74.9511	0.2398 /0.2249	-0.2398 /-0.2249	
…..						
256	100	100000000	49.9022	0.1597 /0.1497	-0.1597 /-0.1497	
…..						
510	1FE	111111110	0.1957	0.0006262 /0.0005871	-0.0006262 /-0.0005871	
511	1FF	111111111	0.0	0.0	0.0	

e) Input gain (G1/2) adjustment (Register name: ING)

Register for setting the total gain.
The input gain is adjusted according to the full-scale voltage of the pressure sensor.
Adjust the input gain so that the internal gain amp 2 output voltage is 400mV (@VDD: 5.0V) or less.

Address: 0D hex D[3:0]=EIG[3: 0]

EIG[2:0]			G1 Gain	Total Gain (times)		Comments
Dec	Hex	Bin	(times)	EIG[3]=0	EIG[3]=1	
0	0	000	2	20	40	Default
1	1	001	3	30	60	
2	2	010	4	40	80	
3	3	011	5	50	100	
4	4	100	6	60	120	
5	5	101	7	70	140	
6	6	110	8	80	160	
7	7	111	9	90	180	

f) BUF gain adjustment (Register name: BUFG)

Sets up the buffer circuit's gain.
After the level shift voltage is determined by the VOUT voltage, use EOG[2:0] for gain adjustment so that the detection maximum output is 4000mV (@VDD: 5.0V) with Vop (level shift voltage is uppermost or lowermost) or Vpp (± output centered on the level shift voltage).

Address: 0E hex D[2:0]=EOG[2:0]

EOG[2: 0]			Ratio	BUFF gain	Total	Comments
Dec	Hex	Bin	(%)	(times)	(times)	
0	0	000	100	2.0	25.00	Default
1	1	001	125	2.5	31.25	
2	2	010	150	3.0	37.50	
3	3	011	175	3.5	43.75	
4	4	100	200	4.0	50.00	

Note 1) Dec 5 to 7 are unavailable.

g) Pressure detector disable time (Register name: AS)

Sets up the pressure detector disable time.
In order for the pressure detector to accurately detect the pressure at power-up or standby exit ("L" to "H" at STBYN pin), it must wait until the VOUT pin output reference voltage is stabilized (See Section 3 Pressure Detection & Determination Circuit Operation at Power-Up and Standby Exit (STBYN pin "L" to "H") in "Functional Description").

g-1) Pressure detection valid (EINT1[1:0]=1h)
Address : 0F hex D[2:0]=EAS[2:0]

EAS[2: 0]			Pressure Detector Disable Time (msec)				Comments
Dec	Hex	Bin	fs: 100Hz	fs: 1kHz	fs: 2kHz	fs: 10kHz	
0	0	000	10	1.0	0.5	0.1	Default
1	1	001	10	1.0	0.5	0.2	
2	2	010	20	2.0	1.0	0.4	
3	3	011	60	6.0	3.0	0.8	
4	4	100	140	14.0	7.0	1.6	
5	5	101	300	30.0	15.0	3.1	
6	6	110	620	62.0	31.0	6.3	
7	7	111	1260	126.0	63.0	12.5	

g-2) Pressure detection & self diagnosis valid (EINT1[1:0]=3h)
Address : 0F hex D[2:0]=EAS[2:0]

EAS[2: 0]			Pressure Detector Disable Time (msec)				Comments
Dec	Hex	Bin	fs: 100Hz	fs: 1kHz	fs: 2kHz	fs: 10kHz	
0	0	000	10.2	1.2	0.7	0.3	Default
1	1	001	10.2	1.2	0.7	0.3	
2	2	010	40.2	4.2	2.2	0.6	
3	3	011	80.2	8.2	4.2	1.0	
4	4	100	160.2	16.2	8.2	1.8	
5	5	101	320.2	32.2	16.2	3.3	
6	6	110	640.2	64.2	32.2	6.5	
7	7	111	1280.2	128.2	64.2	12.7	

h) Pressure detector threshold (Register name: PTH)

Sets up the pressure detector's detection threshold values.
The detector threshold voltage varies ratiometrically with respect to the supply voltage. The thresholds for positive (+) and negative (-) comparators cannot be defined independently.

Address: 10 hex D[3:0]=EPT[3:0]

EPT[3:0]			Detection threshold (V)			Comments
Dec	Hex	Bin	Detection threshold	ex. VDD: 5V +ve side	ex. VDD: 5V -ve side	
-8	8	1000	0.50*VDD	2.50	2.50	
-7	9	1001	0.53*VDD	2.65	2.35	
-6	A	1010	0.56*VDD	2.80	2.20	
-5	B	1011	0.59*VDD	2.95	2.05	
-4	C	1100	0.62*VDD	3.10	1.90	
-3	D	1101	0.65*VDD	3.25	1.85	
-2	E	1110	0.68*VDD	3.40	1.60	
-1	F	1111	0.71*VDD	3.55	1.45	
0	0	0000	0.74*VDD	3.70	1.30	Default
1	1	0001	0.77*VDD	3.85	1.15	
2	2	0010	0.80*VDD	4.00	1.00	
3	3	0011	0.83*VDD	4.15	0.85	
4	4	0100	0.86*VDD	4.30	0.70	
5	5	0101	0.89*VDD	4.45	0.55	
6	6	0110	0.92*VDD	4.60	0.40	Note)
7	7	0111	0.95*VDD	4.75	0.25	Note)

Note) When EVD[0]:1 is used, setup of VDD: 2.2 to 3.6 V and EPT[3:0]:6h, 7h is prohibited.

i) Comparator hysteresis voltage adjustment for pressure detection (Register name: HYS)

The hysteresis voltage of the comparator for the pressure detector is set up.
The hysteresis voltage varies ratiometrically with respect to the supply voltage. The hysteresis voltages for positive (+) and negative (-) comparators cannot be defined independently.

Address: 11 hex D[2:0]=EHYS[2:0]

EHYS[2:0]			Hysteresis voltage (mV)		Comments
Dec	Hex	Bin	Hysteresis voltage	ex. VDD: 5V	
0	0	000	0.0200*VDD	-100.0	Default
1	1	001	0.0175*VDD	-87.5	
2	2	010	0.0150*VDD	-75.0	
3	3	011	0.0125*VDD	-62.5	
4	4	100	0.0100*VDD	-50.0	
5	5	101	0.0075*VDD	-37.5	
6	6	110	0.0050*VDD	-25.0	
7	7	111	0.0025*VDD	-12.5	

Note) See Functional Description **10) Note on the pressure detection circuit hysteresis voltage setup**

5.1.2) Reference Voltage Generator Register

j) VREF voltage adjustment (Register name: VREF)

Register for adjusting the AK8996 reference voltage. Perform an adjustment to attain the reference voltage of 1000 mV (See Recommended Connection Example for Components).
ΔVREF3/5 in the table below indicates a value varying with the setup values of the register. ΔVS3/5 represents the values of ΔVREF3/5 multiplied by two and four, respectively. The ratio is benchmarked to 1000mV (VREF ideal value) as 100% (Ratio = ΔVREF/1000[mV]*100[%]).

Address: 12 hex D[2:0]=EVR[2:0]

EVR[2:0]			Ratio	VDD: 3V, 3.3V mode		VDD: 5V		Comments
Dec	Hex	Bin	(%)	ΔVREF3 (mV)	ΔVS3 (mV)	ΔVREF5 (mV)	ΔVS5 (mV)	
-4	4	100	96	-40	-80	-40	-160	
-3	5	101	97	-30	-60	-30	-120	
-2	6	110	98	-20	-40	-20	-80	
-1	7	111	99	-10	-20	-10	-40	
0	0	000	100	0	0	0	0	Default
1	1	001	101	+10	+20	+10	+40	
2	2	010	102	+20	+40	+20	+80	
3	3	011	103	+30	+60	+30	+120	

k) IREF current adjustment (Register name: IREF)

Register for adjusting the AK8996 reference current. Perform an adjustment to attain the reference voltage of 20.0μA (See Recommended Connection Example for Components).
ΔIREF in the table below indicates a value varying with the setup values of the register.
ΔVIREF (= ΔIREF*47[kΩ]) is a voltage value varying with the external resistance (47kΩ) at the time of adjustment.
The ratio is benchmarked to 20.0μA (IREF ideal value) as 100% (Ratio = ΔIREF/20[μA]*100[%]).

Address: 13 hex D[3:0]=EIR[3:0]

EIR[3:0]			Ratio	ΔIREF	ΔVIREF	Comments
Dec	Hex	Bin	(%)	(μA)	(V)	
-8	8	1000	83.0	-3.40	-0.220	
-7	9	1001	84.7	-3.05	-0.203	
-6	A	1010	86.6	-2.68	-0.186	
-5	B	1011	88.5	-2.30	-0.168	
-4	C	1100	90.5	-1.89	-0.149	
-3	D	1101	92.7	-1.46	-0.129	
-2	E	1110	95.0	-1.00	-0.107	
-1	F	1111	97.4	-0.52	-0.084	
0	0	0000	100	0	-0.060	Default
1	1	0001	102.8	+0.55	-0.034	
2	2	0010	105.7	+1.14	-0.006	
3	3	0011	108.8	+1.77	+0.023	
4	4	0100	112.2	+2.45	+0.055	
5	5	0101	115.9	+3.17	+0.089	
6	6	0110	119.8	+3.96	+0.126	
7	7	0111	124.1	+4.81	+0.166	

l) OSC frequency adjustment (Register name: OSC)

Register for adjusting the AK8996 operation clock. Perform an adjustment to attain a frequency of 1.024kHz. Frequency Δf in the table below indicates a value varying with the setup values of the register. The ratio is benchmarked to 1.024kHz (OSC ideal value) as 100%
(Ratio = Frequency Δf/1024[kHz]*100[%]).

Address: 14 hex D[3:0]=EFR[3:0]

EFR[3:0]			Ratio	Frequency Δf	Comments
Dec	Hex	Bin	(%)	(kHz)	
-4	C	1100	80	-204.8	
-3	D	1101	85	-153.6	
-2	E	1110	90	-102.4	
-1	F	1111	95	-51.2	
0	0	0000	100	0	Default
1	1	0001	105	+51.2	
2	2	0010	110	+102.4	
3	3	0011	115	+153.6	
4	4	0100	120	+204.8	

Note 1) Hex 5 to B are unavailable.

m) VTMP voltage adjustment (Register name: VTMP)

Compensates the offset values for the AK8996's internal temperature sensor. Adjusts the values so that the difference between VTMP voltage and VREF voltage is close to 0 mV (If VREF is 1005mV, adjust so that VTMP is also 1005mV).
ΔVTMP in the table below indicates a value varying with the setup values of the register. The ratio is benchmarked to 1000mV (VREF ideal value) as 100% (Ratio = ΔVTMP/1000[mV]*100[%]).

Address: 15 hex D[5:0]=ETM[5:0]

ETM[5:0]			Ratio	ΔVTMP	Comments
Dec	Hex	Bin	(%)	(mV)	
-32	20	100000	-6.4	-64	
…..					
-16	32	110000	-3.2	-32	
…..					
-8	38	111000	-1.6	-16	
…..					
-4	3C	111100	-0.8	-8	
…..					
-1	3F	111111	-0.2	-2	
0	00	000000	0.0	0	Default
1	01	000001	+0.2	+2	
…..					
4	04	000100	+0.8	+8	
…..					
8	08	001000	+1.6	+16	
…..					
16	10	010000	+3.2	+32	
…..					
31	1F	011111	+6.2	+62	

5.1.3) Register Available to Users

n) User-writable data space (Register name: UE)

Free area (EEPROM) available to the user.

Address: 16 hex D[7:0]=EUE[7:0]

Name	Content	Address	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
UE	User-writable data	16 hex	EUE7	EUE6	EUE5	EUE4	EUE3	EUE2	EUE1	EUE0
Default			0	0	0	0	0	0	0	0

5.1.4) Mode Setup Register

o) Measurement mode (Register name: MM)

Sets up the measurement mode such as the selection of the AK8996 supply voltages and sampling frequencies.

Address: 17 hex D[5:0]= EAC[1:0], EVD[0], ESF[1:0], EBU[0]

D[5:0]	Symbol	Mode setup
D[5:4]	EAC[1:0]	Pressure judge circuit control register (adj. mode 1 CM1 D[6.5] prioritized)
00	NRM1	Pressure judge circuit functions valid (default)
01	APP	Pressure judge circuit invalid, fixed to positive pressure judge
10	APN	Pressure judge circuit invalid, fixed to negative pressure judge
11		Reserved
D[3]	EVD[0]	Supply voltage setup register
0	VD5	Supply voltage at 5V (default)
1	VD3	Supply voltage at 3V
D[2:1]	ESF[1:0]	Sampling frequency setup register
00	SF0	Sampling frequency 100 Hz (default)
01	SF1	Sampling frequency 1kHz
10	SF2	Sampling frequency 2kHz
11	SF3	Sampling frequency 10.24kHz
D[0]	EBU[0]	BUFFER Block ON/OFF register
0	BU0	BUFFER Block enable (default)
1	BU1	BUFFER Block disable

p) Pressure detection and self-diagnosis modes (Register name: INT)

Sets up the pressure detector and self-diagnosis circuit integrated with the AK8996.

Address: 18 hex D[5:0]= EOUT[0], EINT1[1:0], EINT2[0], EINT3[1:0]

D[7:0]	Symbol	Mode setup
D[7:6]		Reserved
D[5]	EOUT[0]	VOUT pin output status setup register when DET pin is high
0	VOUTE	Normal state (default)
1	VOUTD	VOUT pin Hi-Z output (indeterminate)
D[4:3]	EINT1[1:0]	Pressure detection & self-diagnosis setup register 1
00	INTOFF	Pressure detection & self-diagnosis turned off (default)
01	INTPON	Pressure detection valid
10	INTSON	Self diagnosis valid
11	INTON	Pressure detection & self diagnosis valid
D[2]	EINT2[0]	Pressure detection & self-diagnosis setup register 2
0	INT1OUT	Pressure detection valid (PTH pin reference is used) (default)
1	INT1IN	Pressure detection valid (Internal register reference is used)
D[1:0]	EINT3[1:0]	Pressure detection & self-diagnosis setup register 3
00	INT<	Detect pressure above threshold (default)
01	INT>	Detect pressure below threshold
10	INT><	Detect pressure either above or below threshold
11	INT<>	Detect pressure within a certain range

q) EEPROM batch write mode (Register name: AW)

Initializes the addresses in the EEPROM register map all at once or writes identical data. This address is not available in the EEPROM.

Address: 19 hex D[7:0]=EAW[7:0]

Name	Content	Address	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
AW	EEPROM batch write	19 hex	EAW7	EAW6	EAW5	EAW4	EAW3	EAW2	EAW1	EAW0

5.1.5) Output Reference Voltage and Pressure Judge Threshold Setup Register

r) Output reference voltage adjustment (Register names: LVR, LVF)

Rough adjustment should be performed first, followed by a fine adjustment for the output reference voltage. The content of the adjustment registers is shown here.

r-1) Output reference voltage rough adjustment (LVR)

The output reference voltage is coarsely tuned.
The adjustment voltage varies ratiometrically with respect to the supply voltage.

Address: 1B hex D[4:0]=ELVR[10:6]

ELVR[9: 6]			VO pin		VOUT pin		Comments
Dec	Hex	Bin	ELVR [10]=0 (*VDD)	ELVR [10]=1 (*VDD)	ELVR [10]=0 (*VDD)	ELVR [10]=1 (*VDD)	
0	0	0000	0.000	0.000	0.000*OG Note)	0.000*OG	Default
1	1	0001	-0.026	+0.026	-0.026*OG	+0.026*OG	
2	2	0010	-0.052	+0.052	-0.052*OG	+0.052*OG	
3	3	0011	-0.078	+0.078	-0.078*OG	+0.078*OG	
4	4	0100	-0.104	+0.104	-0.104*OG	+0.104*OG	
5	5	0101	-0.130	+0.130	-0.130*OG	+0.130*OG	
6	6	0110	-0.156	+0.156	-0.156*OG	+0.156*OG	
7	7	0111	-0.182	+0.182	-0.182*OG	+0.182*OG	
8	8	1000	-0.208	+0.208	-0.208*OG	+0.208*OG	
9	9	1001	-0.234	+0.234	-0.234*OG	+0.234*OG	
10	A	1010	-0.260	+0.260	-0.260*OG	+0.260*OG	
11	B	1011	-0.286	+0.286	-0.286*OG	+0.286*OG	
12	C	1100	-0.312	+0.312	-0.312*OG	+0.312*OG	
13	D	1101	-0.338	+0.338	-0.338*OG	+0.338*OG	
14	E	1110	-0.364	+0.364	-0.364*OG	+0.364*OG	
15	F	1111	-0.390	+0.390	-0.390*OG	+0.390*OG	

Note) OG: Indicates the value of the BUF gain (Register name: BUFG) being set.

r-2) Output reference voltage fine adjustment (LVF)

The output reference voltage is fine-tuned.
The adjustment voltage varies ratiometrically with respect to the supply voltage.

Address: 1C hex D[5:0]=ELVF[5:0]

ELVF[5:0]			VO pin		VOUT pin		Comments
Dec	Hex	Bin	ELVR [10]=0 (*VDD)	ELVR [10]=1 (*VDD)	ELVR [10]=0 (*VDD)	ELVR [10]=1 (*VDD)	
0	00	000000	0	0	0*OG	0*OG	Default
1	01	000001	-0.0005	0.0005	-0.0005*OG	0.0005*OG	
2	02	000010	-0.0010	0.0010	-0.0010*OG	0.0010*OG	
:	:	:	:	:	:	:	
30	1E	011110	-0.0150	0.0150	-0.0150*OG	0.0150*OG	
31	1F	011111	-0.0155	0.0155	-0.0155*OG	0.0155*OG	
32	20	100000	-0.0160	0.0160	-0.0160*OG	0.0160*OG	
:	:	:	:	:	:	:	
61	3D	111101	-0.0305	0.0305	-0.0305*OG	0.0305*OG	
62	3E	111110	-0.0310	0.0310	-0.0310*OG	0.0310*OG	
63	3F	111111	-0.0315	0.0315	-0.0315*OG	0.0315*OG	

Note) OG: The value of the BUF gain (Register name: BUFG) being set.

s) Pressure judge threshold adjustment (Register names: PJLV1, PJLV2)

The pressure judge threshold voltage is adjusted.
The adjustment threshold value varies ratiometrically with respect to the supply voltage.

Address: 1D hex D[1:0]=EPJLV[9:8], 1E hex D[7:0]=EPJLV[7:0]

EPJLV[9:0]			DET pin		Comments
Dec	Hex	Bin	VDD: 3V (mV)	VDD: 5V (mV)	
-450	23E	1000111110	1350	2250	
-450	23F	1000111111	1347	2245	
:	:	:	:	:	
-401	26F	1001101111	1203	2005	
-400	270	1001110000	1200	2000	
-399	271	1001110001	1197	1995	
:	:	:	:	:	
-1	3FF	1111111111	3	5	
0	0	0000000000	0	0	Default
1	1	0000000001	-3	-5	
:	:	:	:	:	
399	18F	0110001111	-1197	-1995	
400	190	0110010000	-1200	-2000	
401	191	0110010001	-1203	-2005	
:	:	:	:	:	
449	1C1	0111000001	-1347	-2245	
450	1C2	0111000010	-1350	-2250	

5.2) Description of Control Register (Volatile Memory)

a) Adjustment mode 1 (Register name: CM1)

This register is used to adjust the AK8996 reference voltage and pressure sensor's offset, span, offset temperature drift and sensitivity temperature drift including those of the AK8996.

Address: 00 hex D[6:0]=AC[1:0], AM[3:0], AEPEN[0]
(This is not a nonvolatile EEPROM, but a volatile register.)

D[7:0]	Symbol	Mode setup	Description
D[7]		Reserved	
D[6:5]	AC[1:0]	Pressure judge circuit control	Controls pressure judge circuit
00	NRM2	Normal operation	(Default)
01	APP	Positive pressure output	Pressure determination result is positive pressure.
10	APN	Negative pressure output	Pressure determination result is negative pressure.
11		Reserved	
D[4:1]	AM[3:0]	IC adjustment mode	Adjustment signal is output at the DET pin.
0000	NRM1	Normal operation	(Default)
0001	AVR	VREF adjustment	Outputs the VREF voltage
0010	AIR	IREF adjustment	Outputs the IREF current
0011	AFR	OSC adjustment	Outputs the OSC signal
0100	ATO	VTMP adjustment	Outputs the VTMP voltage Adjust this voltage so that it matches the VREF voltage at 25°C.
0101	ADT+	Positive judge threshold adjustment	Outputs internally set positive determination threshold value
0110	ADT-	Negative judge threshold adjustment	Outputs internally set negative determination threshold value
0111	AHY+	Positive hysteresis voltage	Outputs hysteresis voltage of the positive comparator
1000	AHY-	Negative hysteresis voltage	Outputs hysteresis voltage of the negative comparator
1001	APJ	Pressure judge threshold adjustment	Outputs output determination threshold value
1010-1111		Reserved	
D[0]	AEPEN[0]	EEPROM control mode	Controls the EEPROM operation
0	NRM0	Intermittent EEPROM operation	EEPROM normal operation (intermittent operation) (Default)
1	AEPD	EEPROM always on	EEPROM is always turned on. Always turn on when adjusting the module.

Note) When using the IC adjustment mode for setting the VTMP output, make an additional setup of AEPEN[0] = 1. In any other setup, the circuit is automatically always turned on.

b) Adjustment mode 2 (Register name: CM2)

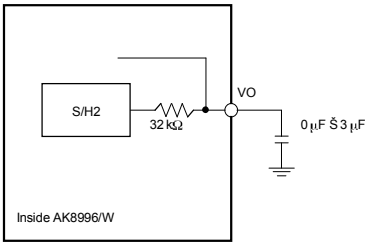
This register is used to adjust the AK8996 and pressure sensor's offset, span, offset temperature drift and sensitivity temperature drift.

Address: 01 hex D[5:0]=INSW[1:0], OTSW[0], STSW[0], 2ND[1:0]
(This is not a nonvolatile EEPROM, but a volatile register.)

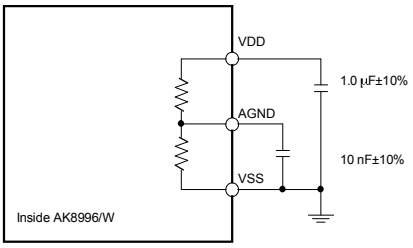
D[7:0]	Symbol	Mode setup	Description
D[7:6]		Reserved	
D[5:4]	INSW[1:0]	Input mode control	Controls the input mode
00	NRM6	Normal operation	Enables the sensor input (Default)
01	AIN0	Reference voltage mode	Internally generated AK8996 reference voltage fed to the input
10	AIN80	80mV voltage mode	Internally generated AK8996 80mV voltage fed to the input
11		Reserved	
D[3]	OTSW[0]	Temperature offset circuit control	Controls offset temperature drift adjustment circuit
0	NRM5	Enable	Enables temperature offset circuit (Default)
1	ASTOF	Disable	Disables temperature offset circuit
D[2]	STSW[0]	ST circuit control	Controls the ST circuit
0	NRM4	Enable	Enables the ST circuit (Default)
1	ASVOF	Disable	Disables the ST circuit
D[1:0]	2ND[1:0]	Secondary characteristic measurement	
00	NRM3	Normal operation	(Default)
01	A2ND	Secondary characteristic output	Outputs secondary characteristic (primary characteristic off)
10	A1ST	Primary characteristic output	Outputs primary characteristic (secondary characteristic off)
11		Reserved	

Recommended Connection Example for Components

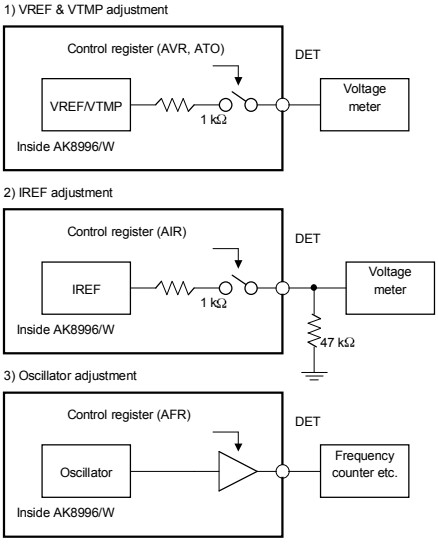
1) VO pin connection example



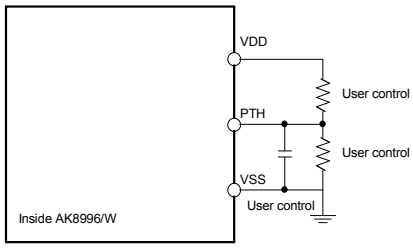
2) Power supply and AGND pin connection example



3) DET pin connection examples for adjustment

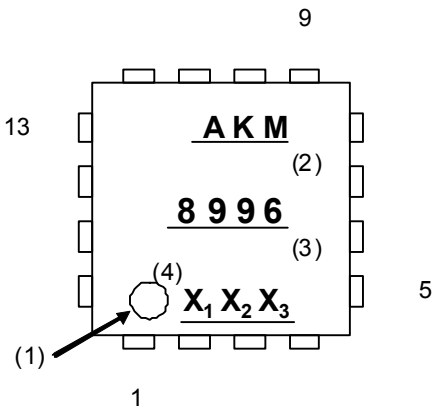


4) PTH pin connection example



Package Information

1. Marking



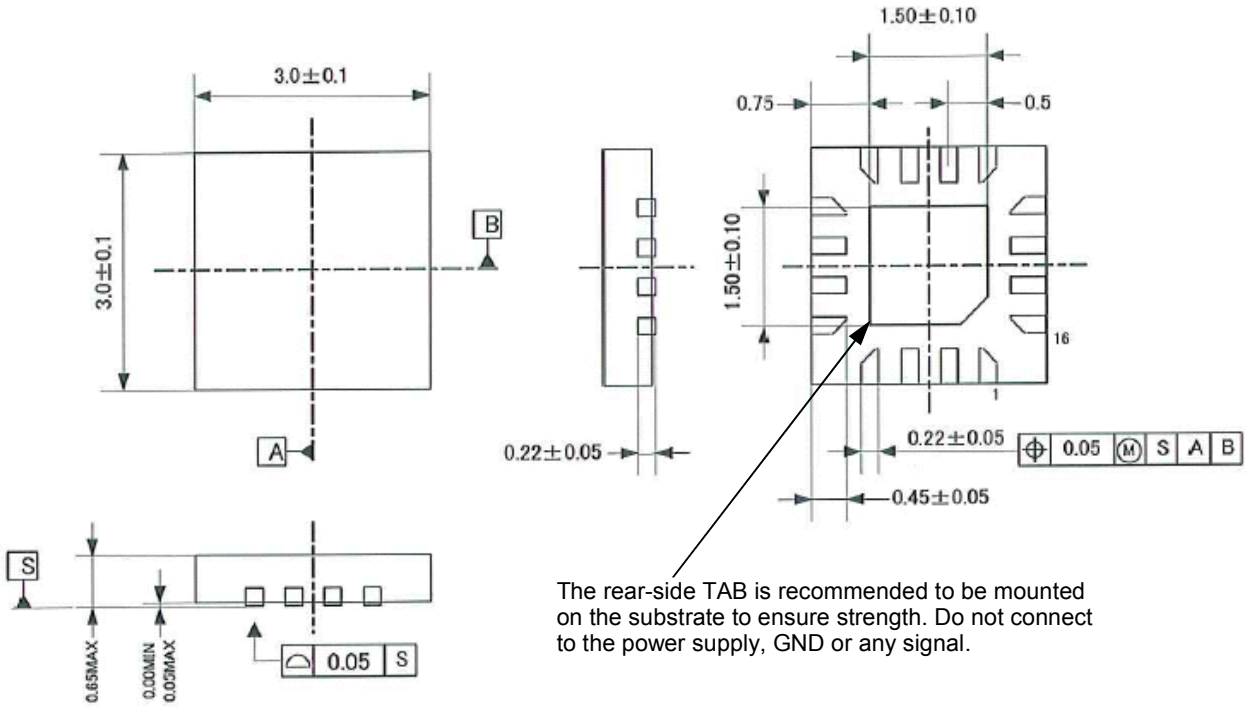
(1) Pin Number 1 indication mark

(2) Asahi-Kasei Microdevices Logo

(3) Part Number

(4) Date Code (3 digits)

2. External Dimensions



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