AK8856
NTSC/PAL Digital Video Decoder

General Description

The AK8856 decodes NTSC or PAL composite video signals into digital video data. The outputs are ITU-R BT. 601 level compatible Y, Cb and Cr signals. The decoded result is scaled to 601, VGA (interlaced output), CIF, QVGA, QCIF, rotated QVGA , or rotated CIF(progressive). Information including closed caption, VBID, and WSS are encoded in the video signal can be read out externally. The AK8856 is controlled by through an I^2C interface.

Features

- NTSC-M, NTSC-4.43 / PAL- B, D, G, H, I, N, Nc, M, 60 composite signal decoding process
- 10 Bit ADC (sampling at 24.5454MHz or 27MHz)
- Integrated PGA (0dB ~ 12dB)
- Automatic color control (ACC) function
- Adaptive automatic gain control (AGC) function
- 1D or 2D YC separation
- Phase compensation for PAL
- Output interface
    - ITU-R BT.656 output format (4:2:2 8-bit parallel output with EAV / SAV)
    - Camera interface
    - Interface with HD / VD / DVALID signals
- Closed caption decoding function (read by register setting)
- VBID (CGMS-A) decoding function (CRCC decode) (read by register setting)
- WSS decoding function (read by register setting)
- Macrovision signal detect function
- Power-down function
- 2-channel analog input selector
- I^2C control compatible
- Core voltage (AVDD, DVDD) 1.65 - 1.8V
- I/O voltage (PVDD) 1.65 - 3.3V (AK8856VG) / 1.65 - 3.6V (AK8856VN)
- Package: 41 FBGA 4.0mm x 4.0mm / 48 QFN 7.2mm x 7.2mm

* The output that meets the ITU-R BT.656 standard according to the fineness of the input signal might not be available.
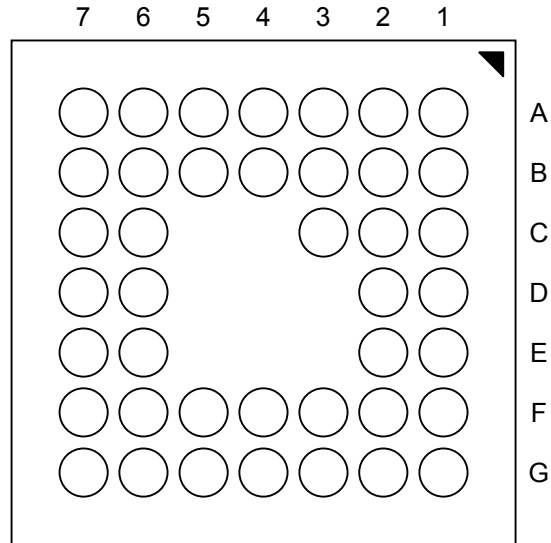
Block Diagram
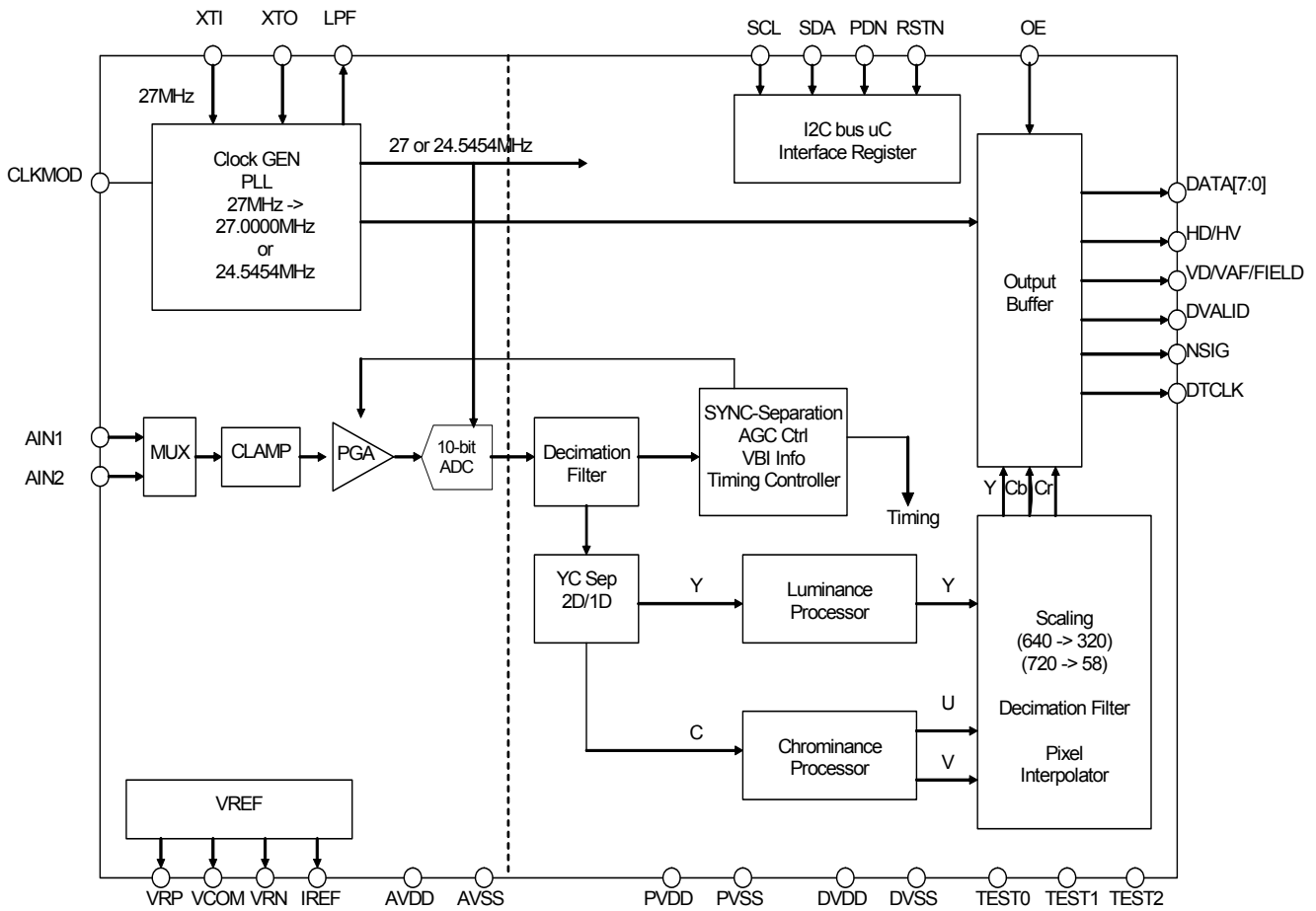
Ordering Guide

AK8856VG 41-pin FBGA
AK8856VN 48-pin QFN

Pin Layout Drawing

AK8856VG

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        7   6   5   4   3   2   1
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Bottom View

	1	2	3	4	5	6	7
A	NC	AIN1	VCOM	VRP	VRN	XTI	TEST0
B	AVDD	LPF	IREF	CLKMOD	DVSS	PDN	XTO
C	AIN2	AVSS	NC			RSTN	DVDD
D	DVDD	DVSS				SCL	OE
E	TEST2	NSIG				SDA	PVDD
F	VD/VAF*	DVALID	DATA7	DATA5	DATA3	DATA1	DTCLK
G	NC	HD/VD	DATA6	DATA4	DATA2	DATA0	TEST1

* "VD/VAF" is described "VD/VAF/FIELD" in this datasheet.

Top View

AK8856VN

Pin (Left)		Pin (Right)	
NC	1	36	NC
NC	2	35	TEST0
AVDD	3	34	PDN
AVSS	4	33	DVDD
AIN2	5	32	RSTN
DVSS	6	31	OE
DVDD	7	30	SCL
NSIG	8	29	PVDD
MACDET	9	28	SDA
DVALID	10	27	DTCLK
NC	11	26	TEST1
NC	12	25	NC

48 QFN (TOP VIEW)

Top pins (48–37): NC, AIN1, LPF, VCOM, IREF, VRP, VRN, CLKMOD, XTI, DVSS, XTO, NC

Bottom pins (13–24): NC, VD/VAF/FIELD, HD/HV, DATA7, DATA6, DATA5, DATA4, DATA3, DATA2, DATA1, DATA0, NC
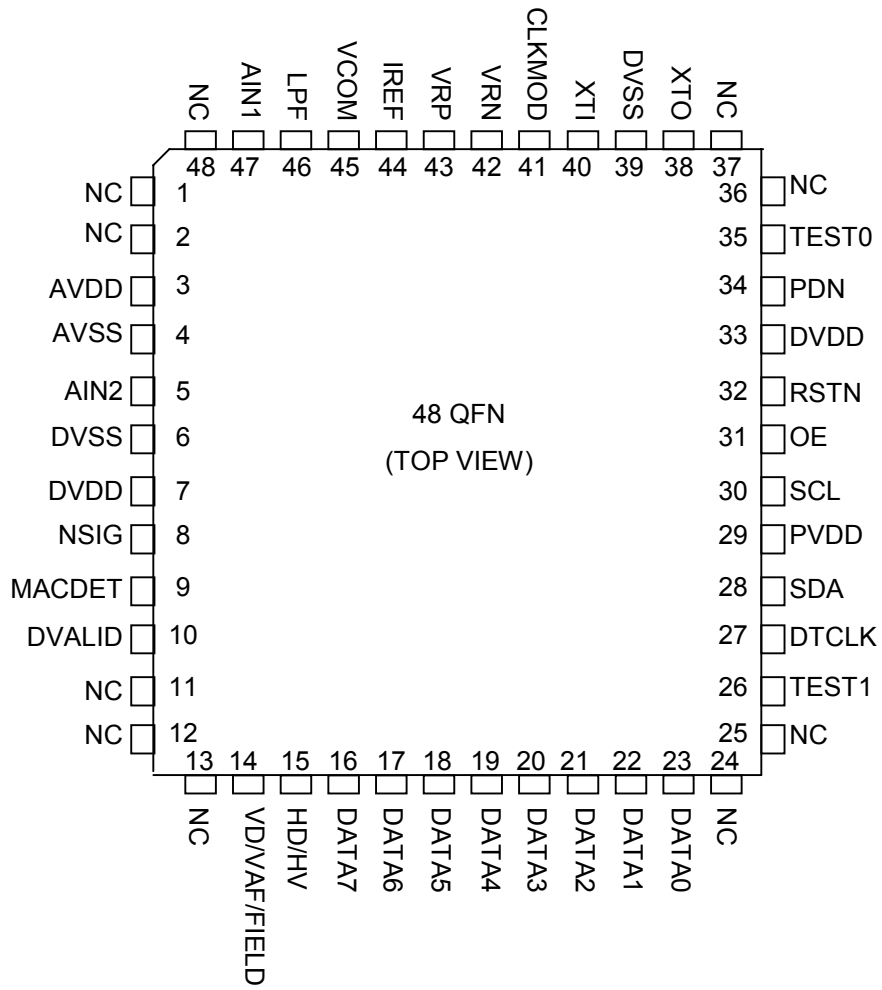
Pin Description

AK8856VG

Pin	Pin Name	A/D/P	I/O	Functional Outline
A6	XTI	D	I	Quartz crystal oscillator connection (tie to digital ground via a 22pF capacitor) - 27.00 MHz crystal oscillator should be used - input from 27.00 MHz crystal oscillator is connected to this pin
B7	XTO	D	O	Quartz crystal oscillator connection (tie to digital ground via a 22pF capacitor) - 27.00 MHz crystal oscillator should be used. - this pin outputs DVSS level when PDN = L. - when a crystal oscillator is not used, this pin can either be left open (NC) or connected to DVSS
B4	CLKMOD	D	I	Clock mode set: connect to either DVDD (high) or DVSS (low) - Low setting: crystal oscillator is used - High setting: external clock source is used
D7	OE	P	I	Output enable - L : digital output pins are at high-Z - H : data is available for output - Hi-Z input on OE pin is prohibited
E6	SDA	P	I/O	I^{2}C data - this pin is pulled-up to PVDD - Hi-Z input is allowed when PDN is low - SDA input is not accepted during reset operation
D6	SCL	P	I	I^{2}C clock input - an input level below PVDD should be input - Hi-Z input is allowed when PDN is low - SCL input is not accepted during reset operation
C6	RSTN	P	I	Reset signal input - Hi-Z input to this pin is prohibited - L: reset - H: normal operation
B6	PDN	P	I	Power-down control - Hi-Z input to this pin is prohibited - L: power-down - H: normal operation
F7	DTCLK	P	I/O	Data clock for output interface - output state is separately controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
F3	DATA7	P	I/O	Data output (MSB) - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
G3	DATA6	P	O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
F4	DATA5	P	I/O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
G4	DATA4	P	O	Data output pin - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)

F5	DATA3	P	I/O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
G5	DATA2	P	O	Data output pin - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
F6	DATA1	P	I/O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
G6	DATA0	P	O	Data output pin (LSB) - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
G2	HD/HV	P	O	HD/HV timing signal output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
F1	VD/VAF /FIELD	P	I/O	VD/VAF/FIELD timing signal output - selection of VD/VAF signal output and FIELD signal output is determined by register setting - in camera I/F mode, VAF signal is always output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
F2	DVALID	P	O	Valid video interval - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
E2	NSIG	P	O	Indicates synchronization condition with input signal - L : synchronized with input signal - H : no signal input or out of synchronization - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1
E1	TEST2	P	I/O	Reserved – leave floating
A2	AIN1	A	I	Analog input pin (1) ; if not used, leave floating
C1	AIN2	A	I	Analog input pin (2) ; if not used, leave floating
B3	IREF	A	I/O	Reference current setting - connect this pin to analog ground through a 6.8kΩ resistor (≤1% accuracy) - this pin goes to high-Z in power-down mode (no high-Z test is performed in production test)
A5	VRN	A	I/O	Internal negative reference voltage for ADC - connect this pin to analog ground through a 0.1uF or larger capacitor - this pin may go to high-Z in power-down mode (no high-Z test is performed in production test) - do not use this as a reference voltage source for external circuitry
A4	VRP	A	I/O	Internal positive reference voltage for ADC - connect this pin to analog ground through a 0.1uF or larger capacitor - there is a case when this pin becomes Hi-Z output at power-down (no Hi-Z test is performed in mass-production test) - do not use this pin as a reference voltage source for external circuit.
A3	VCOM	A	I/O	Internal common voltage for AD converter - connect this pin to analog ground via a 0.1 uF or larger capacitor. - there is case when this pin becomes Hi-Z output at power-down (no Hi-Z test is performed in mass-production test). - do not use this pin as a reference voltage source for external circuit.
B2	LPF	A	I/O	I/O for analog test - connect this pin to AVSS for normal operation
B1	AVDD	A	P	Analog power supply
C2	AVSS	A	G	Analog ground
C7, D1	DVDD	D	P	Digital power supply
B5,	DVSS	D	G	Digital ground pins

D2				
E7	PVDD	P	P	Power supply for interface - interface power supply for DTCLK, OE, PDN, RSTN, DATA[7:0], HD/HV, VD/VAF/FIELD, NSIG, DVALID, SDA, SCL.
A7	TEST0	P	I	Test mode 0 - connect this pin to DVSS (internally pulled-down)
G7	TEST1	P	I	Test mode 1 - connect this pin to DVSS (internally pulled-down)
A1, G1, C3	NC			No connection – leave floating - Reserved for AKM testing

A/D/P A: AVDD, D: DVDD, P: PVDD
I/O I: Input pin, O: Output pin, I/O Input/Output pin

AK8856VN

Pin	Pin Name	A/D/P	I/O	Functional Outline
1	NC			No connection – leave floating - Reserved for AKM testing
2	NC			No connection – leave floating - Reserved for AKM testing
3	AVDD	A	P	Analog power supply
4	AVSS	A	G	Analog ground
5	AIN2	A	I	Analog input pin (2) ; if not used, leave floating
6	DVSS	D	G	Digital ground pins
7	DVDD	D	P	Digital power supply
8	NSIG	P	O	Indicates synchronization condition with input signal - L : synchronized with input signal - H : no signal input or out of synchronization - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1
9	TEST2	P	I/O	Reserved – leave floating
10	DVALID	P	O	Valid video interval - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
11	NC			No connection – leave floating - Reserved for AKM testing
12	NC			No connection – leave floating - Reserved for AKM testing
13	NC			No connection – leave floating - Reserved for AKM testing
14	VD/VAF /FIELD	P	I/O	VD/VAF/FIELD timing signal output - selection of VD/VAF signal output and FIELD signal output is determined by register setting - in camera I/F mode, VAF signal is always output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
15	HD/HV	P	O	HD/HV timing signal output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
16	DATA7	P	I/O	Data output (MSB) - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
17	DATA6	P	O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
18	DATA5	P	I/O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
19	DATA4	P	O	Data output pin - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
20	DATA3	P	I/O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
21	DATA2	P	O	Data output pin - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)

22	DATA1	P	I/O	Data output - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
23	DATA0	P	O	Data output pin (LSB) - output state is controlled by combinations of RSTN/PDN/OE pin settings (note 1)
24	NC			No connection – leave floating - Reserved for AKM testing
25	NC			No connection – leave floating - Reserved for AKM testing
26	TEST1	P	I	Test mode 1 - connect this pin to DVSS (internally pulled-down)
27	DTCLK	P	I/O	Data clock for output interface - output state is separately controlled by combinations of RSTN/PDN/OE pin settings (note 1) - this pin is used as an I/O pin in test mode
28	SDA	P	I/O	I^2C data - this pin is pulled-up to PVDD - Hi-Z input is allowed when PDN is low - SDA input is not accepted during reset operation
29	PVDD	P	P	Power supply for interface - interface power supply for DTCLK, OE, PDN, RSTN, DATA[7:0], HD/HV, VD/VAF/FIELD, NSIG, DVALID, SDA, SCL.
30	SCL	P	I	I^2C clock input - an input level below PVDD should be input - Hi-Z input is allowed when PDN is low - SCL input is not accepted during reset operation
31	OE	P	I	Output enable - L : digital output pins are at high-Z - H : data is available for output - Hi-Z input on OE pin is prohibited
32	RSTN	P	I	Reset signal input - Hi-Z input to this pin is prohibited - L: reset - H: normal operation
33	DVDD	D	P	Digital power supply
34	PDN	P	I	Power-down control - Hi-Z input to this pin is prohibited - L: power-down - H: normal operation
35	TEST0	P	I	Test mode 0 - connect this pin to DVSS (internally pulled-down)
36	NC			No connection – leave floating - Reserved for AKM testing
37	NC			No connection – leave floating - Reserved for AKM testing
38	XTO	D	O	Quartz crystal oscillator connection (tie to digital ground via a 22pF capacitor) - 27.00 MHz crystal oscillator should be used. - this pin outputs DVSS level when PDN = L. - when a crystal oscillator is not used, this pin can either be left open (NC) or connected to DVSS
39	DVSS	D	G	Digital ground pins
40	XTI	D	I	Quartz crystal oscillator connection (tie to digital ground via a 22pF capacitor) - 27.00 MHz crystal oscillator should be used

41	CLKMOD	D	I	- input from 27.00 MHz crystal oscillator is connected to this pin Clock mode set: connect to either DVDD (high) or DVSS (low) - Low setting: crystal oscillator is used - High setting: external clock source is used
42	VRN	A	I/O	Internal negative reference voltage for ADC - connect this pin to analog ground through a 0.1uF or larger capacitor - this pin may go to high-Z in power-down mode (no high-Z test is performed in production test) - do not use this as a reference voltage source for external circuitry
43	VRP	A	I/O	Internal positive reference voltage for ADC - connect this pin to analog ground through a 0.1uF or larger capacitor - there is a case when this pin becomes Hi-Z output at power-down (no Hi-Z test is performed in mass-production test) - do not use this pin as a reference voltage source for external circuit.
44	IREF	A	I/O	Reference current setting - connect this pin to analog ground through a 6.8kΩ resistor (≤1% accuracy) - this pin goes to high-Z in power-down mode (no high-Z test is performed in production test)
45	VCOM	A	I/O	Internal common voltage for AD converter - connect this pin to analog ground via a 0.1 uF or larger capacitor. - there is case when this pin becomes Hi-Z output at power-down (no Hi-Z test is performed in mass-production test). - do not use this pin as a reference voltage source for external circuit.
46	LPF	A	I/O	I/O for analog test - connect this pin to AVSS for normal operation
47	AIN1	A	I	Analog input pin (1) ; if not used, leave floating
48	NC			No connection – leave floating - Reserved for AKM testing

A/D/P A: AVDD, D: DVDD, P: PVDD
I/O I: Input pin, O: Output pin, I/O Input/Output pin

Note 1) Output pin conditions are determined by setting PDN and OE pins

OE	PDN	RSTN	Output1*	Output2*
L	x	x	Hi-Z output	L output
H	L	x	L output	L output
H	H	L	L output	L output
		H	Dataout(*1)	Dataout(*1)

Output1*: DATA[7:0], HD/HV, VD/VAF/FIELD, DVALID, DTCLK
Output2*: NSIG, MACDET
Output pin conditions immediately following power-on are indeterminate, except at OE = "L"
(*1) With no analog input signal, black level data (Y = 0x10, Cb/Cr = 0x80) is output in decoder mode operation

Electrical Characteristics

(1) Absolute Maximum Ratings

Parameter	Min	Max	Units	Note
Supply voltage DVDD, AVDD PVDD	-0.3 -0.3	2.3 4.3	V V	
Analog input voltage (VinA)	-0.3	AVDD + 0.3	V	
Clock input voltage (Vckin)	-0.3	DVDD + 0.3	V	XTI
Digital Input voltage 1 (VinD)	-0.3	DVDD + 0.3	V	CLKMOD
Digital input voltage 2 (VinP)	-0.3	PVDD + 0.3	V	OE,PDN,RSTN, SDA, SCL
Input current (Iin)	-10	10	mA	
Storage temperature	-40	125	°C	

Power supply voltages are values where each ground pin (DVSS = AVSS = PVSS) is at 0V

All power supply ground pins (DVSS, AVSS and PVSS) should be at the same potential

When connecting digital output pins (DTCLK,DATA[7:0], HD/HV,VD/VAF/FIELD, NSIG, DVALID) to the data bus, the data bus operating voltage must be within the input pin voltage range as described above

(2) Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units	Conditions
Supply voltage * AVDD,DVDD	1.65	1.8	2.0	V	AVDD=DVDD
Interface power supply PVDD	1.65	1.8	3.3 (AK8856VG) 3.6 (AK8856VN)	V	PVDD>=DVDD
Operating temperature (Ta)	-30		85	°C	AK8856VG
	-40				AK8856VN

* Power supply voltages are values where each ground pin (PVSS = AVSS = PVSS) is at 0 V (voltage reference)

All power supply ground pins (DVSS, AVSS and PVSS) should be at the same potential

(3) DC Characteristics

operating voltage: PVDD =DVDD1.65~2.0V, temperature -30~+85°C(AK8856VG), -40~+85°C(AK8856VN)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Digital input H voltage (VIH)	VIH	0.8PVDD			V	
Digital input1 L voltage (VIL)	VIL			0.2PVDD	V	
Digital input leak current	IL			±10	uA	
Digital output H voltage (VOH)	VOH	0.7PVDD				IOH = -600uA
Digital output L voltage (VOL)	VOL			0.3PVDD		IOL = 1mA
I2C (SDA) L output	VOLC			0.3PVDD	V	IOLC = 3mA

Digital output pins refer to DTCLK, DATA[7:0], HD/HV, VD/VAF/FIELD, NSIG, DVALID pin outputs in general terms

Digital input pins refer to OE, PDN, RSTN, SCL, SDA pin outputs in general terms

SDA output is not included as a digital output pin unless otherwise noted

(4) Analog Characteristics (AVDD = 1.8 V, temperature 25°C)

Selector Clamp

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Maximum input range	VIMX	0	0.64	0.75	V_{PP}	PGA_GAIN (minimum setting)
Clamp current	CLPI UDCLP		120 40		uA	FINE clamp (default) UP/DN clamp (default)

PGA

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Resolution			7		bit	
Minimum gain	GMN		0		dB	
Maximum gain	GMX		12		dB	
Gain step	GST		0.094	0.235	dB	

A/D Converter

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Resolution	RES	10			bits	
Operating clock frequency	FS		24.545427		MHz	
Integral non-linearity error	INL		2.0	4.0	LSB	fs=27MHz, PGA_GAIN (default)
Differential non-linearity error	DNL		1.0	2.0	LSB	fs=27MHz, PGA_GAIN (default)
S/N	SN		50		dB	fin=1MHz, fs=27MHz PGA_GAIN (default)
S/(N+D)	SND		48		dB	fin=1MHz, fs=27MHz PGA_GAIN (default)
ADC internal common voltage	VCOM		0.8		V	
ADC internal positive-side VREF voltage	VRP		1.0		V	
ADC internal negative-side VREF voltage	VRN		0.6		V	

AAF (Anti Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Passband ripple	Gp	-1		1	dB	6MHz
Stopband attenuation	Gs		-24	-12	dB	27MHz

(5) Current consumption

(DVDD = AVDD = PVDD = 1.8V, Ta = -30 ~ +85°C (AK8856VG), -40 ~ +85°C(AK8856VN))

Parameter	Symbol	Min	Typ	Max	Units	Conditions

Operating power supply current
Total current consumption
    Analog section:
    Digital section:
    Interface section:
			33
			17
			12
			4
				43	mA
					mA
					mA
					mA
						Note1)
						
						Crystal oscillator connection
						Load capacitor CL=15pF

Power-down current
(digital + analog)
    Analog section:
    Digital section:
    Interface section:
			<=1
			<=1
			<=1
			<=1
				20	uA
					uA
					uA
					uA	

Note 1) Input / Output signal : Measured with 100 % Color Bar signal.

Decoder power supply current is measured in 601 output mode (internal clock operation at 27MHz) and 2D YC Separation Mode
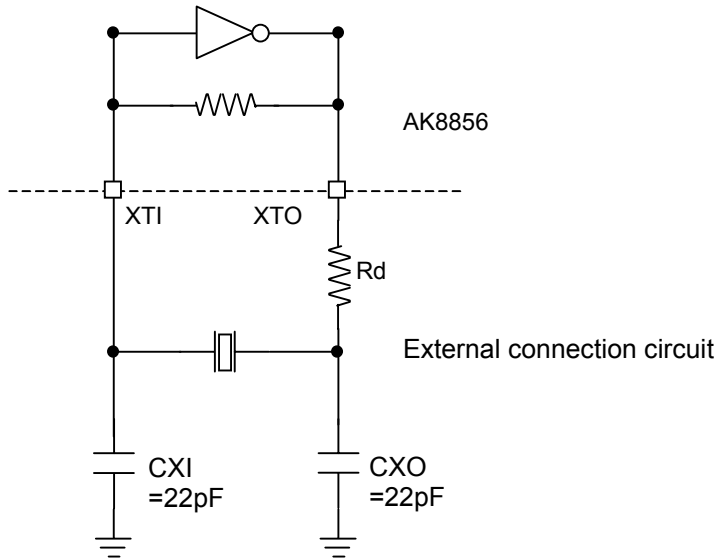
(6) Quartz Crystal Oscillator circuit

Quartz crystal resonator and externally connecting load capacitance

< Ta = -30 ~ +85°C (AK8856VG), -40 ~ +85°C(AK8856VN) >

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Oscillating frequency	f_0		27.000		MHz	
Frequency accuracy	Delta f / f			+/-100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	note1
Parallel capacitance	C0			0.85	pF	
XTI pin externally connecting load capacitance	CXI		22		pF	
XTO pin externally connecting load capacitance	CXO		22		pF	

note 1) effective equivalent resistance is generally given as: $Re = R1 \times (1 + CO / CL)^2$,where R1 = serial equivalent resistance of crystal oscillator and CO = parallel capacitance of crystal oscillator

Circuit connection example

AK8856

XTI   XTO

Rd

External connection circuit

CXI
=22pF

CXO
=22pF

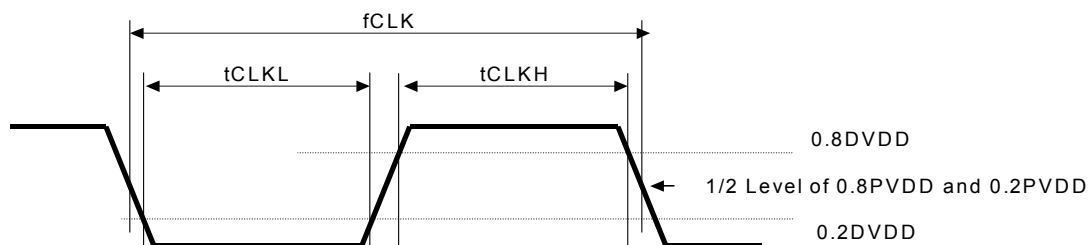Note) Refer to the quartz crystal oscillator section for the value of the limiting resistor Rd

AC Timing

(DVDD = PVDD = 1.65V, Ta at -30 ~ +85°C(AK8856VG), -40 ~ +85°C(AK8856VN))
Load condition: CL = 15pF

(1) CLK
Clock conditions (CLKMOD = 1: external clock mode)

Parameter	Symbol	Min	Typ	Max	Unit
CLK	fCLK		27.00		MHz
CLK duty ratio	pCLKD	40		60	%
Frequency stability				±100	ppm

(2) Clock specification (DTCLK output)

Parameter	Symbol	Min.	Typ.	Max	Unit	Operating mode
DTCLK	fDTCLK		12.2727		MHz	QVGA / Rotate QVGA / Rotated CIF
			13.5			CIF(PAL), QCIF
			24.5454			VGA
			27			CIF(NTSC)/601

(3) Output Data Timing

All output signals except for NSIG and TESTFLG, and MACFLG outputs

CLKINV-bit = 0(Register Setting)

DTCLK — 1/2PVDD

tDS   tDH

Output signal — 0.7PVDD
0.3PVDD

CLKINV-bit=1(Register Setting)

DTCLK — 1/2PVDD

tDS   tDH

Output signal — 0.7PVDD
0.3PVDD
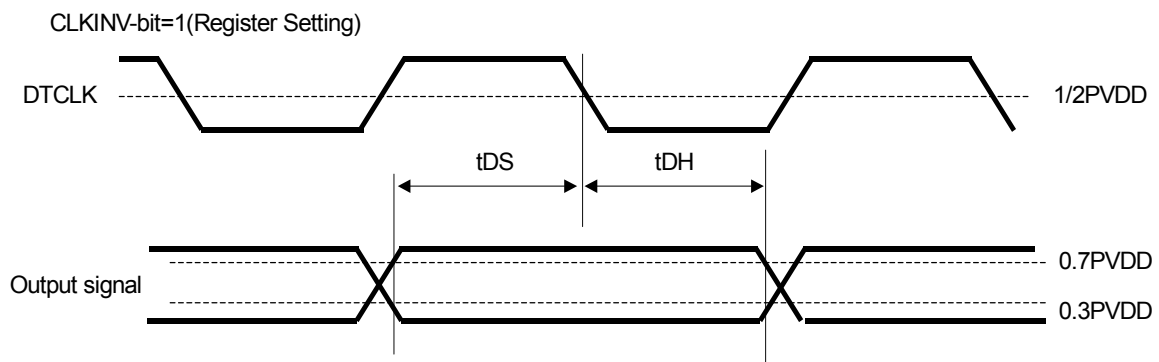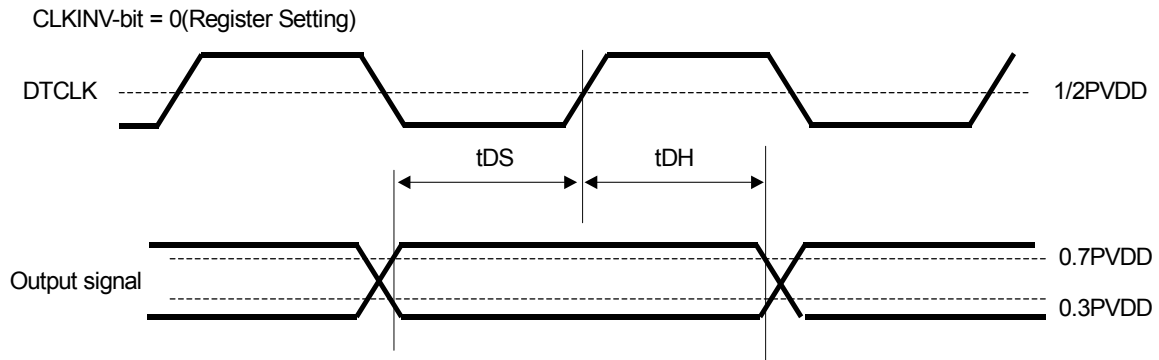
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output Data Setup Time	tDS	10			nsec	
Output Data Hold Time	tDH	10			nsec	

(4) Reset Timing (Register reset)
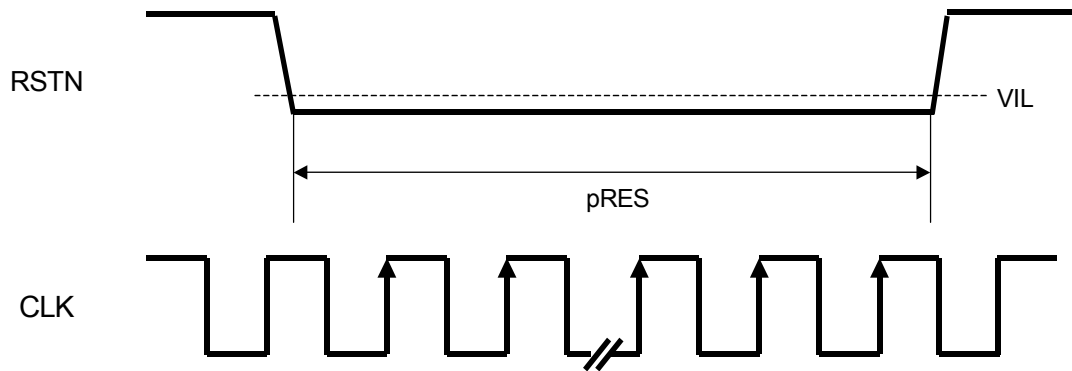
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
RSTN pulse width	pRES	100			CLK	Rising Clock Edge

Note) clock input is required for reset. Set RSTN pin low after the clock is present.

(5) Power-down sequence and reset sequence after power-down release

Activate reset for longer than 1024 clock cycles before setting PDN (PDN to low)
Activate reset after PDN release (PDN to high)
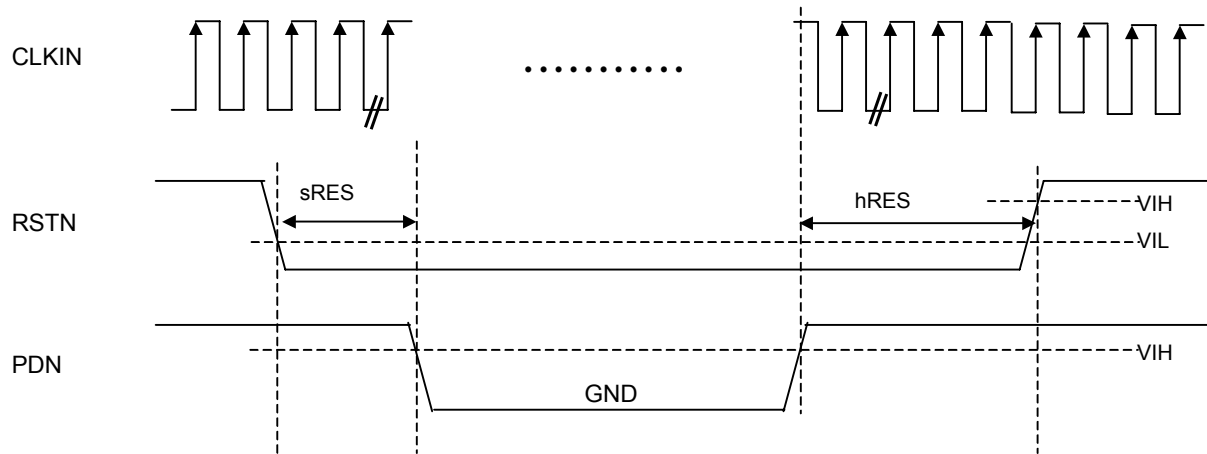
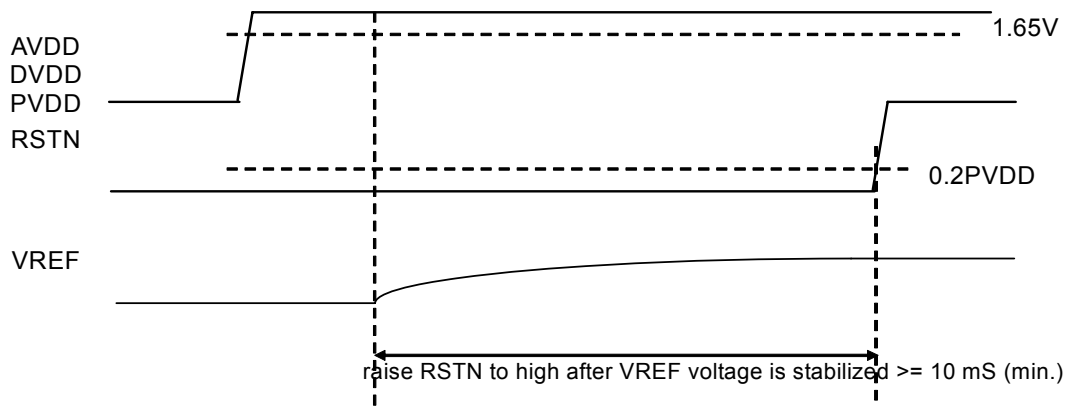| Parameter	Symbol	Min	Typ	Max	Unit
RSTN pulse width	sRES	1024			SYSCLK
Time from PDN to high to RSTN to high	hRES	10			msec

During power-down, all control signals must be connected to either the selected power supply or ground, and <u>not</u> to ViH / ViL levels.
When turning off power supplies (AVDD / DVDD) other than PVDD, place the AK8856 into power down mode.

Note) Clock input is required for reset operation

(6) Power-On-Reset

At power-on, reset must be enabled until the analog reference voltage and current are stabilized.

Power-on operation must be initiated with either simultaneous power-on of PVDD / AVDD / DVDD or PVDD first and then AVDD / DVDD
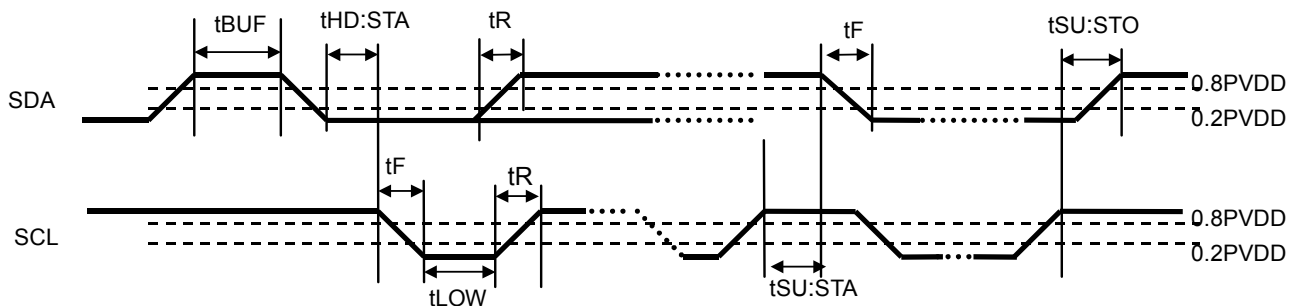

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
RESETN pulse width	pRES_PON	10			msec	

Note) clock input is required for reset operation

(7) I²C bus input / output timing
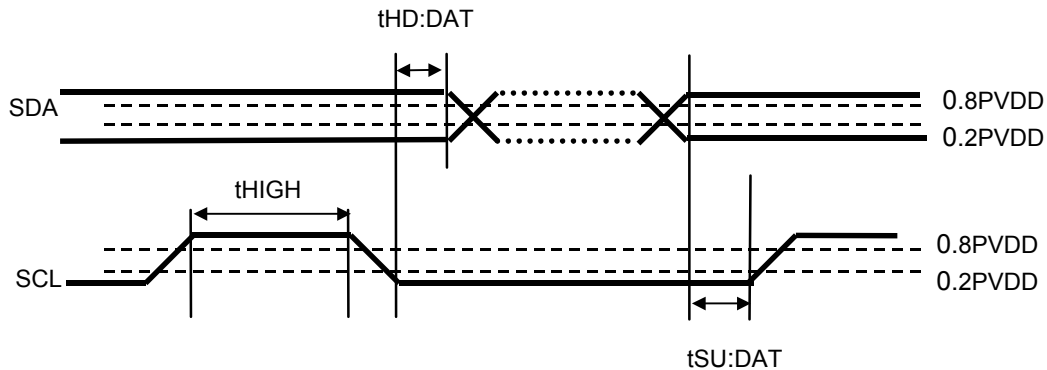**(DVDD = PVDD 1.65 V ~ 2.0V, Ta = -30 ~ +85°C(AK8856VG), -40 ~ +85°C(AK8856VN))**

(7-1) Timing 1

Parameter	Symbol	Min	Max	Unit
Bus free time	tBUF	1.3		usec
Hold time (start condition)	tHD:STA	0.6		usec
Clock pulse low time	tLOW	1.3		usec
Input signal rise time	tR		300	nsec
Input signal fall time	tF		300	nsec
Setup time (start condition)	tSU:STA	0.6		usec
Setup time (stop condition)	tSU:STO	0.6		usec

I^2C bus related timing is established by the I^2C Bus Specification, and it is not limited by the device performance. For details, please refer to the I^2C Bus Specification.

(7-2) Timing 2

tHD:DAT

SDA   0.8PVDD
                                                                                        0.2PVDD

tHIGH

SCL   0.8PVDD
                                                                                        0.2PVDD

tSU:DAT

Parameter	Symbol	Min	Max	Unit
Data Setup Time	tSU:DAT	100 (note1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (note2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

note 1) when operating in I^2C Bus Standard mode, tSU:DAT ≥ 250 ns must be met
note 2) when the AK8856 is used in a bus interface where tLOW is not extended (at minimum specification of tLOW), this condition must be met.

Functional Outline

(1) Clock
  Connect a 27MHz crystal or a 27MHz clock source.
  Internal operating clock rates are:
        24.5454 MHz for VGA / QVGA / rotated QVGA size / rotated CIF size outputs
        27 MHz   for 601 pixel mode, CIF / QCIF

  24.5454 MHz clock is generated by an internal PLL.
  Although the clock is asynchronous with the input signal, vertical position is aligned since the Digital Pixel
  Interpolator is integrated.

(2) Analog Interface
  The AK8856 accepts composite video signals.

(3) Input Signal
  NTSC-M, PAL-B, -D, -G, -H, -I compatible composite video signals are accepted as input signals.

(4) Analog Input Signal Processing
  An anti-aliasing filter is integrated.
        PGA   0 dB ~ 12 dB (approximately 0.1 dB / step)
        ADC   operates at either 24.5454 MHz or 27.00 MHz

(5) Clamp Processing
  Sync-tip clamping is processed in the analog block and digital pedestal clamping is processed in the digital
  signal processing block.

(6) Adaptive AGC Function
  Based on the difference between the sync-tip level and the pedestal level, the input signal value is corrected
  to a proper level.
  A video signal level gain adjust function is applied if only the video signal is larger.

(7) ACC Function
  Based on the color burst level, the input color signal level is corrected to a proper level.

(8) Y / C Separation Function
  Choice of either primary Y / C separation or two dimensional Y / C separation is available.
  Mode setting of Y / C separation is done through register settings.

(9) Pixel Interpolator
  The AK8856 has an integrated Digital Pixel Interpolator to align the output pixels' vertical position. No
  line-synchronized clock is required.

(10) Picture Quality Adjustment Function
  Adjustments of contrast, brightness, color hue and color saturation levels are available.

(11) Output Interface
  Outputs are ITU-R BT.601 compatible signal levels (with limit ON / OFF)
  Output formats include:
  - Camera interface
  - ITU-R BT.656-like output*
  - Active video region is indicated by HD / VD (FIELD) / DVALID
    * With SAV/EAV, 27MHz   The number of clocks from EAV to SAV becomes irregular.

(12) Variable Frame-Rate Function
    * Frame rates of 30 / 15 / 7.5 frames per second are selectable for NTSC video
    * Frame rates of 25 / 12.5 / 6.75 frames per second are selectable for PAL video

 (13) Output Picture Size
  - VGA   (640 X 480 - interlaced output)
  - QVGA   (320 X 240)
  - CIF   (352 X 288)
  - QCIF   (176 X 144)
  - 601   (NTSC: 720 X 480 / PAL: 720 X 576 - interlaced output)
  - rotated QVGA   (240 X 180)
  - rotated CIF   (288 X 216)

(14) Other Functions
  - Black level signal (Y = 16, Cb / Cr = 128) is output in self-operating mode when no input signal is present
    (Blue back output is also possible)
  - No signal input detection function
  - I^2C host interface
  - Power-down function
  - Decoding function for closed caption, VBID (CGMS-A 525 line), WSS signal (625 line signal). CRCC added
    to CGMS-A is decoded by the AK8856.

Input Signal

The AK8856 is designed to decode the following video signals:
> - NTSC
> - PAL-B, -D, -G, -H, -I.

Those input signal types are set by **Input Video Standard Register (R/W) [Sub Address 0x00]**.

The input signal is converted into digital code as follows:

Clamp Block ---- Anti-aliasing Filter ---- PGA Block ---- ADC Block

Then the digitized signal is processed in digital block.

Settings of the **Input Video Standard Register (R/W) [Sub Address 0x00]** is described here.
This register sets the input signal attributes.

Sub Address 0x00   **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	AINSEL	VLF	VCEN	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

[VSCF1 : VSCF0]-bit
The input signal sub-carrier frequency is set by the [VSCF1 : VSCF0] bits.

[VSCF1:VSCF0]-bit	Sub-carrier frequency (MHz)	Conditions
[00]	3.57954545	NTSC
[01]	3.57561188	
[10]	3.582054	
[11]	4.43361875	PAL-B,D,G,H,I

[VCEN]-bit
The input signal Color Encoding system is set by the [VCEN]-bit.

[VCEN]-bit	Color Encoding system	Conditions
0	NTSC	
1	PAL	

[VLF]-bit
The number of lines per each Frame of the input signal is set by the [VLF] bit.

[VLF]-bit	Number of lines	Conditions
0	525 lines	
1	625 lines	

[AINSEL]-bit
The input signal is selected by the [AINSEL] bit.

[AINSEL]-bit	Input signal	Conditions
0	AIN1 input is selected	
1	AIN2 input is selected	

PGA (Programmable Gain Amp)

A PGA (Programmable Gain Amp) is integrated into the input stage of the AK8856.
The PGA is adjustable from 0 dB to 12 dB, with gain steps of 0.1 dB / step.
The input signal is attenuated by 50% by a resistor divider.
The PGA setting is determined by **PGA Control Register (R/W) [Sub Address 0x05].**

By writing a "1" to the **Control 2 Register (R/W) [Sub Address 0x04]** AGC-bit, the AGC function is enabled.
Since the setting of the AGC is written by the **PGA Control Register (R/W) [Sub Address 0x05]**, the AGC value can be read through this register (manual setting of the PGA is invalid).
When the AGC function is disabled, manual setting of the PGA gain is allowed.
Bit allocation of **PGA Control Register** is as follows:

[PGA Control Register]
Sub Address 0x05   **Default Value: 0x15**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA6	PGA5	PGA4	PGA3	PGA2	PGA1	PGA0
Default Value							
0	0	0	1	0	1	0	1

AGC

The AK8856 has an adaptive AGC function. When AGC is enabled, the input signal is controlled to an optimized level by the PGA.
When AGC is turned off, manual gain setting of PGA by is allowed.
Enable / disable setting of the AGC is done by **Control 2 Register (R/W) [Sub Address 0x04].**

Sub Address 0x04   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	NSIGDEF	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[AGC]-bit
The [AGC] bit sets the mode of for the AGC.

[AGC]-bit	Function	Condition
0	Disable	
1	Enable	

note) writing into the PGA register is possible while the AGC is enabled, but the written result is not valid to register. The written result becomes valid to the register when the AGC is disabled.

There are two types of AGC-bits – one is AGCC-bit to set coring level, and the other is AGCTR-bit to control transition speed between Peak AGC and Sync AGC operations.

AGCC [1:0]-bit

[AGCC]-bit setting	Function	Note
00	+/- 2 LSB coring level	
01	+/- 3 LSB coring level	
10	+/- 4 LSB coring level	
11	no coring	

AGCCTR-bit

[AGCTR]-bit setting	Function	Note
0	Slow	same as AK8855
1	transition speed from Peak AGC to Sync AGC is fast	

Clamp

The input signal is Analog Sync-Tip clamped.
The Sync-Tip clamped input signal is then clamped to the Pedestal level after A/D conversion.

Anti-Aliasing Filter

An Analog Band Limit Filter is integrated before the ADC input in the AK8856.
The Anti-Aliasing Filter has following characteristics:

± 1.0dB (~ 6.0MHz)
27MHz -24dB (typ)

Clock

Sampling is controlled by a fixed clock in the AK8856. A PLL to synchronize the sampling clock with analog input signal is not built-in. The clock rate differs depending on the selected output picture sizes and types of input signal. The internal operating clock is either 27MHz or 24.5454MHz, which is generated from the input clock by the PLL. The internal clock rate is automatically determined by the output picture size.

	Operation clock	Size	Signal	Note
VGA	24.5454MHz	640 x 480	NTSC/PAL	Interlace output
QVGA	24.5454MHz	320 x 240	NTSC/PAL	Progressive output
CIF	27MHz	352 x 288	NTSC/PAL	
QCIF	27MHz	176 x 144	NTSC/PAL	
601	27MHz	720 x 480	NTSC	
	27MHz	720 x 576	PAL	
QVGA	24.5454MHz	240 x 180	NTSC/PAL	Rotated size
CIF	24.5454MHz	288 x 216	NTSC/PAL	Rotated size

note) For rotated CIF size, both the left-end and right-end 16 pixels are omitted and 288 X 216 picture size is output (90% area of the effective picture is output). When decoding CIF (NTSC), output rate is 2X speed of input HD.
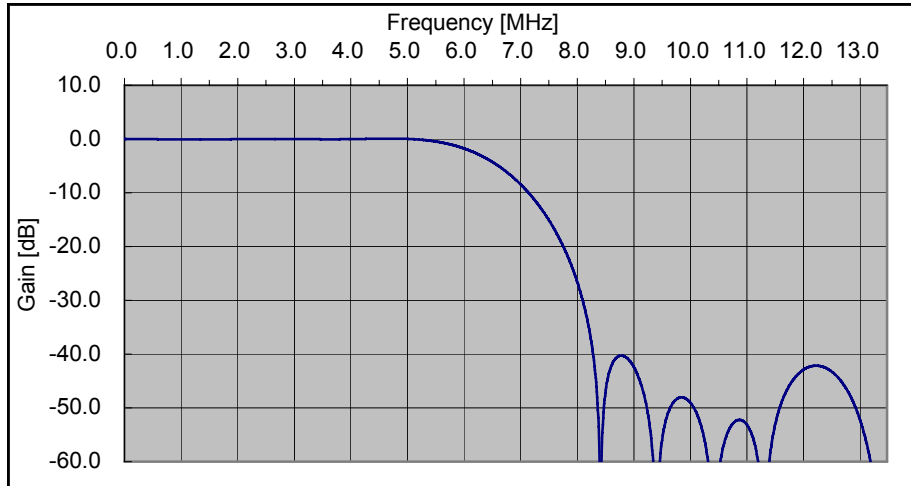
Output Picture Size

The output picture size is set by the [OFORM2 : OFORM0] bits of **Output Control 1 Register (R/W) [Sub Address 0x01]**.

[OFORM2:OFORM0]-bit

[OFORM2:OFROM0]-bit	Function	Condition
000	QVGA	
001	VGA	
010	CIF	
011	QCIF	
100	Rotated QVGA	
101	Rotated CIF	
110	601	

Decimation Filter

Typical characteristic of the decimation filter is shown here (27 MHz sampling).

Sync-Separation, Sync-Detection

Sync-Detection and Separation are executed from the digitized input signal. The recognized Sync-signal is used as reference timing for decoding process.

Digital Pedestal Clamp

The pedestal is clamped in the digital domain. The internal clamp level differs according to the type of input signal (286mV Sync signal or 300 mV Sync signal), but the output is fixes the pedestal position at code 16 (8-bit Rec. 601 level) for either condition.

YC Separation

YC separation can be either 1D or 2D. The filter characteristic for YC separation is shown here (27 MHz sampling):
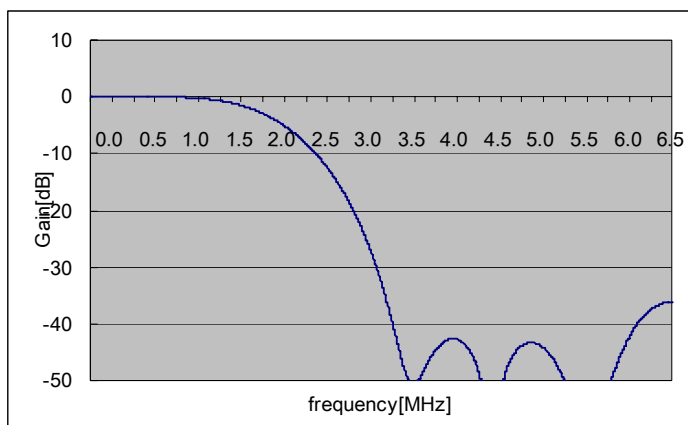
YC separation is set by the YCSEP-bit of the **Control 1 Register (R/W) [Sub Address 0x03]**

Sub Address 0x03   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	VDFLD	AGCTR	AGCC1	AGCC0	CKILSEL1	CKILSEL0	YCSEP
Default Value							
0	0	0	0	0	0	0	0

YCSEP-bit setting results in the following conditions:

YCSEP-bit	NTSC		
	QVGA, QCIF, QVGAL, CIFL	CIF	VGA, 601
0	Y: 1DYC-filter C: 1DYC-filter AK8855 compatible	Y: 1DYC-filter C: 1DYC-filter AK8855 compatible	Y: 1DYC-filter C: 1DYC-filter AK8855 compatible
1	Y: 1DYC-filter C: 2DYC-filter		Y : 2DYC-filter C : 2DYC-filter

PAL
DPAL* switch is turned ON / OFF by the YCSEP-bit (DPAL switch is always OFF in VGA mode (YCSEP-bit has no effect)).
DPAL*: process of averaging Color phases between Lines.

Auto Color Control (ACC)

This function is used to adjust the Color Burst level of the input signal to a proper level (NTSC : 286mV / PAL: 300mV). The Input Color signal level is determined by the Color Burst signal. ACC gain is 20dB maximum. ACC is turned ON / OFF by setting the ACC-bit of **Control 2 Register (R/W) [Sub Address 0x04]** .

Sub Address 0x04   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	NSIGDEF	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[ACC] bit
The [ACC] bit selects enable / disable of ACC and time constant.

[ACC]-bit	ACC Setting	Condition
0	Disable	
1	Enable	

The ACC function operates independently from the Color Saturation Adjust function (when ACC is enabled, Color Saturation adjustment is performed on the signal, which is adjusted to a proper level by ACC).

Color Killer

The Chroma Signal Quality is determined by the Color Burst level of the input signal. When the Chroma Signal level is lower than a threshold level, it is regarded as an improper signal, and the input signal is processed as strictly a luminance signal. In this case, Cb / Cr data from the AK8856 is fixed at 0x80 in 601 level.

Color Killer operation is selectable from the following 3 conditions, and it is set by the CKILSEL 1:0 bits:

(1) When the Color Burst level is lower than approximately – 23 dB.
(2) When the PLL for Color decoding cannot be locked.
(3) When either condition (1) or (2) is met.

Color Killer is set ON or OFF by the **Control 2 Register (R/W) [Sub Address 0x04].** Color Killer operating conditions are set by the CKILSEL[1:0] bit of the **Control 1 Register (R/W) [Sub Address 0x03].**

Sub Address 0x04   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	NSIGDEF	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[COLKILL]-bit
This bit enables or disables the Color Killer function.

COLKILL-bit	Color Killer Function	Condition
0	Enable	
1	Disable	

Sub Address 0x03   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	VDFLD	AGCTR	AGCC1	AGCC0	CKILSEL1	CKILSEL0	YCSEP
Default Value							
0	0	0	0	0	0	0	0

[CKILSEL 1:0]-bit

CKILSEL1:0-bit	Color Killer Operation	Note
00	when either Color Burst level is lower than –23 dB or when PLL for Color decoding cannot be locked.	
01	when PLL for Color decoding cannot be locked.	
10	when Color Burst level is lower than approximately – 23 dB.	AK8855 compatible
11	Reserved	

Frame Rate Setting

The Frame Rate is set by the [FRMRT1 : FRMRT0] bits of the **Control 2 Register (R/W) [Sub Address 0x04]**.

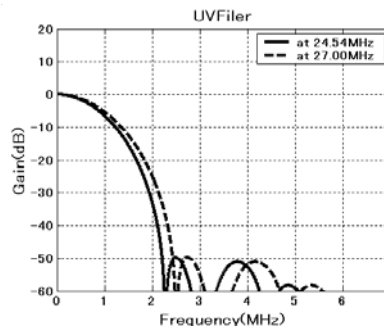| [FRMRT1:FRMRT0]-bit	Frame Rate	Condition
00	30/25(525/625)	
01	15/12.25(525/625)	
10	7.5/6.25(525/625)	
11	Reserved	

Even / Odd Field Selection

Even or Odd Field setting is used for QVGA / CIF / QCIF output modes, selected by the [ODEV] bit of the **Control 2 Register (R/W) [Sub Address 0x04]**.

ODEV-bit		Condition
0	ODD Field	
1	EVEN Field	

UV Filter

The UV Filter characteristic is shown here:

Picture Quality Adjust Process Function

Picture Quality Adjustments such as contrast, brightness, color saturation and color hue are integrated in the AK8856.

(1) Contrast
Contrast is adjusted by multiplying the Luminance signal (Y) by a gain value which is set by
Contrast Control Register (R/W) [Sub Address 0x06].

CNTSEL bit = 0
$YOUT = CONT* (YIN – 128) + 125$ YOUT : contrast arithmetic operation result
                                                                YIN   : before contrast arithmetic operation
                                                                CONT : contrast coefficient (register value)

It is also possible to define the equation by setting the register:
CNTSEL bit = 1
$YOUT = CONT* (YIN – 128) + 16$ YOUT : contrast arithmetic operation result
                                                                YIN   : before contrast arithmetic operation
                                                                CONT : contrast coefficient (register set value)

Setting is done with the [CNTSEL] bit of **Control 2 Register (R/W) [Sub Address 0x04]**

The range of the contrast gain coefficient varies from 0 to 1.99 (1/128 step), and when the arithmetic operation result exceeds this range, it is clipped to the upper-limit of 254, or the lower-limit of 1 (the output result ranges from 16 to 235 when the 601 limit-bit is 1).

Bit allocation of **Contrast Control Register**:

Sub Address 0x06   **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Sub Address 0x04   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	NSIGDEF	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

[CNTSEL] bit
This bit sets the changeover point of the contrast adjustment.

[CNTSEL]-bit	Function	Condition
0	To be adjusted at Luminance 125 as a center point	
1	To be adjusted at Luminance 16 as a center point.	

(2) Brightness

Brightness is adjusted by adding a value which is set by **Brightness Control Register (R/W) [Sub Address 0x07]** to the luminance (Y) signal.

YOUT = YIN + BR

YOUT : brightness arithmetic operation result
YIN   : before brightness arithmetic operation
BR   : brightness coefficient (register value)

The brightness coefficient varies from –127 to +127, and the value is in 2's complement format. When the arithmetic operation result exceeds this range, it is clamped to the upper-limit of 254 or the lower-limit of 1 (output result ranges from 16 to 235 when the 601 limit-bit is 1).

Bit allocation of **Brightness Control Register**:

Sub Address 0x07   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

(3) Color Saturation

Color Saturation is adjusted by multiplying the Color Signal (C) by a value which is set by the **Saturation Control Register (R/W) [Sub Address 0x08]**. The arithmetic result is U / V de-modulated. The Saturation coefficient varies from 0 to 255 in 1/128 programmable steps. The default value of the register is a non-adjusted value (0x80).

Bit allocation of **Saturation Control Register:**

Sub Address 0x08   **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

(4) Color Hue

Color Hue can be rotated in the AK8856. The rotation amount of Color Hue is determined by a value which is set by the **HUE Control Register (R/W) [Sub Address 0x09]**. Rotation phase varies from ±45 degrees (0.35 degrees per step). The default value of the register is a non-adjusted value (0x00). The register value is in 2's complement format.

Bit allocation of **Hue Control Register:**

Sub Address 0x09   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

Input Video Decoding Period

The number of lines used for video decoding varies according to the output mode. Refer to the figure on thr next page which shows "Input Video Signal vs. Output Data relationship".

Active Video Period:
      525 line system: line 22 ~ line 261 & line 285 ~ line 524
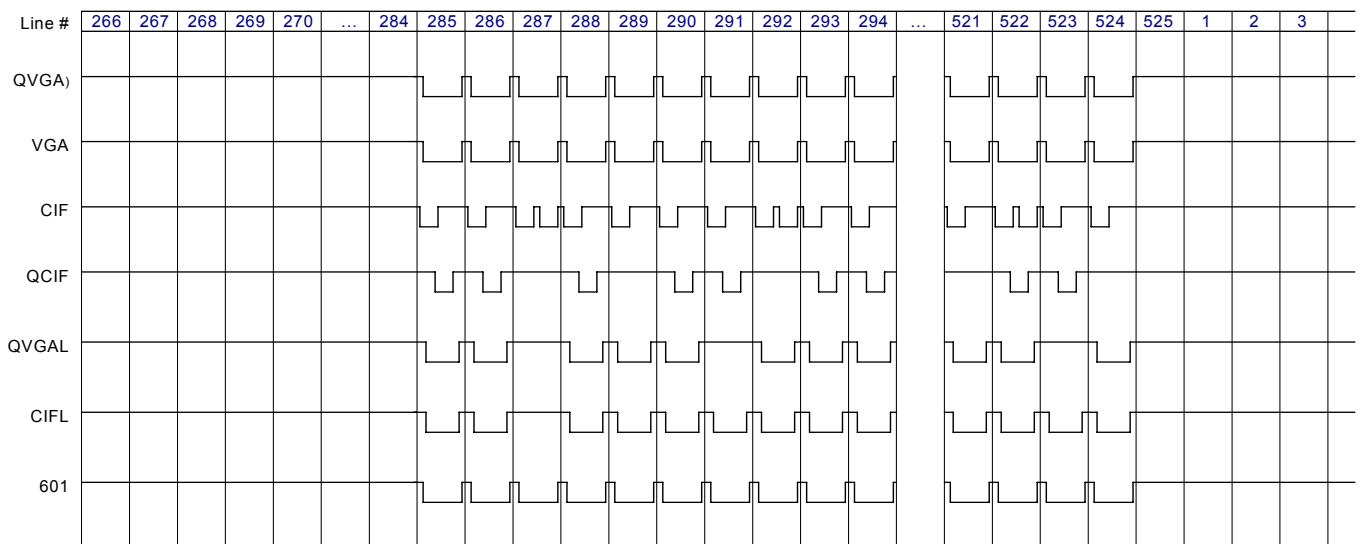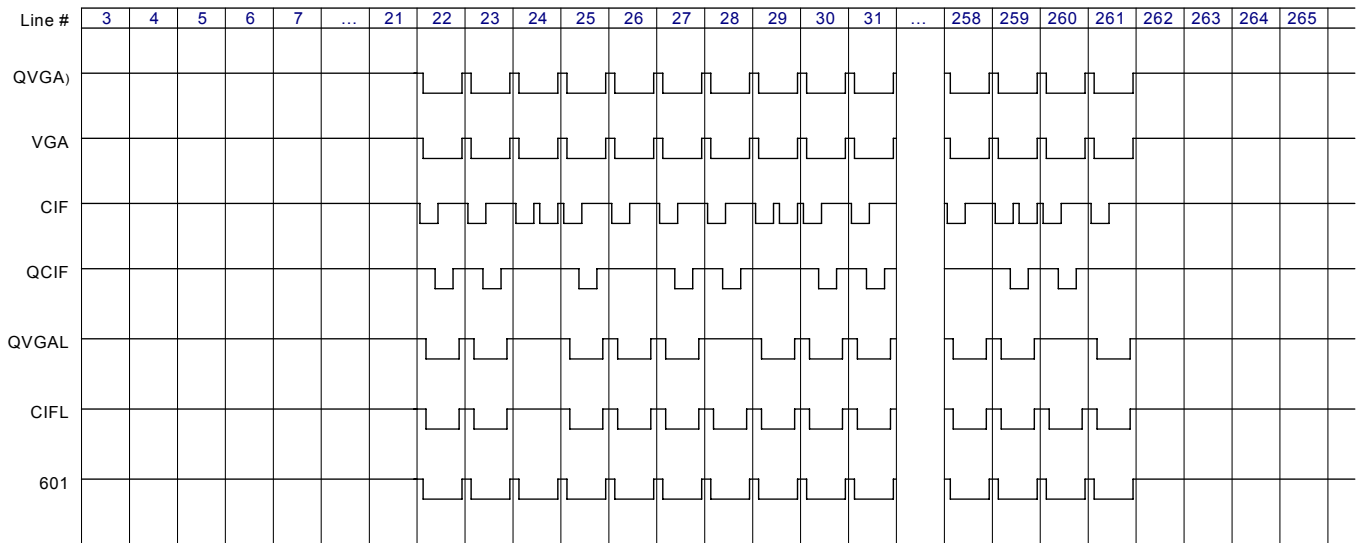   625 line system: line 23 ~ line 310 & line 336 ~ line 623

Vertical Blanking Period:
      525 line system: line 525 ~ line 1 ~ line 21 & line 262 ~ line 284
      625 line system: line 624 ~ line 625 – line1 ~ line 22 & line 311 ~ line 335

  The default value for the output during the Vertical Blanking period is Black level (Y = 0x10, Cb/Cr = 0x80)

NTSC   (Low logic indicates Active lines.)

Input Video Signal vs Output Data Relationship (NTSC)

PAL (Low logic indicates Active lines.)

| Line # | 625 | 1 | 2 | 3 | 4 | ... | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | ... | 307 | 308 | 309 | 310 | 311 | 312 | 313 | 314 |

QVGA

VGA

CIF

QCIF

QVGAL

CIFL

601

| Line # | 313 | 314 | 315 | 316 | 317 | ... | 335 | 336 | 337 | 338 | 339 | 340 | 341 | 342 | 343 | 344 | 345 | ... | 620 | 621 | 622 | 623 | 624 | 625 | 1 | 2 |

QVGA

VGA

CIF

QCIF

QVGAL

CIFL

601
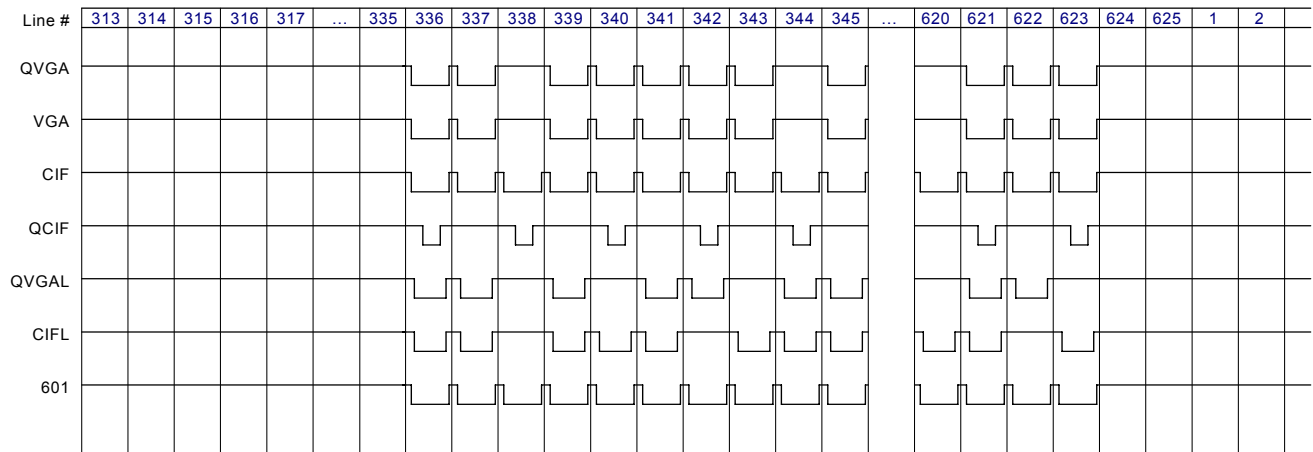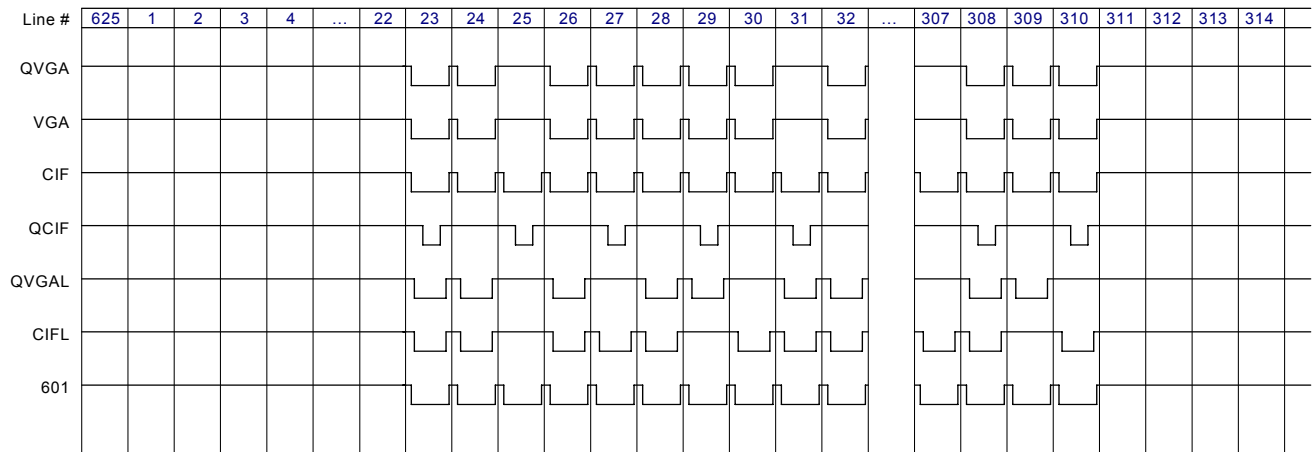
<u>Input Video Signal vs Output Data Relationship (PAL)</u>

Closed Caption / Closed Caption Extended Data / VBID (CGMS) / WSS

Closed Caption data, Closed Caption Extended data, VBID (CGMS) and WSS signals that are super-imposed during the VBI interval are decoded in the AK8856. The decoded data is written into a register. When the request bits [bit3 : bit 0] of the **Request VBI Info Register (W) [Sub Address 0x0A]** are set, the AK8856 acknowledges that a decode request of the data has been made, and it is placed into a data wait condition. After data is detected and decoded, the host is notified, using [bit7 : bit 5] of the **Status Register (R/W) [Sub Address 0x10]** that decoding has been completed.

The results are written into the **Closed Caption 1 Register (R) [Sub Address 0x12]** / **Closed Caption 2 Register (R) [Sub Address 0x13]**, **Extended Data 1 Register (R) [Sub Address 0x14]** / **Extended Data 2 Register (R) [Sub Address 0x15]**, **VBID / WSS1 Register (R) [Sub Address 0x16]** / **VBID / WSS2 Register (R) [Sub Address 0x17]** respectively.

The data are super-imposed on the respective line:
CRCC code of VBID data (CGMS-A) is decoded and the result is stored in the register.

Signal	Line	Note
Closed Caption	NTSC : Line-21	525-Line
Closed Caption Extended	NTSC : Line-284	525-Line
VBID	NTSC : Line-20/283	525-Line
WSS	PAL : Line-23	625-Line

Configuration of **Request VBI INFO Register:**

Sub Address 0x0A   **Default Value: 0x00**
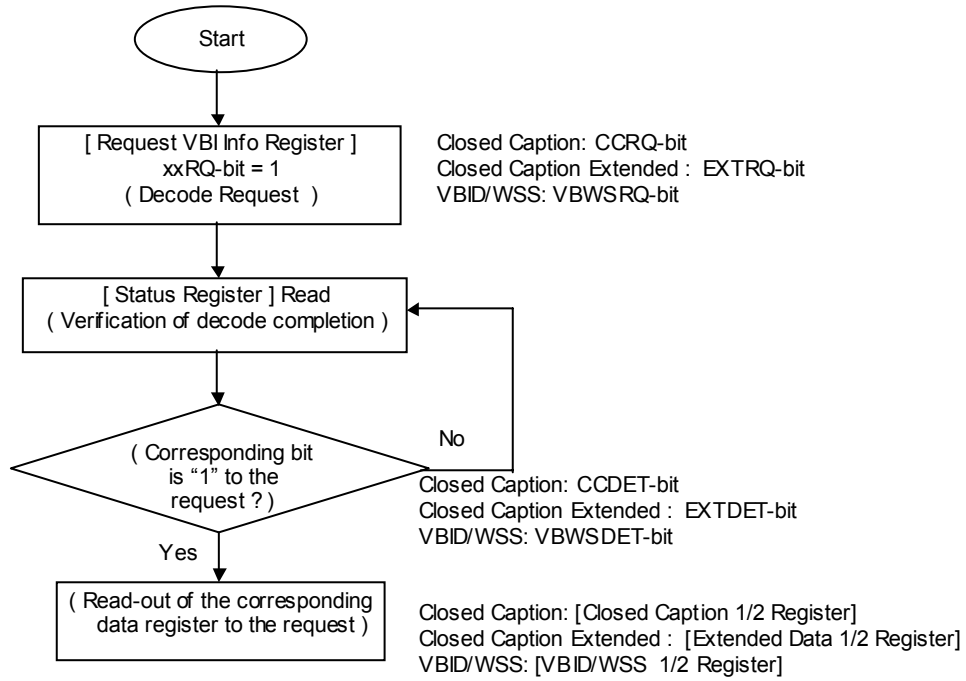
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	VBWSRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Configuration of **Status Register** is as follows

Sub Address 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBWSSDET	EXTDET	CCDET	AGCSTS	VLOCKSTS	PKWHITE	COLKILST	NSIG

Information read-out flow during VBI interval:

```
                    ┌─────────────┐
                   (    Start      )
                    └──────┬──────┘
                           │
                           ▼
        ┌──────────────────────────────┐
        │  [ Request VBI Info Register ]│      Closed Caption: CCRQ-bit
        │      xxRQ-bit = 1             │      Closed Caption Extended :  EXTRQ-bit
        │    ( Decode Request )         │      VBID/WSS: VBWSRQ-bit
        └──────────────┬───────────────┘
                       │
                       ▼
        ┌──────────────────────────────┐
        │   [ Status Register ] Read    │◄──────────┐
        │ ( Verification of decode completion ) │    │
        └──────────────┬───────────────┘           │
                       │                            │
                       ▼                         No │
                  ◇─────────────◇──────────────────┘
                 ( Corresponding bit
                   is "1" to the          Closed Caption: CCDET-bit
                   request ? )            Closed Caption Extended :  EXTDET-bit
                  ◇─────────────◇         VBID/WSS: VBWSDET-bit
                       │ Yes
                       ▼
        ┌──────────────────────────────┐
        │ ( Read-out of the corresponding │   Closed Caption: [Closed Caption 1/2 Register]
        │   data register to the request ) │   Closed Caption Extended :  [Extended Data 1/2 Register]
        └──────────────────────────────┘   VBID/WSS: [VBID/WSS  1/2 Register]
```

Reading Closed Caption data :
   Write a "1" to the CCRQ-bit of Request VBI Info **Register (W) [Sub Address 0x0A]**. When a "1" is written to
   this bit, the AK8856 is placed in a wait condition for Closed Caption Data decoding. Then when data arrives,
   it is decoded and a "1" is written back to the CCDET-bit of the **Status Register (R / W) [Sub Address 0x10]**.

   After reset, the CCDET-bit is "1" (it goes to "0" when a "1" is written to the CCRQ-bit). The decoded data is
   written into the **Closed Caption 1 Register (R) [Sub Address 0x12]** and the **Closed Caption 2 Register
   (R) [Sub Address 0x13]**. Data in the **Closed Caption 1 Register** and **Closed Caption 2 Register** are
   retained until they are over-written with new data.

Configuration of **Closed Caption 1 Register** and **Closed Caption 2 Register:**

Closed Caption 1 Register (R) [Sub Address 0x12]
Sub Address 0x12

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Closed Caption 2 Register (R) [Sub Address 0x13]
Sub Address 0x13

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

Reading out Closed Caption Extended Data :
   Write a "1" to the EXTRQ-bit of the **Request VBI Info Register (W) [Sub Address 0x0A]**. When a "1" is
   written to this bit, the AK8856 is placed in a wait condition for Extended Data decoding. Then when data
   arrives, it is decoded and a "1" is written to the EXTDET-bit of the **Status Register (R / W) [Sub Address
   0x10]**.

   After reset, the EXTDET-bit is "1" (it goes to "0" when a "1" is written to the EXTRQ-bit). The decoded data is
   written into the **Extended Data 1 Register (R) [Sub Address 0x14]** and the **Extended Data 2 Register (R)
   [Sub Address ox15]**. Data in the **Extended Data 1 Register** and **Extended Data 2 Register** are retained
   until they are over-written with new data.

Configuration of **Extended Data 1 Register** and **Extended Data 2 Register:**

Extended Data 1 Register (R) [Sub Address 0x14]
Sub Address 0x14

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Extended Data 2 Register (R) [Sub Address 0x15]
Sub Address 0x15

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

Reading out VBID Data :

Write a "1" to the VBWSRQ-bit of the **Request VBI Info Register (W) [Sub Address 0x0A]**. When a "1" is written to this bit, the AK8856 is placed in a wait condition for VBID data decoding. Then when data arrives, it is decoded and a "1" is written to the VBWSDET-bit of the **Status Register (R / W) [Sub Address 0x10]**.

After reset, the VBWSDET-bit is a "1" (it goes to "0" when a "1" is written to the VBWSRQ-bit). Decoded data is 13-bits long, and it is written into the **VBID / WSS1 Register (R) [Sub Address 0x16]** and **VBID / WSS 2 Register (R) [Sub Address 0x17]**. VBID data is valid only in a 525-line system. These registers are also commonly used for WSS Read-Out register.

CRCC code is decoded and the result is stored in the register. Data in the **VBID / WSS 1 Register** and **VBID / WSS 2 Register** are retained until they are over-written with new data.

Configuration of **VBID / WSS 1 Register** and **VBID / WSS 2 Register:**

VBID/WSS 1 Register (R) [Sub Address 0x16] Register to store VBID data
Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6

VBID/WSS 2 Register (R) [Sub Address 0x17] Register to store VBID data
Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14

Reading out WSS Data :

Write a "1" to the VBWSRQ-bit of the **Request VBI Info Register (W) [Sub Address 0x0A]**. When a "1" is written to this bit, the AK8856 is placed in a wait condition for VBWS data decoding. Then when data arrives, it is decoded and a "1" is written back to the VBWS-bit of **Status Register (R / W) [Sub Address 0x10]**.

After reset, the VBWS-bit is a "1" (it goes to "0" when a "1" is written to the VBWSRQ-bit). WSS data is valid only for 625-line systems. These registers are also commonly used for VBID Read-Out register. Decoded data are written into the **VBID / WSS 1 Register (R) [Sub Address 0x16]** and the **VBID / WSS 2 Register (R) [Sub Address 0x17]**. Data in the **VBID / WSS 1 Register** and the **VBID / WSS 2 Register** are retained until they are over-written with new data.

VBID/WSS 1 Register (R) [Sub Address 0x16] Register for storing WSS data
Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

VBID/WSS 2 Register (R) [Sub Address 0x17] Register for storing WSS data
Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

Macrovision Decoding

When a Macrovision Copy Protect signal is present, the AK8856 decodes the additional Macrovision information and stores the result in the **Macrovision Status Register (R/W) [Sub Address 0x11]**.

Configuration of the **Macrovision Status Register:**

Sub Address 0x11

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PSPDET	AGCPDET	BPPDET	SYNCRED	CSTYPE	CSDET	AGCDET

[AGCDET] bit
When Macrovision AGC process is detected, this bit goes to "1".

[AGCDET]-bit	Status of Macrovision Detection	Condition
0	AGC Process not detected	
1	AGC Process detected	

[CSDET] bit
When Macrovision Color Stripe Process is detected, this bit goes to "1".

[CSDET]-bit	Status of Macrovision Detection	Condition
0	Color Stripe Process not detected	
1	Color Stripe Process detected	

[CSTYPE] bit
When the CSDET-bit is "1", Color Stripe Process type is indicated.

[CSTYPE]-bit	Status of Macrovision Detection	Condition
0	Color Stripe Type 2 is set	
1	Color Stripe Type 3 is set	

[SYNCRED] bit
When the SYNCRED-bit is "1", Sync Reduction has been detected.

[SYNCRED]-bit	Status of Macrovision Detection	Condition
0	-	
1	Sync Reduction detected	

[BPPDET] bit
When the BPPDET-bit is "1", an "End of Field Back Porch Pulse" has been detected.

[BPPDET]-bit	Status of Macrovision Detection	Condition
0	-	
1	End of Field Back Porch Pulse detected	

[AGCPDET] bit
When AGCPDET-bit is "1", an AGC Pulse has been detected.

[AGCPDET]-bit	Status of Macrovision Detection	Condition
0	-	
1	AGC Pulse detected	

[PSPDET] bit
When PSPDET-bit is "1", a Pseudo Sync Pulse has been detected.

[PSPDET]-bit	Status of Macrovision Detection	Condition
0	-	
1	Pseudo Sync Pulse detected.	

Decode Data Output (Rec. 601 Limit)

The AK8856 outputs decoded data at a level (Y / Cb / Cb 4:2:2) specified by ITU-R BT.601. Minimum and maximum output data can be selected by the [LIMIT601] bit of the **Output Control 1 Register (R/W) [Sub Address 0x01]**.

Bit allocation of Output Control 1 Register is as follows.

Sub Address 0x01   **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDPSUP	TRSVSEL	OIF1	OIF0	LIMIT601	OFORM2	OFORM1	OFORM0
Default Value							
0	0	0	0	0	0	0	0

[LIMIT601] bit

Maximum and minimum output data is specified by the [LIMIT601]-bit. All internal arithmetic operations are processed at Min. = 1, Max. = 254. Clipping value of the output code differs by the setting of the [LIMIT601] –bit. The default setting value is "0".

LIMIT601-bit	Output code Min.Max	Condition
0	Y : 1 ~ 254 Cb/Cr : 1 ~ 254	(Default value)
1	Y : 16 ~ 235 Cb/Cr : 16 ~ 240	

Output Interface

The AK8856 supports 3 types of interfaces:

        (1) Camera interface (QVGA / CIF / QCIF)
        (2) Interface by HD / VD / DVALID (VGA / QVGA / CIF / QCIF)
        (3) 656 Interface (601 specification compatible size (720 X 480))

(1) Camera Interface
There are two types of data interfaces: "(1-1) HV & VAF Interface Mode" and "(1-2) SAV / EAV Interface Mode".

In this mode, since synchronization shift with the input signal is adjusted at the head part of the line, the interval between lines may fluctuate to some degree. When an exceptional input signal is decoded, there may be cases where the lack of number of lines and lack of number of pixels per line occur, regardless of operation mode. At the default value, an end of frame is set at the rising edge of the VAF signal, and an end of line is set by the HV signal. The polarity of VAF / HV / DVALID / CLKO is programmable through the **Output Control 2 Register (R/W) [Sub Address (0x02)]**.

The following timing diagrams show operation examples at HDP = 0, VDP = 0, DVALDP = 0, and CLKINV = 1 settings.

Since the output is progressive in Camera Interface mode, picture sizes in this mode are QVGA / CIF / QCIF / rotated QVGA / rotated CIF.

Definition of SAV / EAV Interface Mode:

	SAV	EAV
Active	0x80	0x9D
VBlank	0xAB	0xB6

In SAV / EAV output mode, HV / VAF signal is not output by default. The register must be set for this mode.

(1-1)   HV / VAF Interface
The following timing diagram shows CIF size output as an example.

VD/VAF

HD/HV

D/CDT[7:0]   Line1 Line2 Line3 Line4   Line288   Line1 Line2

CLKO

HD/HV

D/CDT[7:0]   Cb0 Y0 Cr0 Y1 Cb1 Y2 Cr1 Y3 Cb2 Y4   ••••••   Cb175 Y351 Cr175

CLKO
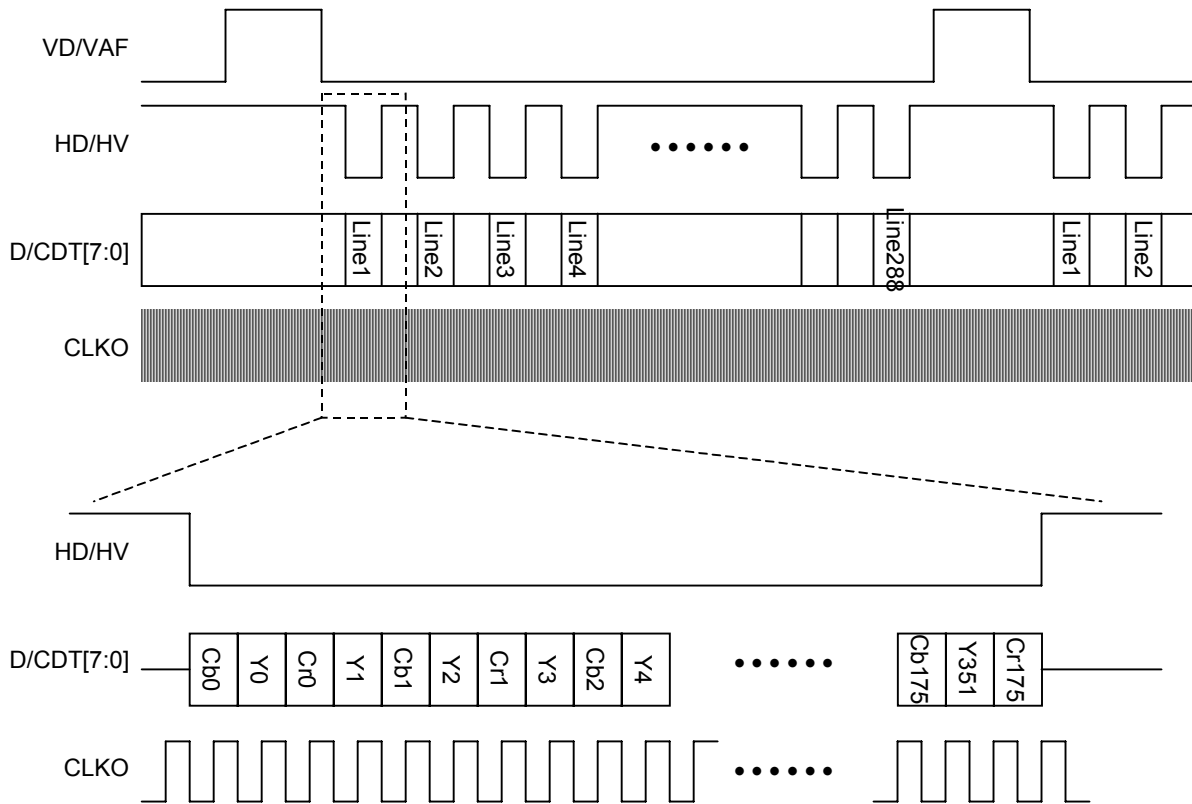
(1-2) SAV / EAV Interface (CIF size output example)
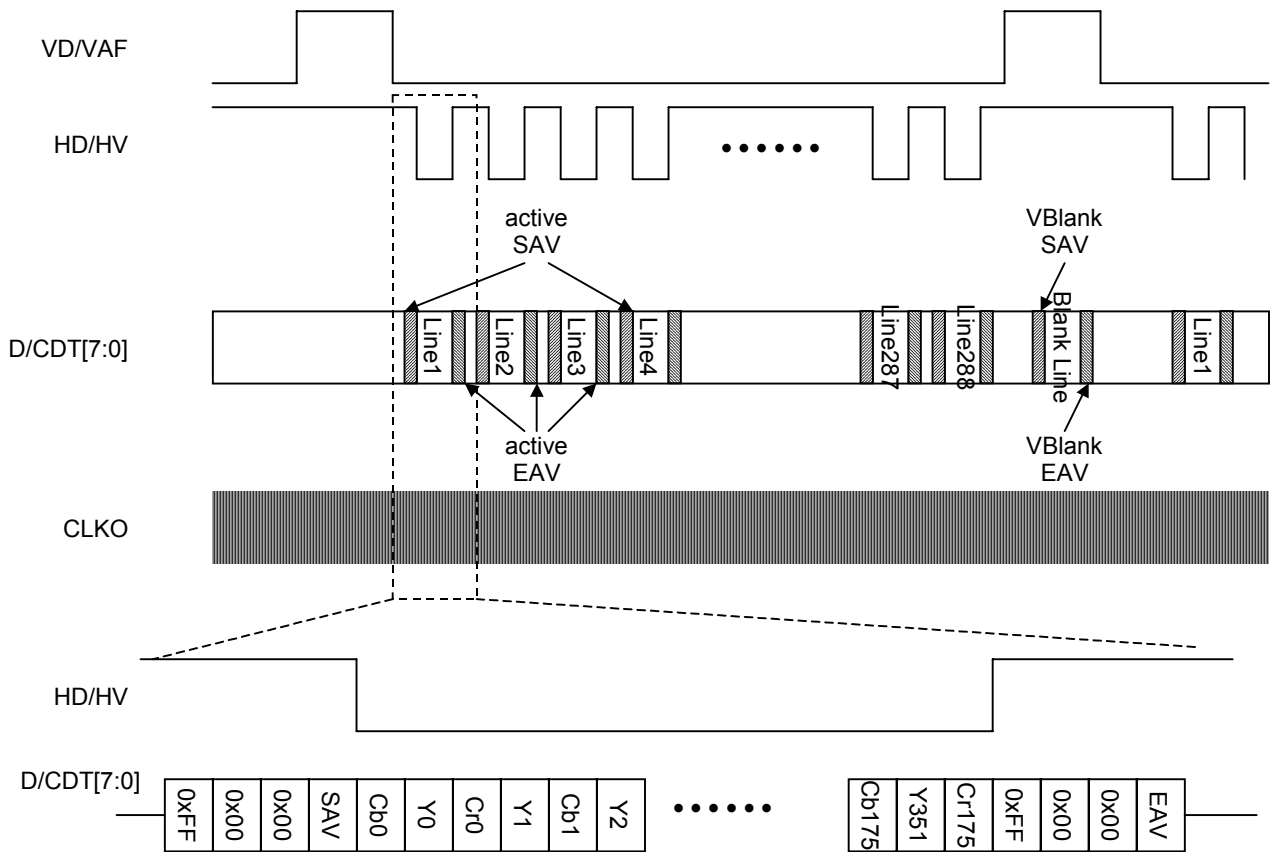
Output timing for the Camera Interface mode is illustrated here (the polarity of HV/VAF/DVALID can be changed by register setting).

NTSC   Register Set : VLF = 1'b0, OIF[1:0] = 2'b10
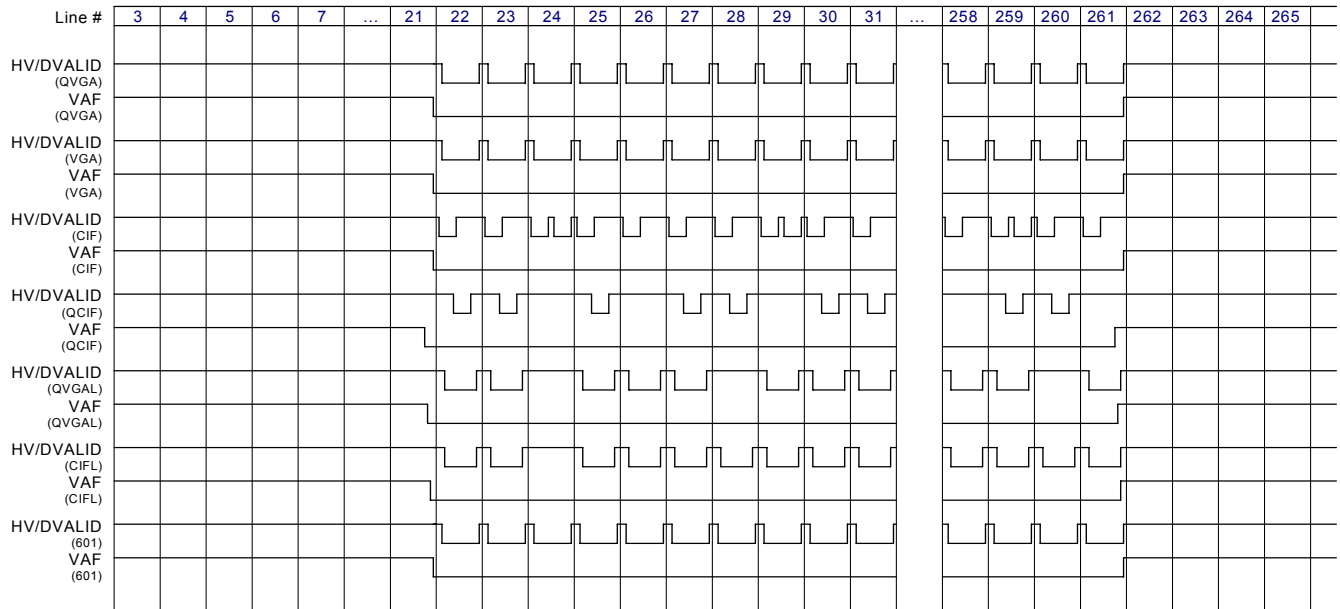
Note: For output modes other than VGA or 601, DVALID signal becomes active (low) at either ODD or EVEN timing.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

NTSC   Register Set : VLF = 1'b0, OIF[1:0] = 2'b10
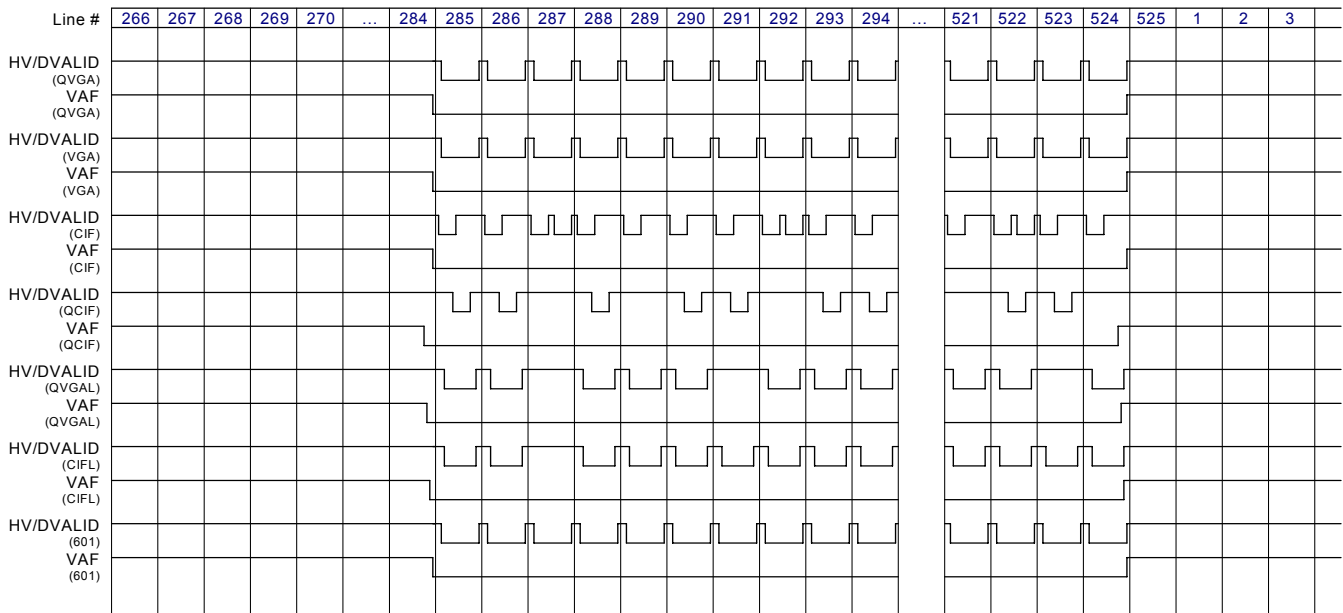
Note: For output modes other than VGA or 601, DVALID signal becomes active (low) at either ODD or EVEN timing.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

PAL   Register Set : VLF = 1'b1, OIF[1:0] = 2'b10

Note: For output modes other than VGA or 601, DVALID signal becomes active (low) for either ODD or EVEN timing.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

PAL   Register Set : VLF = 1'b1, OIF[1:0] = 2'b10
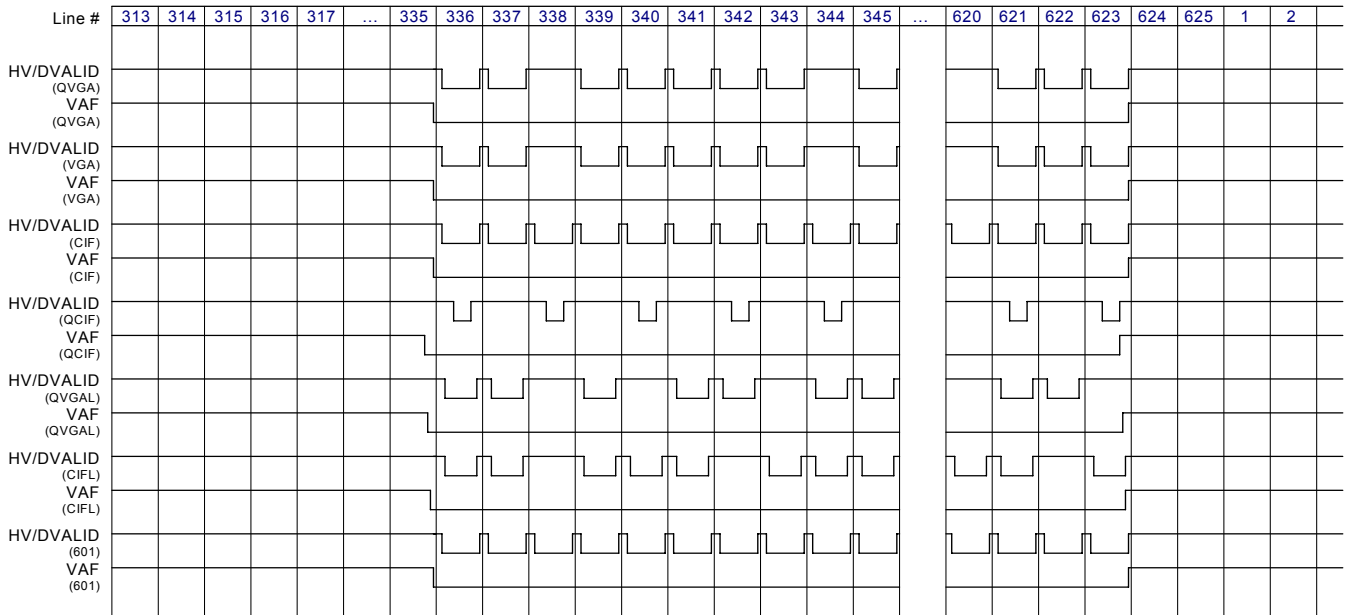
Note: For output mode modes other than VGA or 601, DVALID signal becomes active (low) for either ODD or EVEN timing.
QVGAL: Rotated QVGA, CIFL: Rotated CIF

Timing Chart (Camera I/F)   QVGA (NTSC) Register Set : VLF = 1'b0, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b00
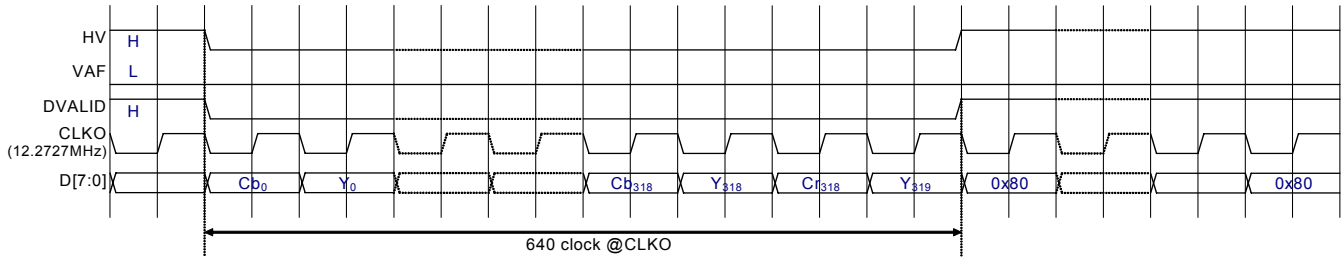
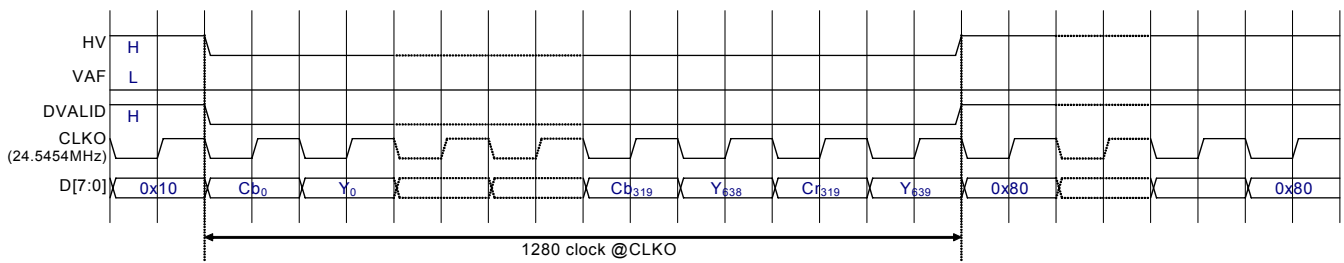Timing Chart (Camera I/F)   VGA (NTSC)   Register Set : VLF = 1'b0, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b00
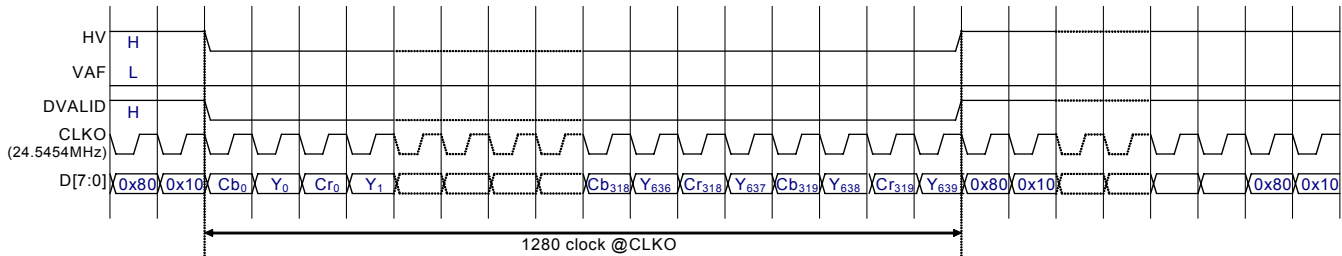
Timing Chart (Camera I/F)   CIF (NTSC)   Register Set : VLF = 1'b0, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b00

HV
VAF
DVALID
CLKO (27.0MHz)
D[7:0]   0x80 0x10 Cb$_0$ Y$_0$ Cr$_0$ Y$_1$ ... Cb$_{348}$ Y$_{348}$ Cr$_{348}$ Y$_{349}$ Cb$_{350}$ Y$_{350}$ Cr$_{350}$ Y$_{351}$ 0x80 0x10 ... 0x80 0x10

704 clock @CLKO
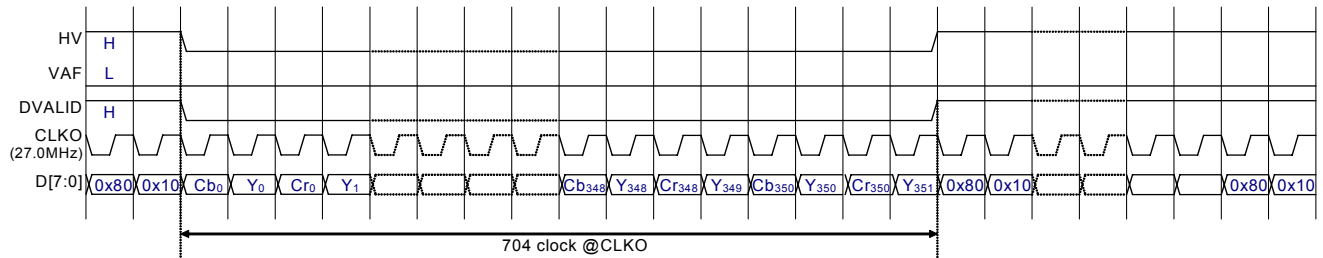
For NTSC, CIF output mode, 2 lines are output while the 1 line input. HD/VD signal are also output doubled rate.

Timing Chart (Camera I/F)   QCIF (NTSC)   Register Set : VLF = 1'b0, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b00
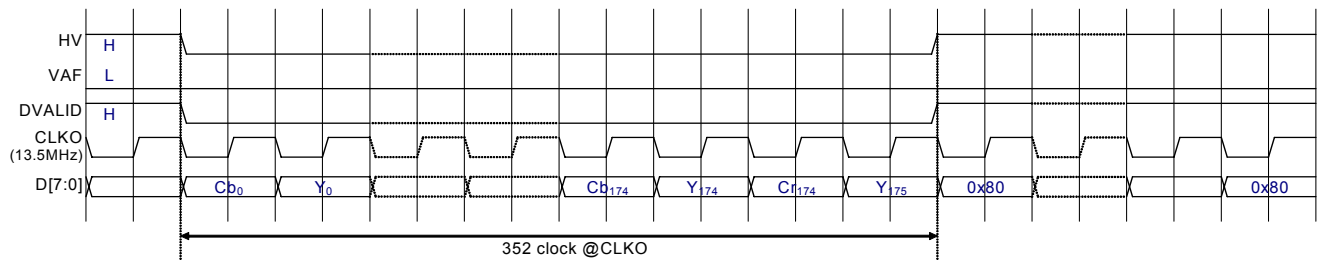
HV
VAF
DVALID
CLKO (13.5MHz)
D[7:0]   Cb$_0$ Y$_0$ ... Cb$_{174}$ Y$_{174}$ Cr$_{174}$ Y$_{175}$ 0x80 ... 0x80

352 clock @CLKO

Timing Chart (Camera I/F)　　　Rotated QVGA (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b00

HV
VAF
DVALID
CLKO (12.2727MH)
D[7:0]

Cb_0　Y_0　... Cb_{238}　Y_{238}　Cr_{238}　Y_{239}　0x80 ... 0x80

480 clock @CLKO

Timing Chart (Camera I/F)　　　Rotated CIF (NTSC)　　　Register Set: VLF = 1'b0, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b00

HV
VAF
DVALID
CLKO (12.2727MHz)
D[7:0]

Cb_0　Y_0　... Cb_{286}　Y_{286}　Cr_{286}　Y_{287}　0x80 ... 0x80

576 clock @CLKO
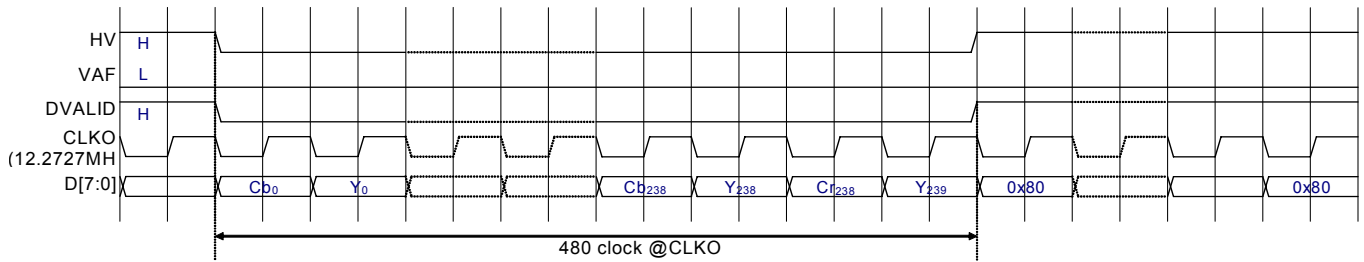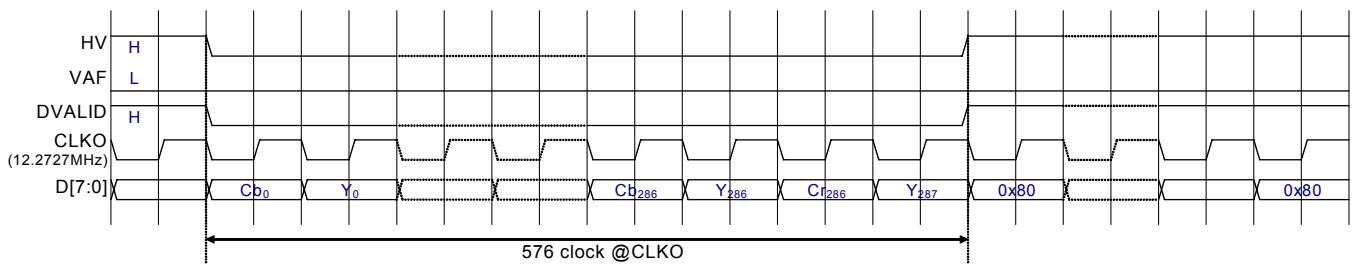
Timing Chart (Camera I/F)　　　601Output (NTSC)　　　Register Set: VLF = 1'b0, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b00

HV
VAF
DVALID
CLKO (27.0MHz)
D[7:0]

0x80 0x10 Cb_0 Y_0 Cr_0 Y_1 ... Cb_{716} Y_{716} Cr_{716} Y_{717} Cb_{718} Y_{718} Cr_{718} Y_{719} 0x80 0x10 ... 0x80 0x10

1440 clock @CLKO

Timing Chart (Camera I/F)   QVGA (PAL)   Register Set: VLF = 1'b1, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b00

640 clock @CLKO

Timing Chart (Camera I/F)   QVGA (PAL)   Register Set: VLF = 1'b1, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b00

1280 clock @CLKO

Timing Chart (Camera I/F)   CIF (PAL)   Register Set : VLF = 1'b1, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b00
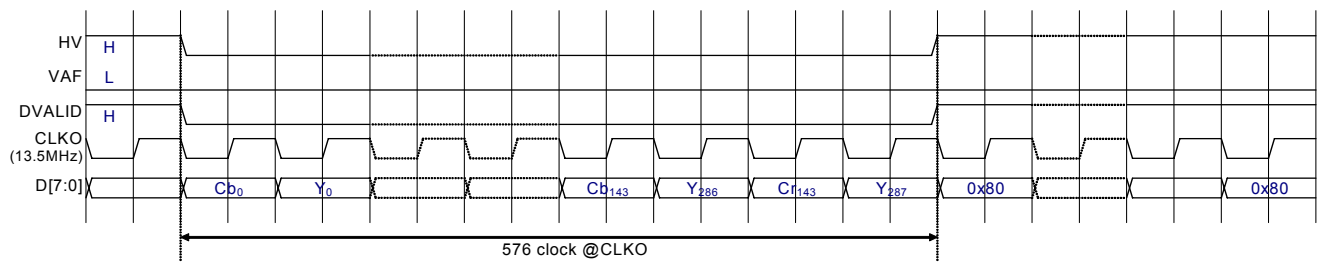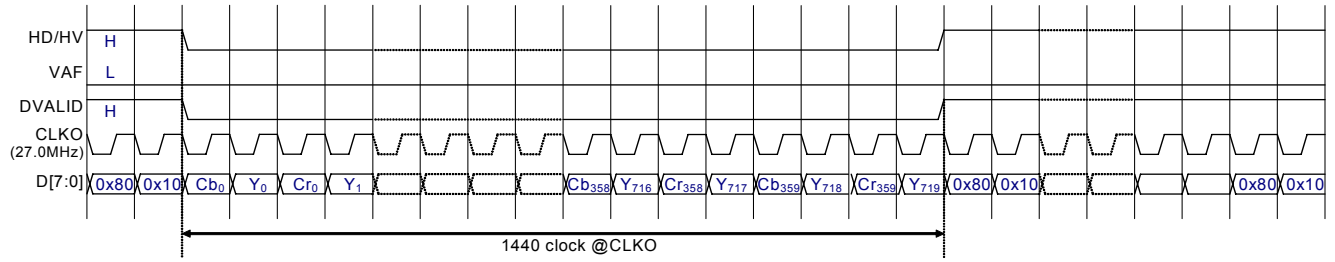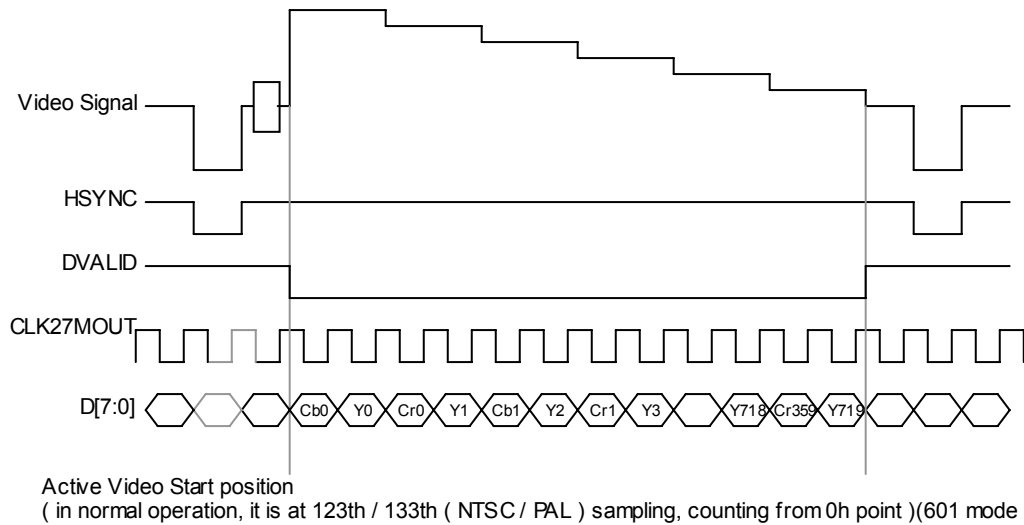

704 clock @CLKO
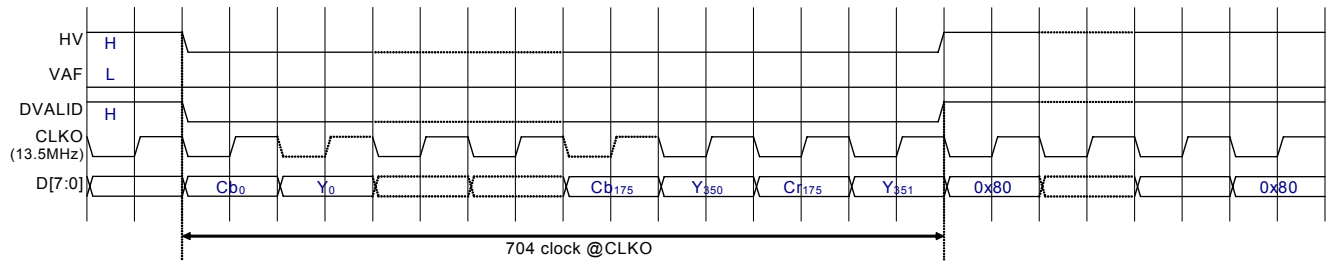
Timing Chart (Camera I/F)   QCIF (PAL)   Register Set : VLF = 1'b1, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b00
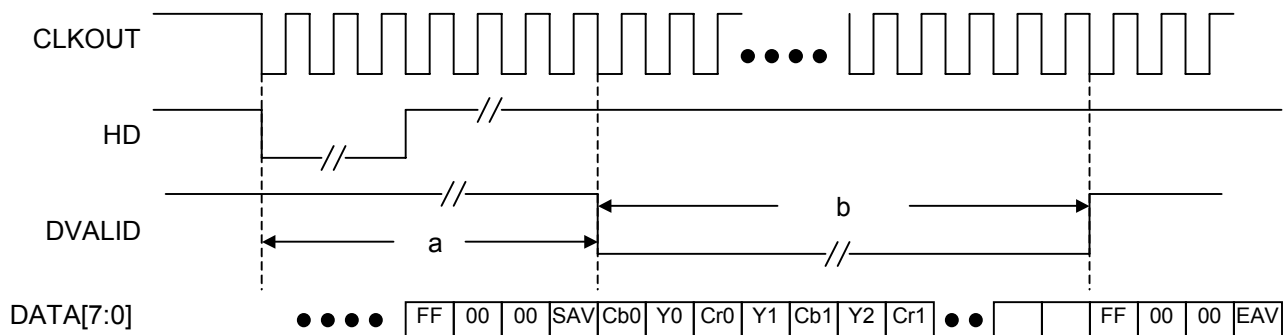

352 clock @CLKO
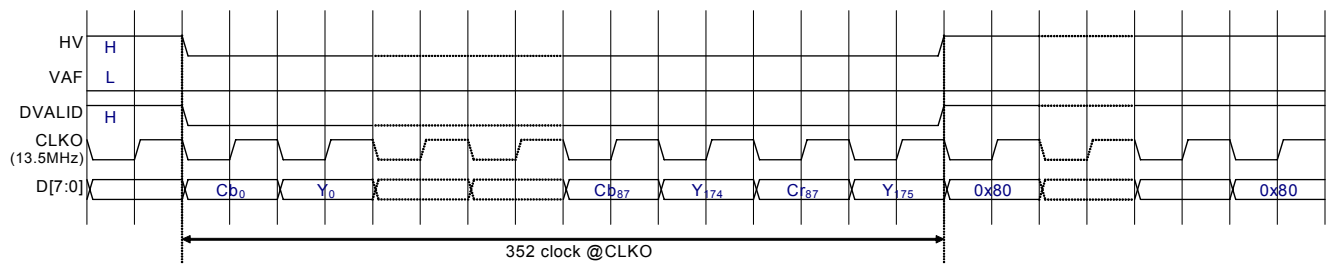
Timing Chart (Camera I/F)　　　Rotated QVGA (PAL)　　Register Set: VLF = 1'b1, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b00

480 clock @CLKO
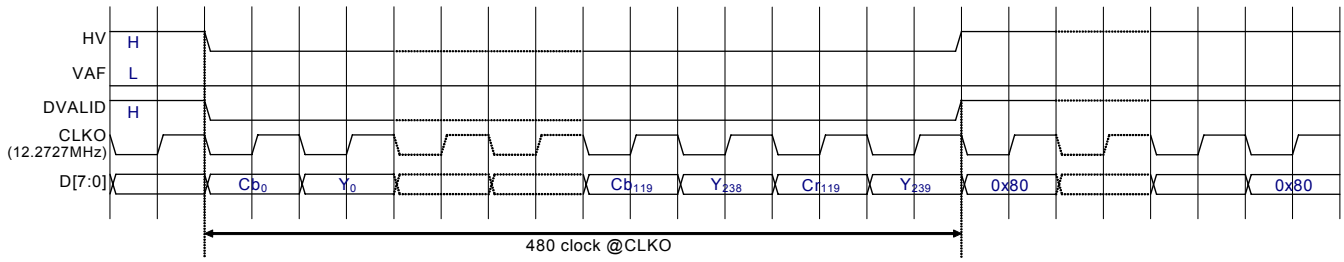
Timing Chart (Camera I/F)　　　Rotated CIF (PAL)　　　Register Set: VLF = 1'b1, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b00

576 clock @CLKO

Timing Chart (Camera I/F)　　601Output (PAL)　　　　Register Set : VLF = 1'b1, OFORM[2:0] = 3'b110, OIF[1:0] =

HD/HV	H	
VAF	L	
DVALID	H	
CLKO (27.0MHz)		
D[7:0]		0x80 0x10 Cb_0 Y_0 Cr_0 Y_1 ... Cb_{358} Y_{716} Cr_{358} Y_{717} Cb_{359} Y_{718} Cr_{359} Y_{719} 0x80 0x10 ... 0x80 0x10

1440 clock @CLKO

(2) Interface by HD / VD / DVALID

In this interface mode, synchronization is determined by HD and VD. The DVALID signal is active low during the active video space. Since even and odd field recognition can be achieved through HD and VD, interlace information is known. The relationship of the DVALID signal and video data is illustrated here (601 output):

Video Signal

HSYNC

DVALID

CLK27MOUT

D[7:0]   Cb0 Y0 Cr0 Y1 Cb1 Y2 Cr1 Y3 Y718 Cr359 Y719

Active Video Start position
(in normal operation, it is at 123th / 133th (NTSC / PAL) sampling, counting from 0h point)(601 mode)

Timing diagram for HD / VD interface mode:

CLKOUT

HD

DVALID

a   b

DATA[7:0]   ● ● ● ●   FF | 00 | 00 | SAV | Cb0 | Y0 | Cr0 | Y1 | Cb1 | Y2 | Cr1 ● ● | FF | 00 | 00 | EAV

(Data FF0000SAV & FF0000EAV are in Rec.656 mode. For modes other than Rec.656, the data are replaced with 10H80H10H80H data)

Mode	[OFORM2:OFROM0]	525-Line (VLF-bit = 0) Number of CLKO cycles			625-Line (VLF-bit = 1) Number of CLKO cycles		
		a	b	DTCLK Rate	a	b	DTCLK Rate
QVGA	000	118	640	12.2727MHz	127	640	12.2727MHz
VGA	001	236	1280	24.5454MHz	254	1280	24.5454MHz
CIF	010	130	704	27.0MHz	140	704	13.5MHz
QCIF	011	306	352	13.5MHz	316	352	13.5MHz
Rotated QVGA	100	198	480	12.2727MHz	207	480	12.2727MHz
Rotated CIF	101	150	576	12.2727MHz	159	576	12.2727MHz
601	110	244	1440	27MHz	264	1440	27.0MHz

* note: output data rate of CIF size mode in 525 line system (NTSC) is doubled.

The relationship of HD/VD/DVALID is illustrated here. (The polarity of HD/VD/DVALID can be changed by setting the register)

NTSC Register Set : VLF = 1'b0, OIF[1:0] = 2'b10
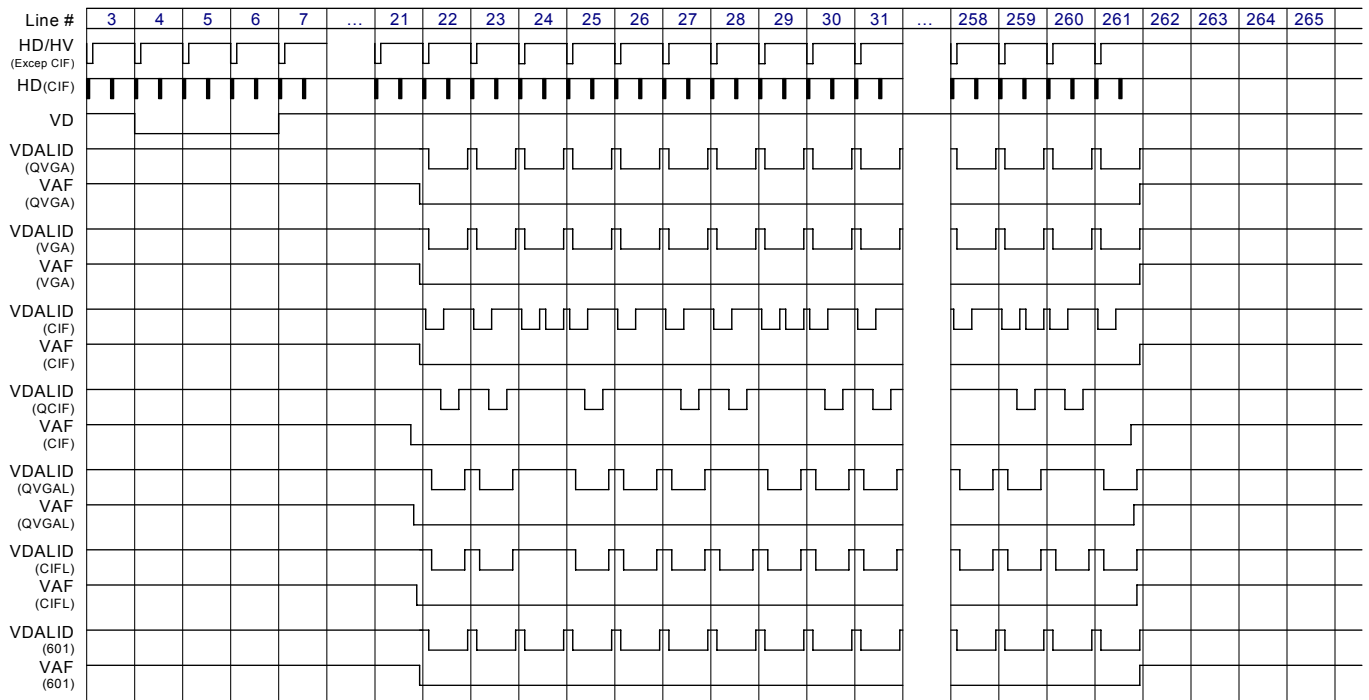
Note: For output modes other than VGA or 601, the DVALID signal becomes active (low) for either ODD or EVEN timing. QVGAL: Rotated QVGA, CIFL: Rotated CIF
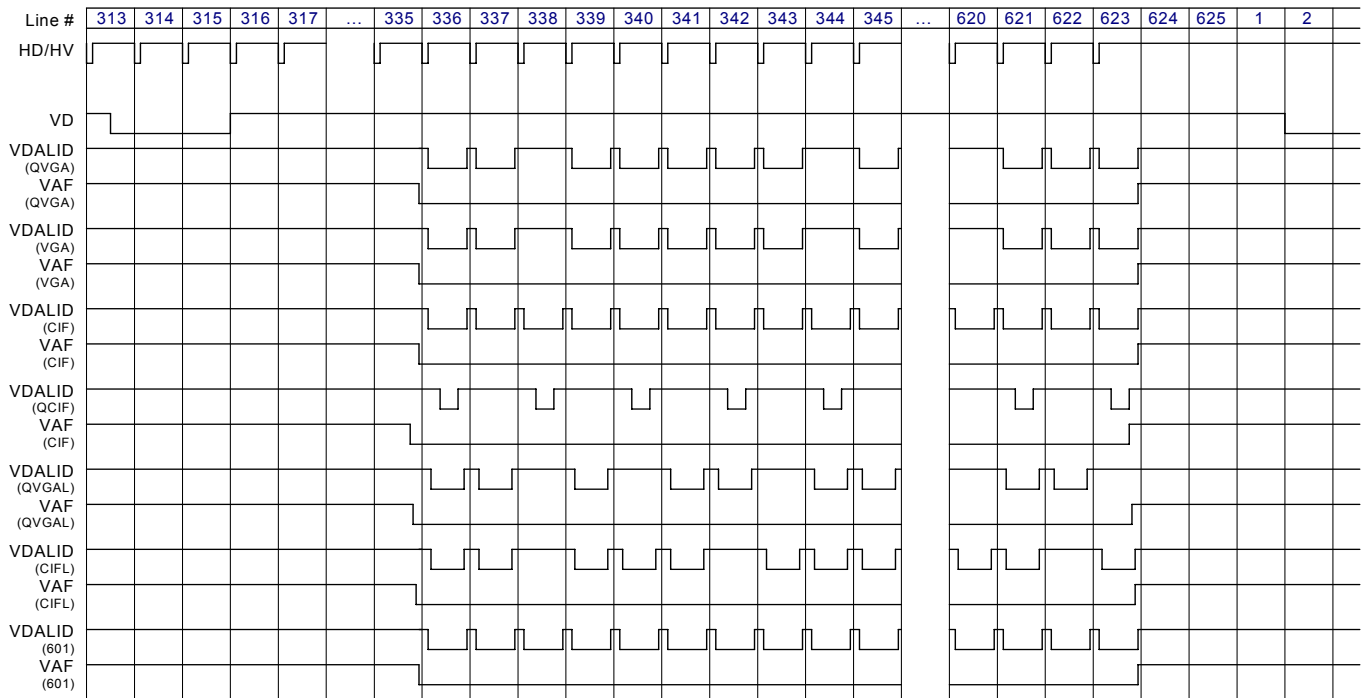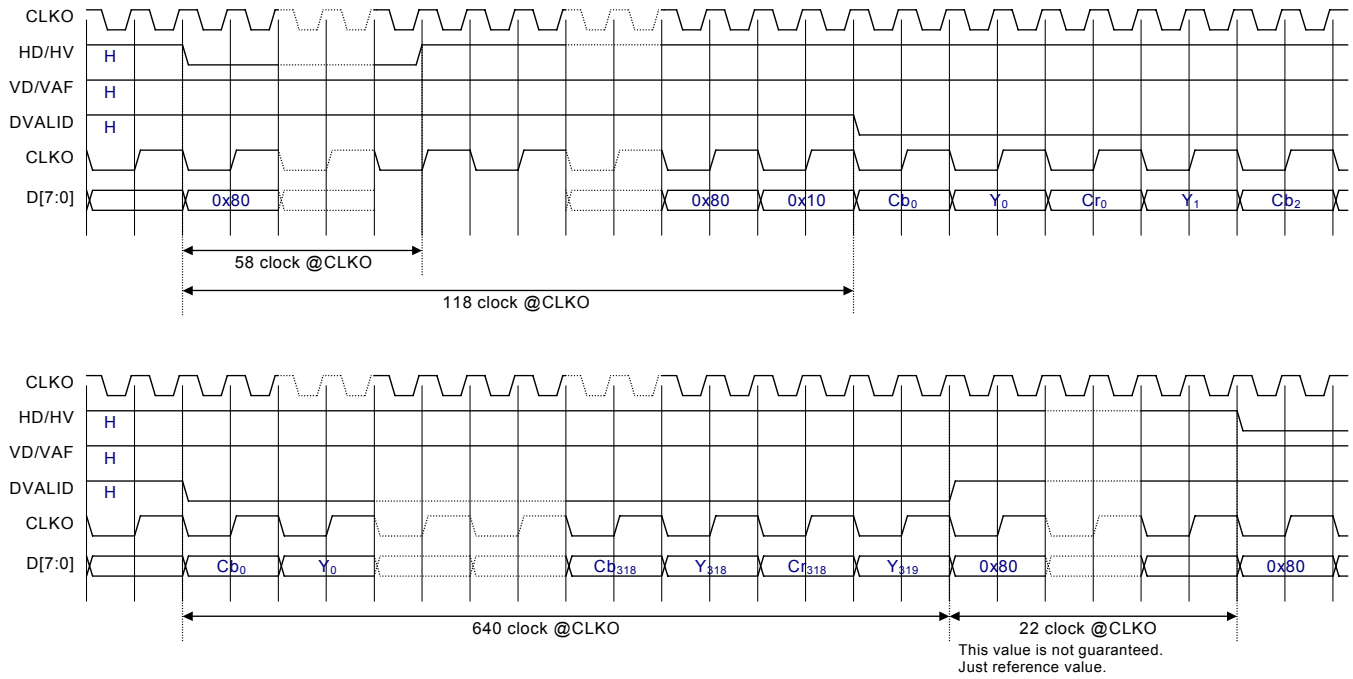
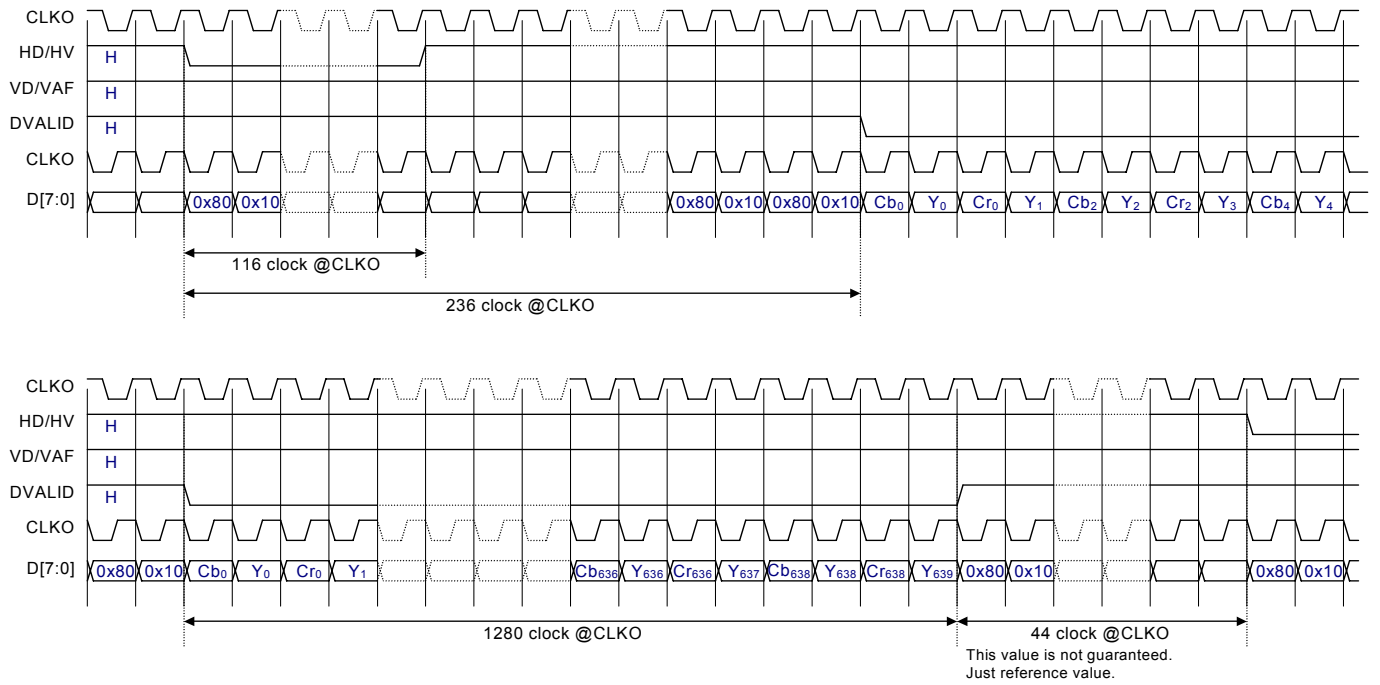NTSC   Register Set: VLF = 1'b0, OIF[1:0] = 2'b10

Note: For output modes other than VGA or 601, the DVALID signal becomes active (low) for either ODD or EVEN timing. QVGAL: Rotated QVGA, CIFL: Rotated CIF

PAL   Register Set: VLF = 1'b1, OIF[1:0] = 2'b10
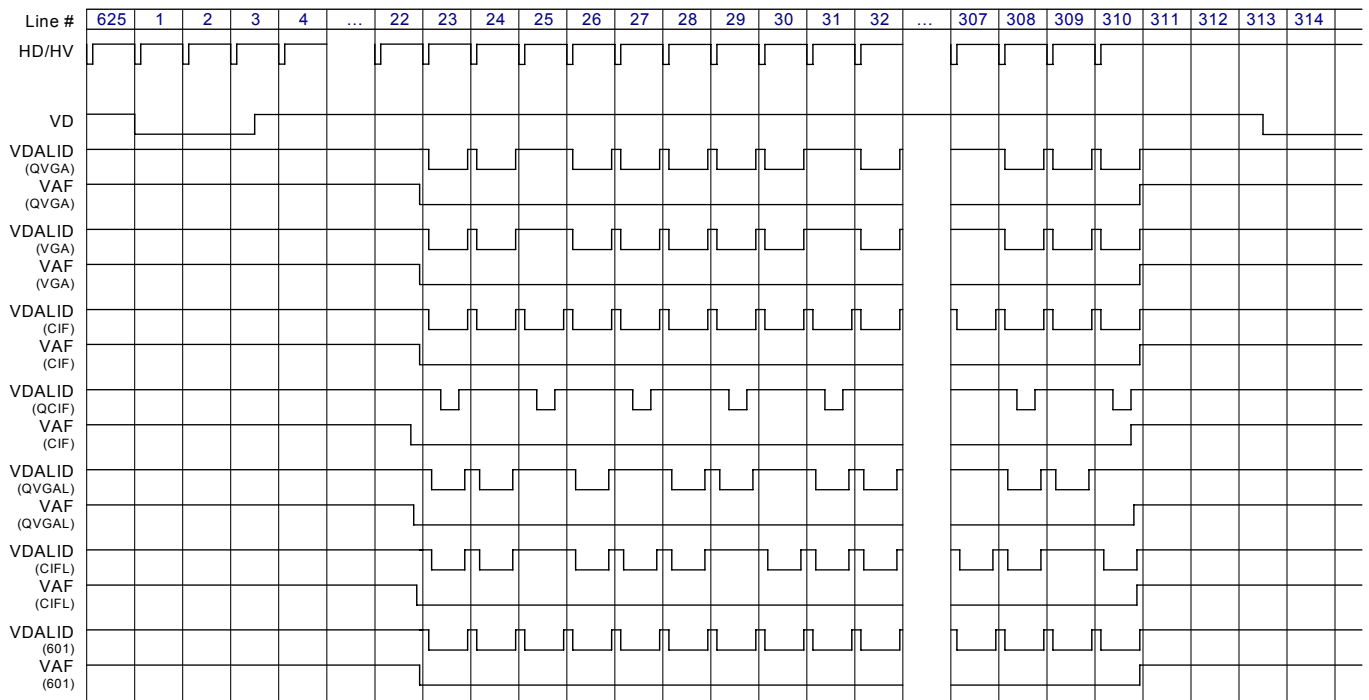
Note: For output modes other than VGA or 601, the DVALID signal becomes active (low) for either ODD or EVEN timing. QVGAL: Rotated QVGA, CIFL: Rotated CIF

PAL   Register Set: VLF = 1'b1, OIF[1:0] = 2'b10

Note: For output modes other than VGA or 601, the DVALID signal becomes active (low) for either ODD or EVEN timing. QVGAL: Rotated QVGA, CIFL: Rotated CIF

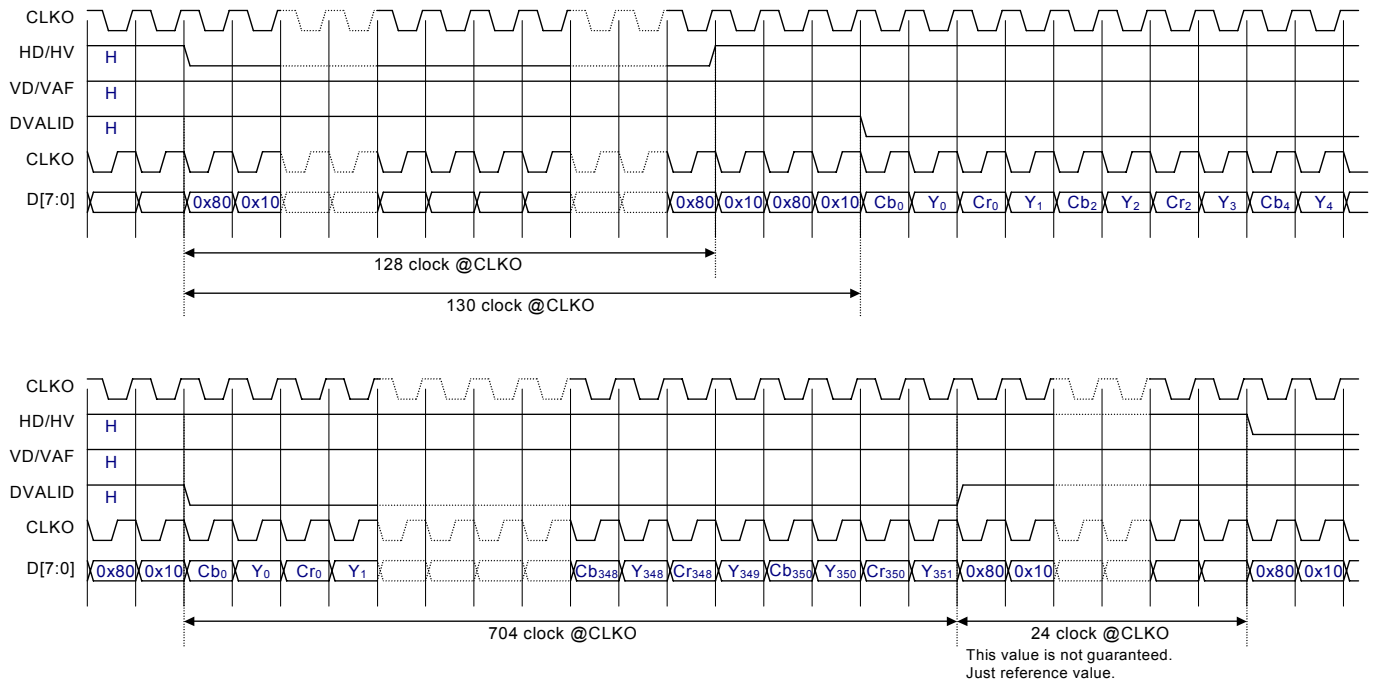Timing Chart   QVGA (NTSC) Register Set : VLF = 1'b0, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b10

CLKO
HD/HV   H
VD/VAF   H
DVALID   H
CLKO
D[7:0]   0x80   0x80   0x10   Cb0   Y0   Cr0   Y1   Cb2

58 clock @CLKO

118 clock @CLKO

CLKO
HD/HV   H
VD/VAF   H
DVALID   H
CLKO
D[7:0]   Cb0   Y0   Cb318   Y318   Cr318   Y319   0x80   0x80

640 clock @CLKO   22 clock @CLKO
                                       This value is not guaranteed.
                                       Just reference value.

Timing Chart   VGA (NTSC)   Register set : VLF = 1'b0, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b10
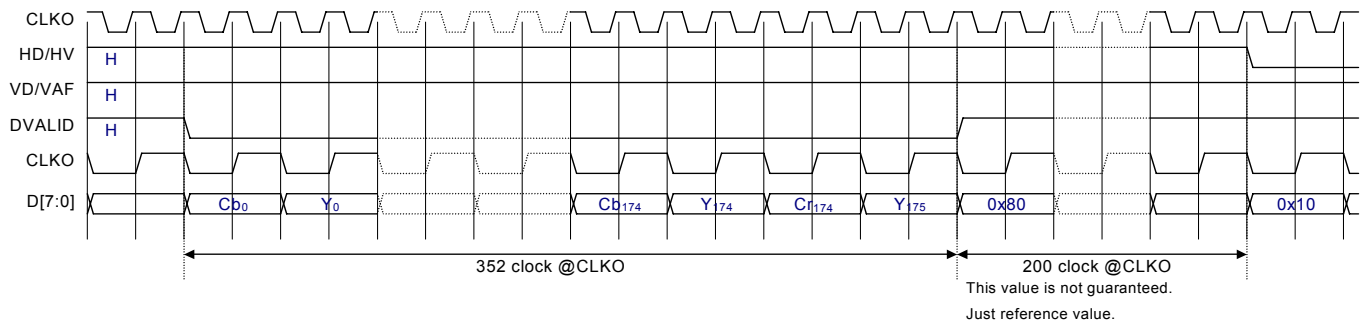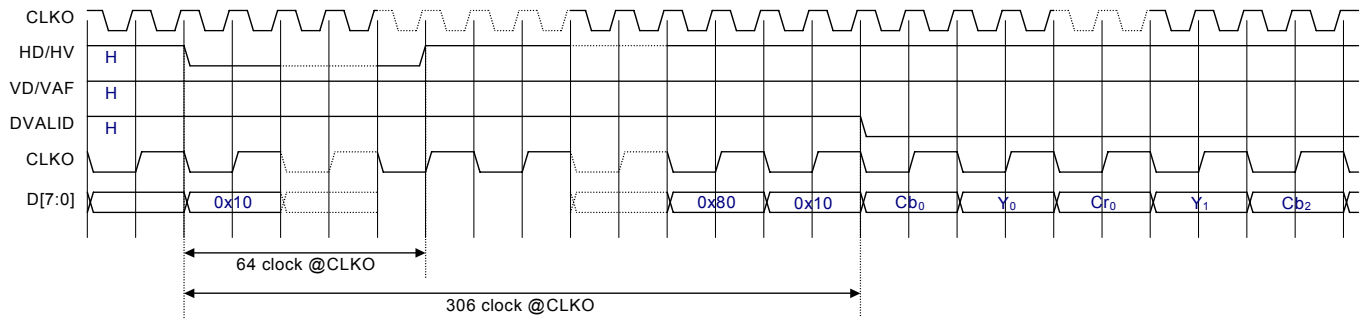
Timing Chart   CIF(NTSC)   Register Set : VLF = 1'b0, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b10
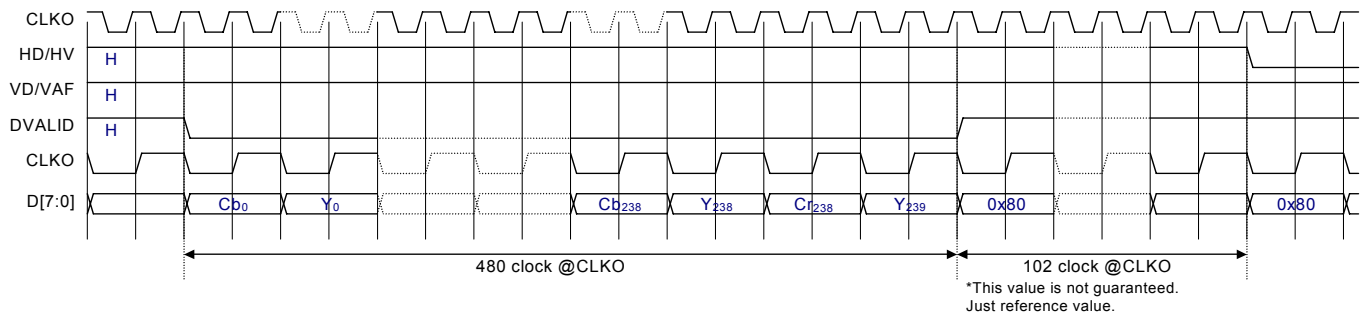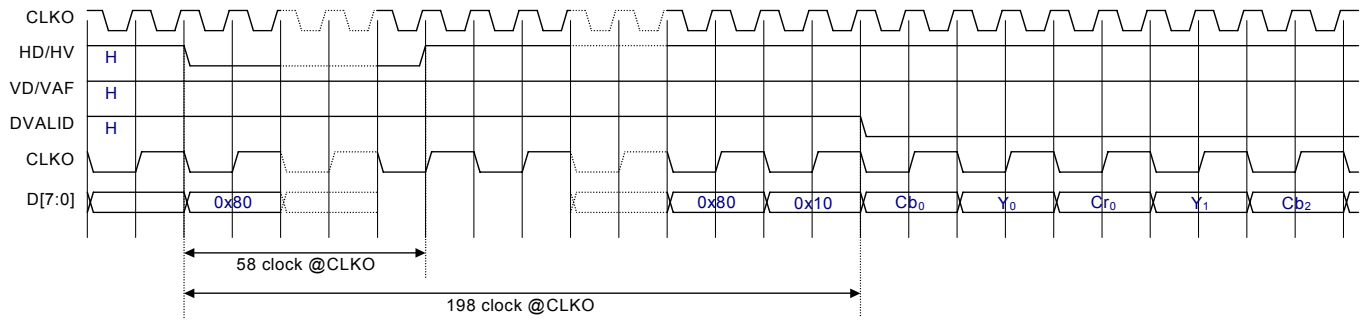

For NTSC and CIF output mode, two lines are output while one line is input. HD/VD signal are also output at a doubled rate.
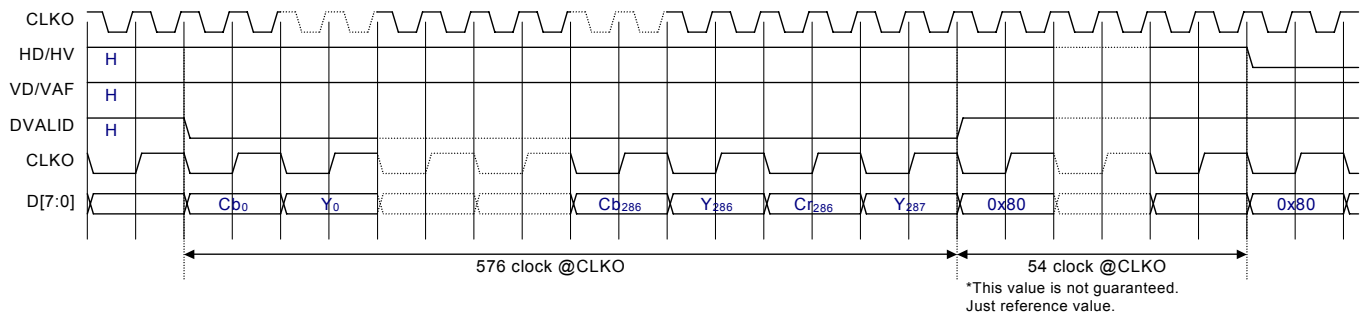
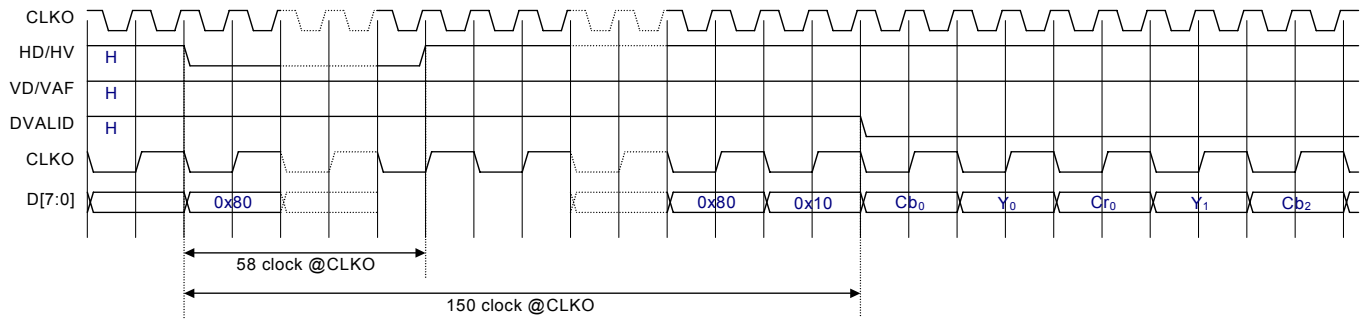Timing Chart   QCIF (NTSC)   Register Set : VLF = 1'b0, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b10

CLKO

HD/HV   H

VD/VAF   H

DVALID   H

CLKO

D[7:0]   0x10   0x80   0x10   Cb_0   Y_0   Cr_0   Y_1   Cb_2

64 clock @CLKO

306 clock @CLKO

CLKO

HD/HV   H

VD/VAF   H

DVALID   H

CLKO

D[7:0]   Cb_0   Y_0   Cb_{174}   Y_{174}   Cr_{174}   Y_{175}   0x80   0x10

352 clock @CLKO

200 clock @CLKO
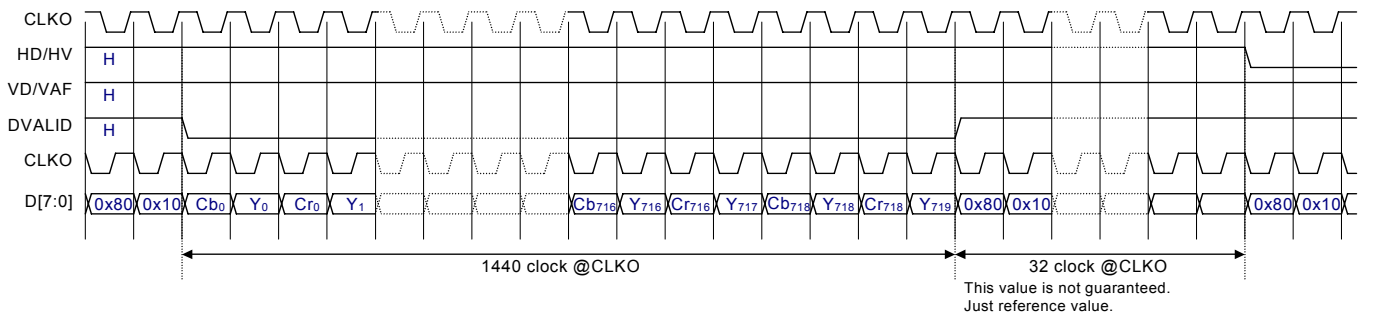
This value is not guaranteed.
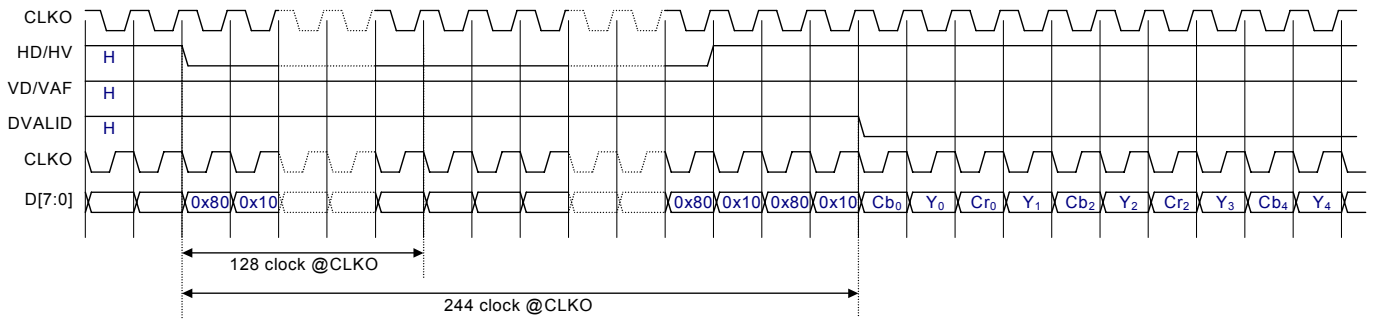
Just reference value.

Timing Chart   Rotated QVGA (NTSC) Register Set: VLF = 1'b0, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b10

Timing Chart   Rotated CIF(NTSC)   Register Set: VLF = 1'b0, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b10

CLKO

HD/HV   H

VD/VAF   H

DVALID   H

CLKO

D[7:0]   0x80   0x80   0x10   Cb₀   Y₀   Cr₀   Y₁   Cb₂

58 clock @CLKO

150 clock @CLKO

CLKO

HD/HV   H

VD/VAF   H

DVALID   H

CLKO

D[7:0]   Cb₀   Y₀   Cb₂₈₆   Y₂₈₆   Cr₂₈₆   Y₂₈₇   0x80   0x80

576 clock @CLKO   54 clock @CLKO

*This value is not guaranteed.
Just reference value.

Timing Chart   601output (NTSC)   Register Set: VLF = 1'b0, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b10

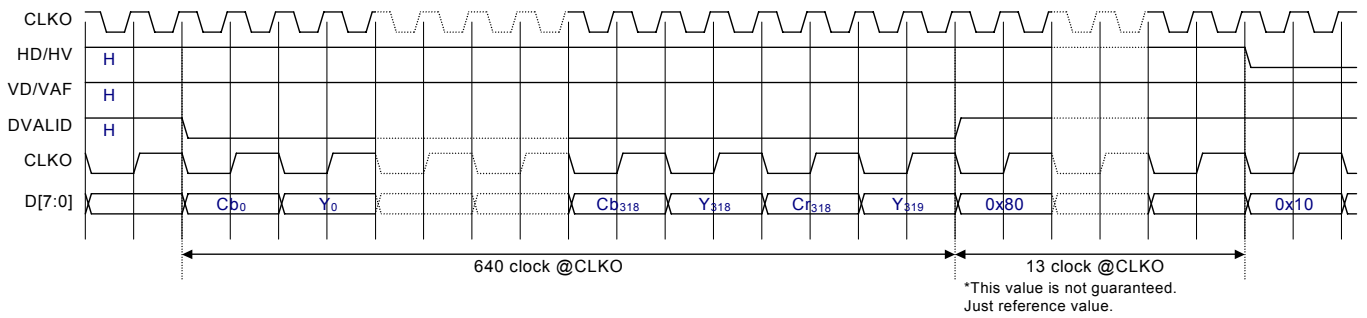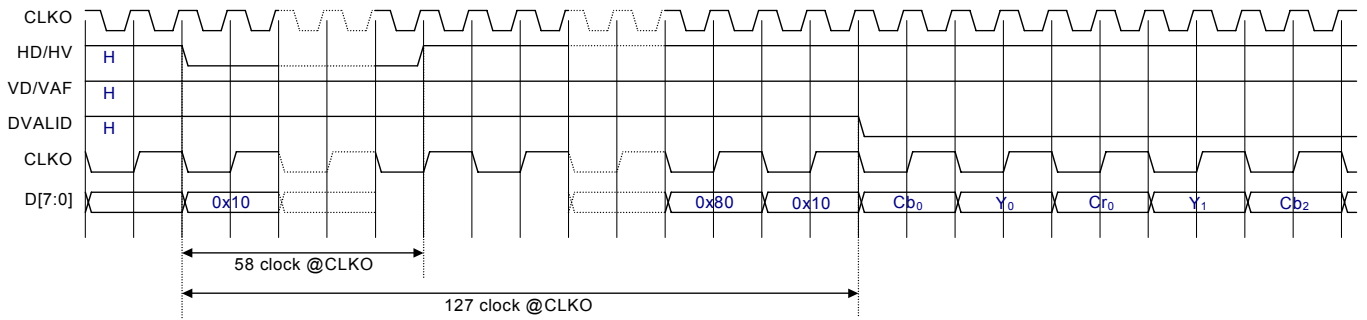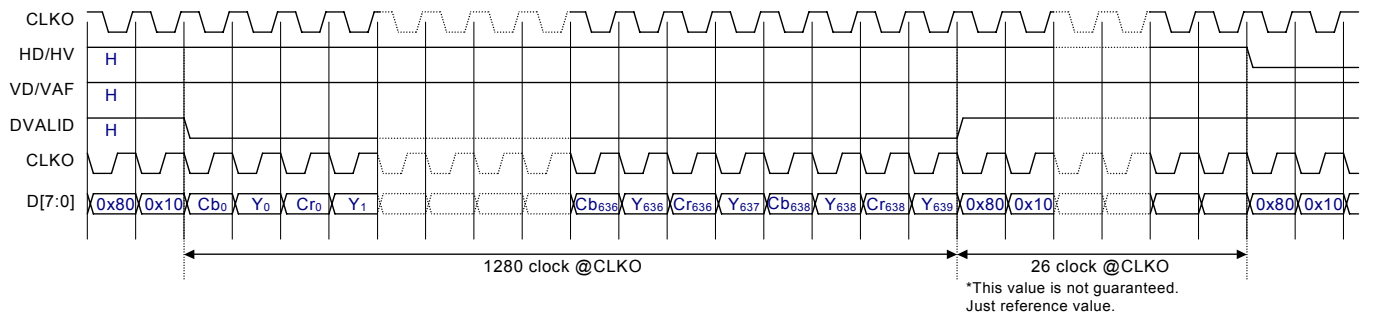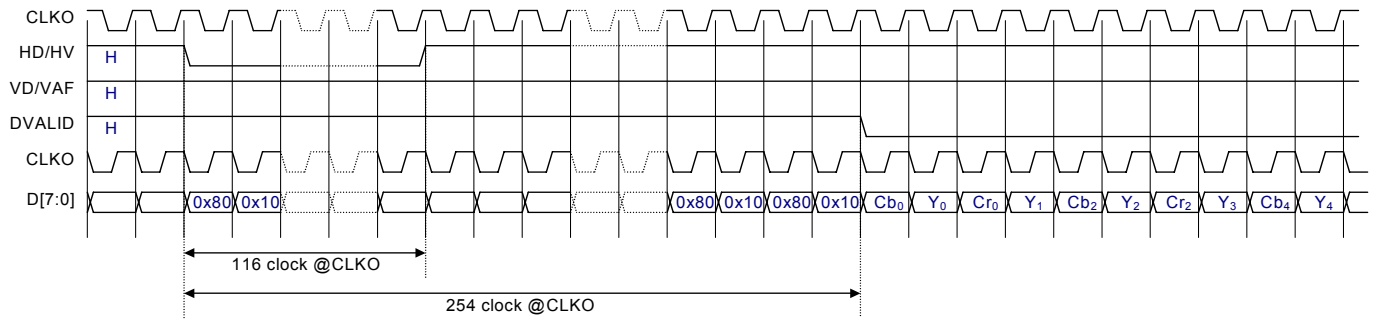Timing Chart   QVGA (PAL)   Register Set: VLF = 1'b1, OFORM[2:0] = 3'b000, OIF[1:0] = 2'b10

58 clock @CLKO

127 clock @CLKO

640 clock @CLKO

13 clock @CLKO

*This value is not guaranteed.
Just reference value.

Timing Chart   VGA (PAL)   Register Set : VLF = 1'b1, OFORM[2:0] = 3'b001, OIF[1:0] = 2'b10

CLKO
HD/HV H
VD/VAF H
DVALID H
CLKO
D[7:0]   0x80 0x10   0x80 0x10 0x80 0x10 Cb_0 Y_0 Cr_0 Y_1 Cb_2 Y_2 Cr_2 Y_3 Cb_4 Y_4

116 clock @CLKO

254 clock @CLKO

CLKO
HD/HV H
VD/VAF H
DVALID H
CLKO
D[7:0] 0x80 0x10 Cb_0 Y_0 Cr_0 Y_1 Cb_{636} Y_{636} Cr_{636} Y_{637} Cb_{638} Y_{638} Cr_{638} Y_{639} 0x80 0x10   0x80 0x10

1280 clock @CLKO

26 clock @CLKO
*This value is not guaranteed.
Just reference value.

Timing Chart   CIF (PAL)   Register Set: VLF = 1'b1, OFORM[2:0] = 3'b010, OIF[1:0] = 2'b10

CLKO

HD/HV   H

VD/VAF   H

DVALID   H

CLKO

D[7:0]   0x80   0x80   0x10 Cb_0 Y_0 Cr_0 Y_1 Cb_2

64 clock @CLKO

140 clock @CLKO

CLKO

HD/HV   H

VD/VAF   H

DVALID   H

CLKO

D[7:0] Cb_0 Y_0 Cb_{350} Y_{350} Cr_{350} Y_{351} 0x80   0x80

704 clock @CLKO   20 clock @CLKO
This value is not guaranteed.
Just reference value.

Timing Chart　　QCIF (PAL)　　　Register Set : VLF = 1'b1, OFORM[2:0] = 3'b011, OIF[1:0] = 2'b10
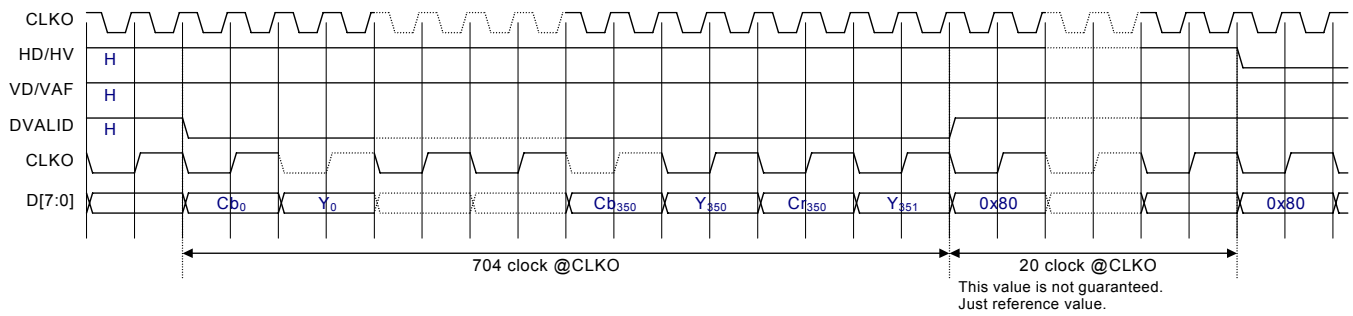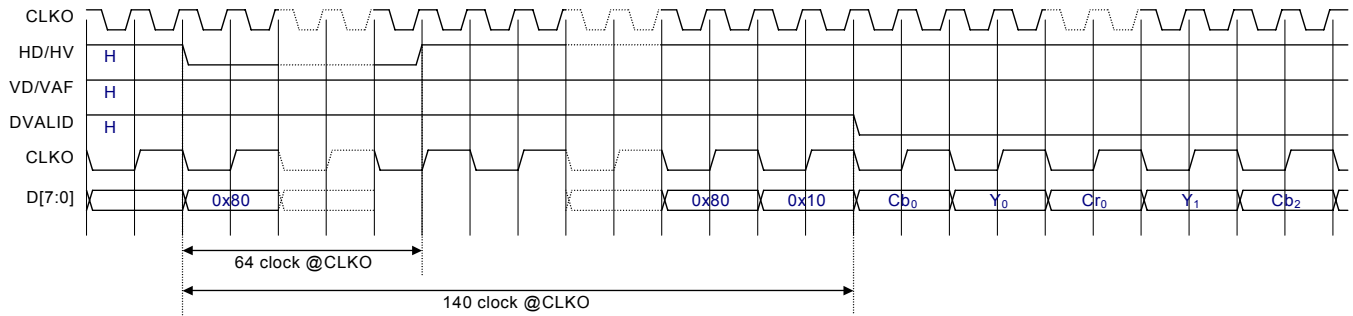
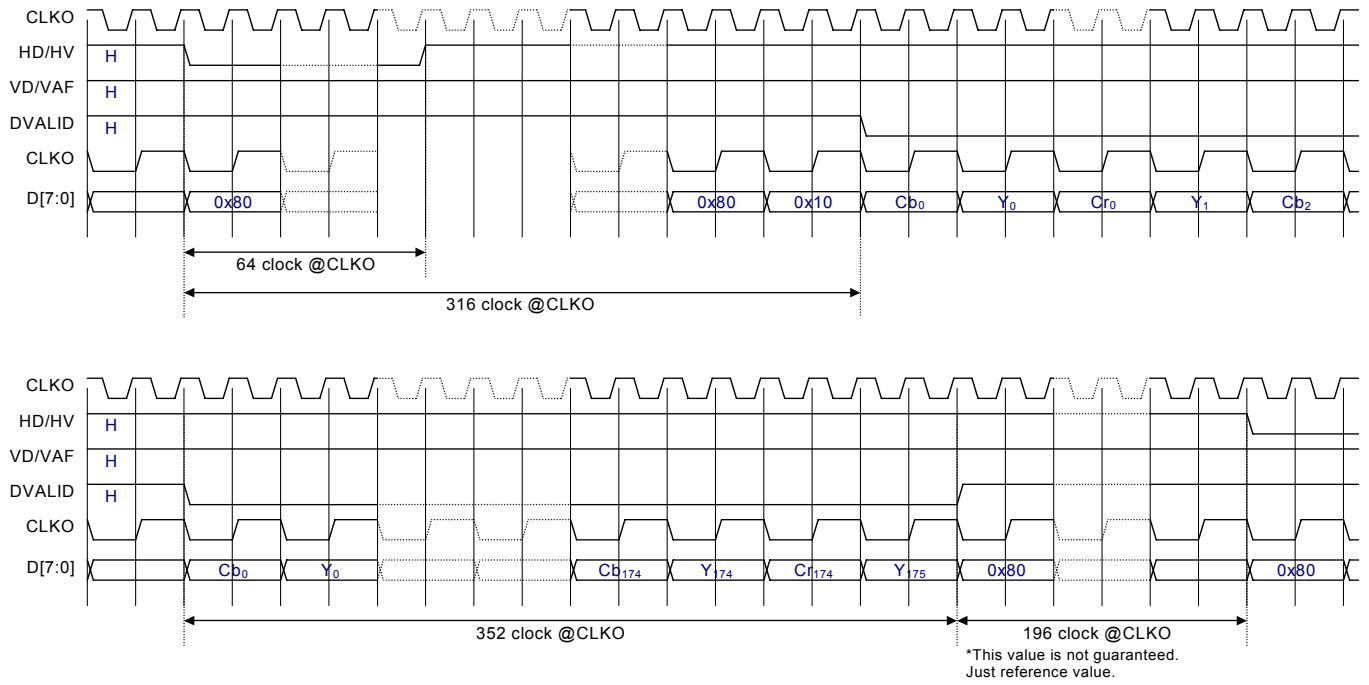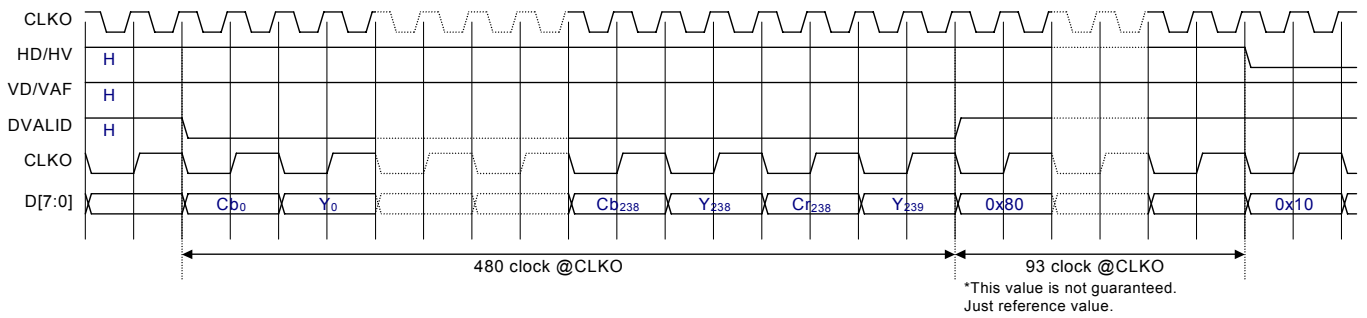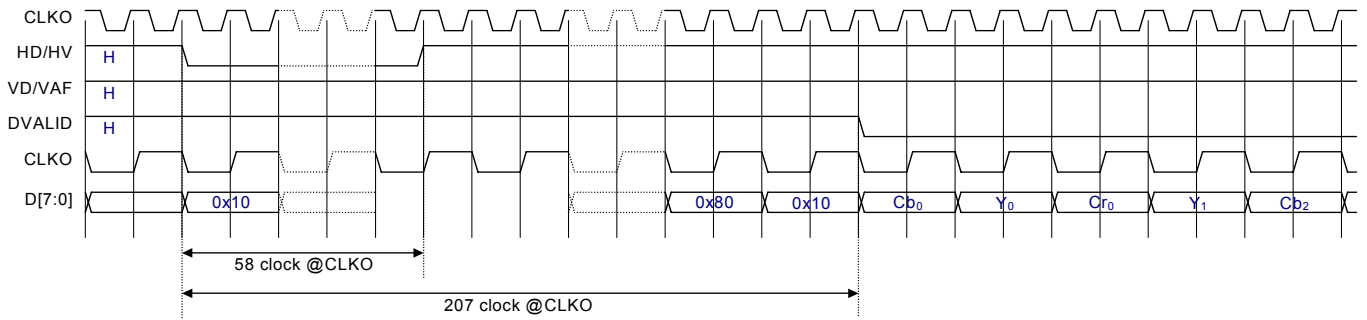Timing Chart   Rotated QVGA (PAL)   Register Set : VLF = 1'b1, OFORM[2:0] = 3'b100, OIF[1:0] = 2'b10

Timing Chart   Rotated CIF (PAL)   Register Set : VLF = 1'b1, OFORM[2:0] = 3'b101, OIF[1:0] = 2'b10

CLKO
HD/HV   H
VD/VAF   H
DVALID   H
CLKO
D[7:0]   0x10   0x80   0x10 Cb_0 Y_0 Cr_0 Y_1 Cb_2

58 clock @CLKO

159 clock @CLKO

CLKO
HD/HV   H
VD/VAF   H
DVALID   H
CLKO
D[7:0] Cb_0 Y_0 Cb_{286} Y_{286} Cr_{286} Y_{287} 0x80   0x10

576 clock @CLKO

45 clock @CLKO
This value is not guaranteed.
Just reference value.

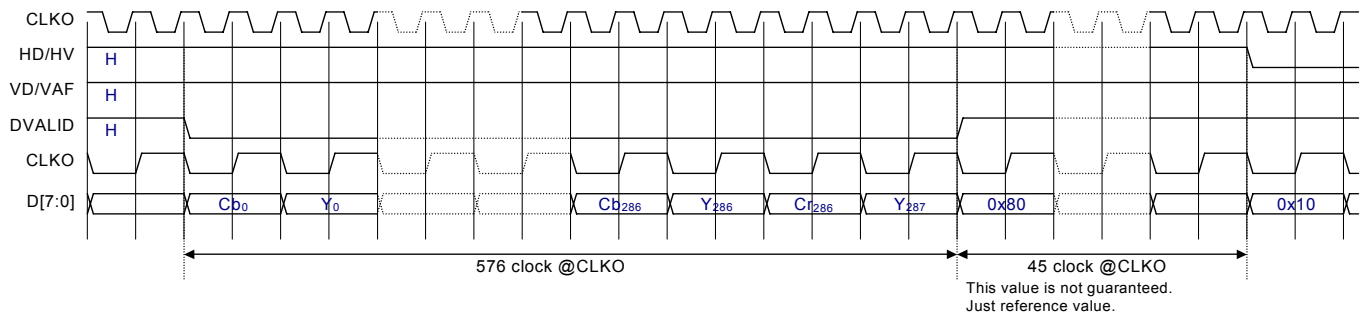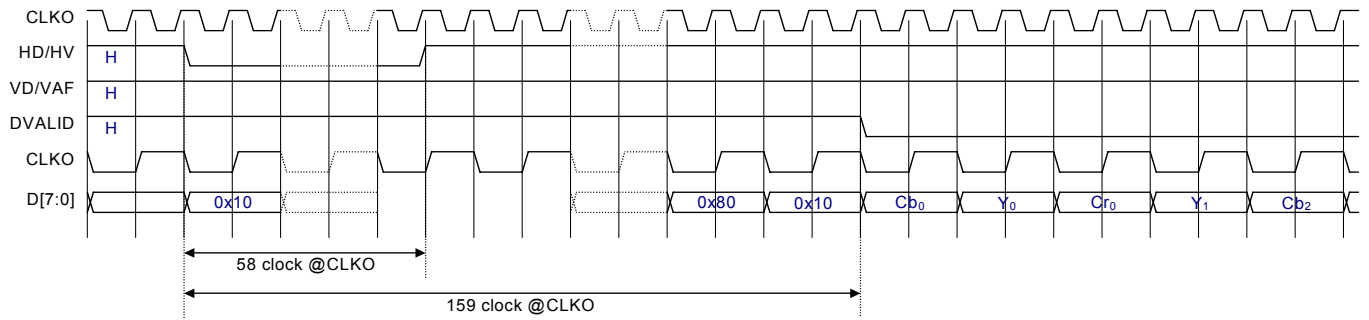Timing Chart   601output (PAL)   Register Set: VLF = 1'b1, OFORM[2:0] = 3'b110, OIF[1:0] = 2'b10

CLKO
HD/HV H
VD/VAF H
DVALID H
CLKO
D[7:0] 0x80 0x10 ... 0x80 0x10 0x80 0x10 Cb₀ Y₀ Cr₀ Y₁ Cb₂ Y₂ Cr₂ Y₃ Cb₄ Y₄

128 clock @CLKO
264 clock @CLKO

CLKO
HD/HV H
VD/VAF H
DVALID H
CLKO
D[7:0] 0x80 0x10 Cb₀ Y₀ Cr₀ Y₁ ... Cb₇₁₆ Y₇₁₆ Cr₇₁₆ Y₇₁₇ Cb₇₁₈ Y₇₁₈ Cr₇₁₈ Y₇₁₉ 0x80 0x10 ... 0x80 0x10

1440 clock @CLKO   24 clock @CLKO
*This value is not guaranteed.
Just reference value.

(3) 656 Interface

The AK8856 is designed for applications where the video data is typically processed with an MPEG algorithm. As such, it is capable of supporting a specific subset of the BT656 data interface. In 656 mode, the AK8856 generates synchronization codes SAV and EAV to indicate active video data. These codes are interpreted by the external digital video processor. In this mode, HD, DV, and DVALID signals are held low. The HD and DV signals can be read through a register setting.

The relationship between the interface and the output format register is described here. Related registers are [OFORM1 : OFORM0] bits and [OIF2 : OIF0] bits of the **Output Control 1 Register (R/W) [Sub Address 0x01]**.

Interface modes are set, regardless of OFORM register setting.
OIF[0] =   1'b0 : without SAV/EAV
           1'b1 : with SAV/EAV (at OFORM [2:0] = = 3'b 110 ", ITU-R BT.656)
OIF[1] =   1'b0 : Camera I/F
           1'b1 : HD/VD/DVALID I/F

The Rec.656 mode supported by the AK8855 can be ITU-R BT. 656 compatible by setting OIF with SAV / EAV code (OIF [0] = = 1'b 1) when OFORM [2:0] = = 3' b 110. In all other codes, the V-bit of SAV / EAV becomes "0" during Vertical Active Video region only.

When OIF [1:0] = = 2'b 11, the interface mode is HD / VD / DVALID interface with SAV / EAV code in the AK8856. In addition, when OFORM [2:0] = = 3'b 110, SAV / EAV is output in ITU-R BT.656 compatible fashion.

By setting the [TRSVSEL] bit of the **Output Control 1 Register (R/W) [Sub Address 0x01]**, it is possible to change the V-bit shift point of the 656 specified Video Timing Reference code (SAV / EAV) separately from the values referred to in the previous section. By properly setting the [TRSVSEL] bit, it is possible to make the shift point of V-bit compatible with ITU-R BT.656-3 or ITU-R BT.656-4 and SMPTE125M.

Bit allocation of **Output Control 1 Register**

Sub Address 0x01   Default Value : 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDPSUP	TRSVSEL	OIF1	OIF0	LIMIT601	OFORM2	OFORM1	OFORM0
Default Value							
0	0	0	0	0	0	0	0

[TRSVSEL] bit
This is a control bit to specify V-bit handling in the Rec 656 EAV / SAV code.
    <V-bit value in Rec. 656 TRS signal and Line relation>

V-bit	NTSC(525Lines)		PAL(625Lines)	
	TRSVSEL = 0 Based on ITU-R Bt.656-3	**TRSVSEL = 1 Based on ITU-R Bt.656-4 and SMPTE125M**	**TRSVSEL = 0**	**TRSVSEL = 1**
V-bit = 0	Line10 ~ Line263 Line273 ~ Line525	Line20 ~ Line263 Line283 ~ Line525	Line23 ~ Line310 Line336 ~ Line623	
V-bit = 1	Line1 ~ Line9 Line264 ~ Line272	Line1 ~ Line19 Line264 ~ Line282	Line1 ~ Line22 Line311 ~ Line335 Line624 ~ Line625	

(4) Field Signal Output

The field signal can be output on VD / VAF /FIELD signal output pin. Output signal selection between VD / VAF signal and FIELD signal is done by **Control 1 Register (Sub Address 0x03)**.

Pin output and Field relation:

FIELD Signal State	Field Information
Low	Odd
High	Even

The value of the Field signal is determined during DVALID active. The Field signal does not directly reflect the input field, but it is a field signal which is forced to toggle at each VSYNC signal. Therefore, even when Odd Field or Even Field only signal is input, the Field signal also toggles.

Switching Timing between Field signal and VD signal:

NTSC
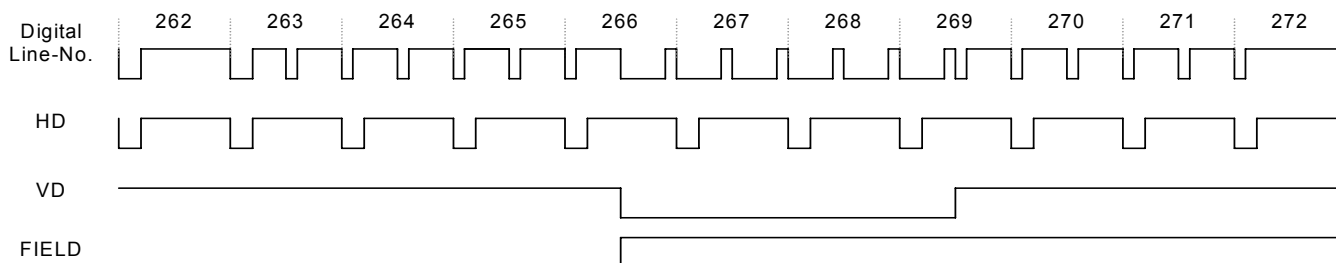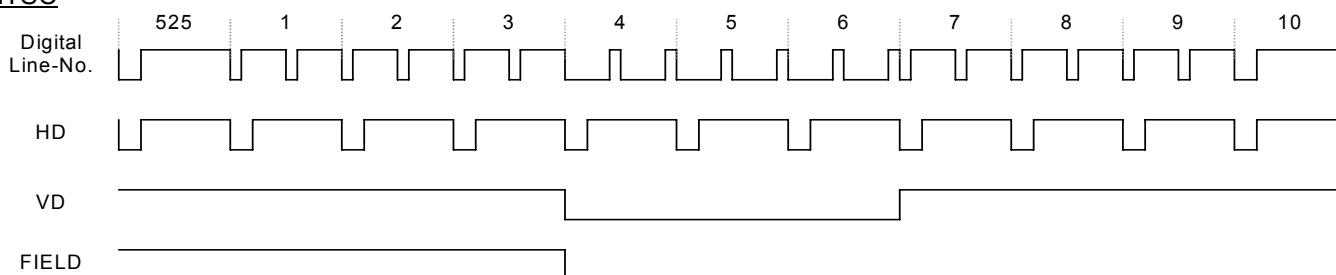
PAL

Variable Frame Rate Function

The AK8856 can vary the output frame rate. The frame rate can be selected by the [FRMRT1 : FRMRT0] bits of
Control 2 Register (R/W) [Sub Address0x04]

NTSC : 30 / 15 / 7.5 [fps]
PAL : 25 / 12.5 / 6.25 [fps]

Output timing is illustrated here. (■ indicates "active")

QVGA, CIF, QCIF, Rotated QVGA, Rotated CIF

VGA,601
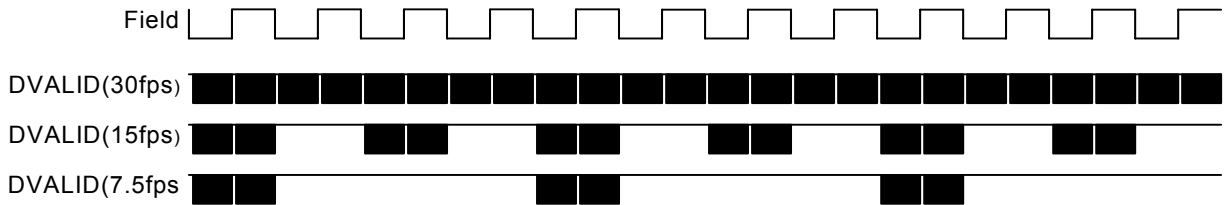
Note 1: These diagrams are typical for OFORM and OIF modes.
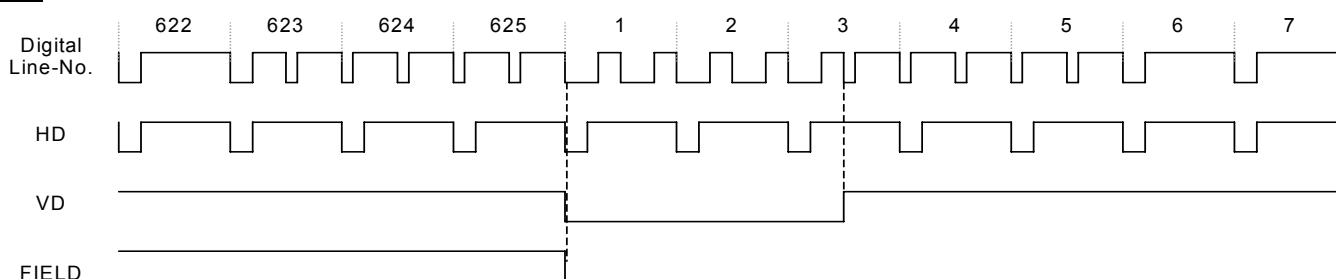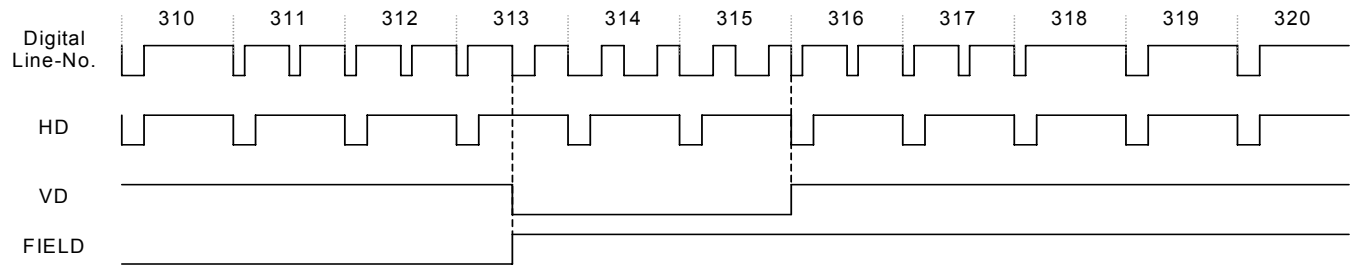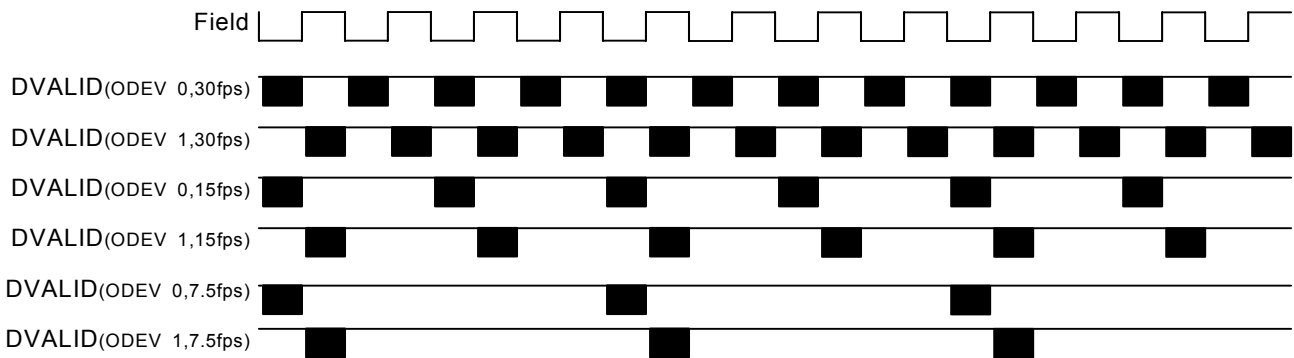Note 2: When OIF [1:0] = 2'b 10 is set, VD pulse is not output at the default setting. However, HD pulse and DVALID signal
are output at the FIELD (Frame) where video is not output. In this case, the data is Black level data (Y : 0x10, Cb / Cr : 0x80).
In order to output VD pulse in this mode, set the VDPSUP-bit of **Output Control 1 Register (R/W) [Sub Address 0x01].**

Note 2: When OIF [1:0] = 2'b 10 is set, VD pulse is not output at the default setting. However, HD pulse and DVALID signal
are output at the FIELD (Frame) where video is not output. In this case, the data is Black level data (Y : 0x10, Cb / Cr : 0x80).
In order to output VD pulse in this mode, set VDPSUP-bit of **Output Control 1 Register (R/W) [Sub Address 0x01].**

Note 3: In VGA or 601 mode, ODEV setting does not affect output.
Note 4: When Vertical Sync is disturbed during switching signals., this timing may not be valid.

Setting of [VDPSUP-bit]

VDPSUP-bit condition	VD pulse output	Note
0	To output VD pulse during Active Frames only.	
1	To output VD pulse even at other than Active Frames.	

Digital Pixel Interpolator

The Digital Pixel Interpolator is used to align vertical pixels (the interpolation block used is not compatible with the AK8855/AK8880. The AK8856 Interpolator is the same one used for theAK8851).

YC Delay

YC delay time is adjustable. In tuner output mode, there is a condition where the C signal is delayed from the Y signal. The adjustable YC Delay function is effective for this condition. The delay amount is adjustable with a single, internal processing clock unit. The setting is in 2's complement format.

The delay amount is adjusted by setting the **YC Delay Control Register (R/W) [Sub Address 0x0B]**.

Sub Address 0x0B   **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	YCDELAY2	YCDELAY1	YCDELAY0
Default Value							
0	0	0	0	0	0	0	0

YCDELAY2 :YCDELAY0	Delay amount	Note
101	Y is delayed from C by 3 clock cycles	Delay amount depends on the selected output mode. VGA/QVGA/QVGA Rotated/CIF Rotated : 12. 2727 MHz 601/CIF/QCIF : 13.5 MHz Delay amount is based on the selected clock mode.
110	Y is delayed from C by 2 clock cycles	
111	Y is delayed from C by 1 clock cycles	
000	No delay between Y and C	
001	Y is advanced from C by 1 clock cycles	
010	Y is advanced from C by 2 clock cycles	
011	Y is advanced from C by 3 clock cycles	

Notification Function of Internal Conditions

The AK8856 has a **Status Register (R/W) [Sub Address 0x10]** to notify externally the AK8856 internal condition. Bit allocation of **Status Register** is as follows.

Sub Address 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBWSSDET	EXTDET	CCDET	AGCSTS	VLOCKSTS	PKWHITE	COLKILST	NSIG

(1) No Signal Decision
The AK8856 detects when no signal input is present. When there is no input signal, the data output goes to Black level output (Y = 0x10, Cr / Cb = 0x80). This result is flagged by the output pin NSIG and the [NSIG] bit of **Status Register**. The output logical state is:

Signal condition	[NOSIG] bit	NSIG pin
With signal input	0	0
No signal input	1	1

(2) COLKILST
This indicates that the Color Killer Function has been activated, since the color signal level is very small.

[COLKIL]-bit	Input level	Condition
0	Normal signal	
1	Color Killer is enabled	

(3) Input Level Overflow Notification Function
This function is activated when the numerical result of the luminance signal exceeds 255.

[PKWHITE] bit
When an overflow of the luminance signal is detected, this bit is set to "1".

[PKWHITE]- bit	Input level	Condition
0	Input signal overflow occurred	
1	No input overflow occurred	

(4) Color PLL Status
This indicates a PLL lock condition with the input Color Burst signal.
[CPLLLCK] bit

[CPLLLCK] bit	Input level	Condition
0	Locked with input Color Burst signal	
1	Not locked with input Color Burst signal	

(5) AGC Status
This indicates the status of adaptive AGC.
[AGCSTS] bit

[AGCSTS]-bit	Input level	Condition
0	Operating in Sync AGC	
1	Operating in Peak AGC	

No Input Signal Condition

Two output modes can be selected when no Video signal is input to the AK8856. The default value is Black code output. This is set by the NSIGMD-bit of **Output Control 2 Register (R/W) [Sub Address 0x02]**. Detection of a no signal condition is indicated by a hardware pin and the **Status Register (R / W) [Sub Address 0x10]**.

[NSIGMD] bit
This sets the output signal when no input signal is detected.

[NSIGMD]-bit	Output signal when no signal is input	Condition
00	Black code output	Y = 0x10 Cb/Cr = 0x80
01	Blue back output	
10	Input signal is directly output as is.	So-called " Sand-Storm " mode output.
11	Reserved	

Power-Down Mode

The AK8856 has a power-saving wait mode function. The PDN pin is used to put the AK8856 into power-saving mode, including the digital block. By setting this pin low, all blocks in the analog and digital blocks are put into power-saving mode. After recovering from power-saving mode by resetting the PDN pin, a reset sequence must be executed.

When reducing power supplies (except PVDD), a power-down sequence must be followed by setting the PDN pin and then reducing AVDD and DVDD after the power-down condition is established. During power-down mode, digital output pins should be tied to the PVDD power supply, or set the OE pin = high (high output).

Output Pin Condition

Output pins of the AK8856 are controlled by the OE (Output Enable) pin and RSTN pin conditions.

Output pin conditions:

	After Power up	RSTN = Low	After Reset Sequence	
			PDN = Low	PDN = High
OE = High	unknown	Hi-z	High	Data output
OE = Low	Hi-z	Hi-z	Hi-z	Hi-z

Device Control Interface

The AK8855 is controlled through an I^{2}C Bus Control Interface.

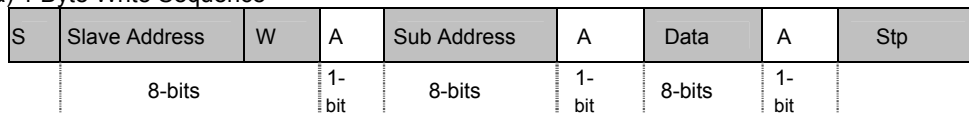**[I^{2}C SLAVE Address]**
I^{2}C Slave Address is 0x88

A6	A5	A4	A3		A2	A1	A0	R/W
1	0	0	0		1	0	0	

[I^{2}C Control Sequence]
(1) Write Sequence

When the Slave Address of the AK8856 Write Mode is received at the first byte, Sub Address at the second byte and Data at the third and succeeding bytes are received. There are two operations in the Write Sequence - a sequence to write at every single byte, and a sequential write operation to write multiple bytes successively.

(a) 1 Byte Write Sequence

S	Slave Address	W	A	Sub Address	A	Data	A	Stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	

(b) Multiple Bytes (m-bytes) Write Sequence (Sequential Write Operation)

S	Slave Address	w	A	Sub Address(n)	A	Data(n)	A	Data(n+1)	A	---	Data(n+m)	A	stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit		8-bits	1-bit	
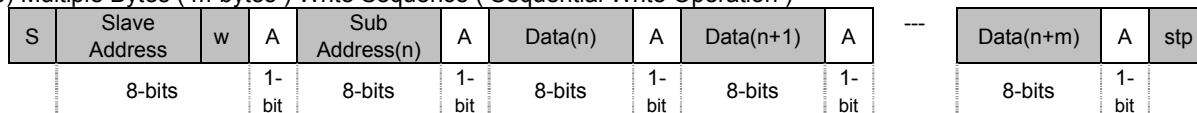
(2) Read Sequence
When the Slave Address of the AK8855 Read mode is received, Data at the second and succeeding bytes are transmitted.

S	Slave Address	w	A	Sub Address(n)	A	rS	Slave Address	R	A	Data1	A	Data1	A	Data2	A	---	Data n	Ā	stp
	8-bits	1		8-bits	1		8-bits		1	8-bits	1	8-bits	1	8-bits	1		8-bits	1	
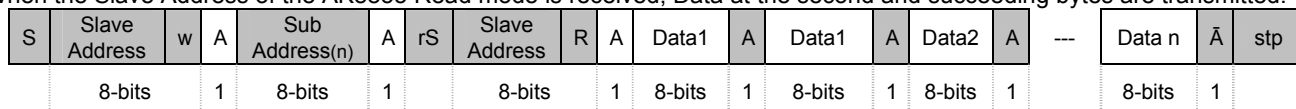
Note) At Sequential Read Operation, the first byte Read-out Data is repeatedly output (this does not occur in a normal, single byte Read operation).

Abbreviated terms listed in the tables :

S, rS   : Start Condition
A   : Acknowledge (SDA Low)
A-   : Not Acknowledged (SDA High)
stp   : Stop Condition
R/W   1 : Read   0 : Write
          : Controlled by the Master Device; micro-computer interface is output.
          : Controlled by the Slave Device; output by the AK8856.

Register Definition

Sub Address	Register	Default	R/W	Function
0x00	Input video standard register	0x00	R/W	Sets standard input signal
0x01	Output control 1 register	0x00	R/W	Sets output picture size
0x02	Output control 2 register	0x00	R/W	Sets output pin characteristics
0x03	Control 1 register	0x00	R/W	Sets YC separation, color killer, AGC, VD field
0x04	Control 2 register	0x00	R/W	Sets AGC, color killer, frame rate, contrast mode
0x05	PGA control register	0x15	R/W	Sets PGA parameters
0x06	Contrast control register	0x80	R/W	Sets contrast level
0x07	Brightness control register	0x00	R/W	Sets brightness level
0x08	Saturation control register	0x80	R/W	Sets saturation level
0x09	HUE control register	0x00	R/W	Sets Hue level
0x0A	Request VBI info register	0x0A	W	Requests VBI information
0x0B	YC Delay control register	0x00	R/W	Controls YC delay
0x10	Status register		R	Status register
0x11	Macrovision status register		R	Macrovision Status register
0x12	Closed caption 1 register		R	Closed Caption Data 1 register
0x13	Closed caption 2 register		R	Closed Caption Data 2 register
0x14	Extended data 1 register		R	Closed Caption Extended Data 1 register
0x15	Extended data 2 register		R	Closed Caption Extended Data 2 register
0x16	VBID/WSS 1 register		R	VBID (CGMS-A) / WSS1 Data register
0x17	VBID/WSS 2 register		R	VBID (CGMS-A) / WSS 2 Data register
0x18	Device & revision ID & mode status register	0x80	R	Device & Revision ID register

Input Video Standard Register (R/W) [Sub Address 0x00]
Sets input signal

Sub Address 0x00   **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	AINSEL	VLF	VCEN	VSCF1	VSCF0
Default Value							
0	0	0	0	0	0	0	0

Input Video Standard Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	VSCF0 ~ VSCF1	Sub carrier Frequency	R/W	**Sets Sub-carrier frequency of input video signal** VSCF1 - VSCF0 [MHz] 00 : 3.57954545 01 : 3.57561188 10 : 3.5820558 11 : 4.43361875
bit 2	VCEN	Video Color Encode	R/W	**Sets Color Encoding System of input video signal** 0: NTSC 1: PAL
bit 3	VLF	Video Line Frequency	R/W	to set Line Frequency of input video signal. 0 : 525 Lines 1 : 625 Lines
bit 4	AINSEL	AIN Select bit	R/W	to select AIN Input Select switch. 0: to decode AIN 1 1: to decode AIN 2
bit 5 ~ bit 7	Reserved	Reserved	R/W	Reserved

Output Control 1 Register (R/W) [Sub Address 0x01]

Sub Address 0x01   **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VDPSUP	TRSVSEL	OIF1	OIF0	LIMIT601	OFORM2	OFORM1	OFORM0
Default Value							
0	0	0	0	0	0	0	0

Output Control 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	OFORM0 ~ OFORM2	Output Format Set bit	R/W	**Set output picture size:** OFORM[2:0] 000: QVGA 001: VGA (interlaced output) 010: CIF 011: QCIF 100: rotated QVGA (240 X 180) 101: rotated CIF (288 X 216) 110: 601 output 111: Reserved
bit 3	LIMIT601	601 Output Limit	R/W	**Sets Minimum / Maximum limit for output data:** 0 : 1-254 (Y/Cb/Cr) 1 : 16-235 (Y) / 16-240 (Cb/Cr) when "1" is set in the LIMIT601 register, data smaller than 16 is clipped to 16 and data larger than 235 / 240 (Y / Cb, Cr) is clipped to 240.
bit 4 ~ bit 5	OIF0 ~ OIF1	Output interface set bit	R/W	**Sets output interface mode**: 00: Camera Interface mode (without SAV / EAV) 01: Camera Interface mode (with SAV / EAV) 10: HD / VD mode 11: 656 Interface mode In modes 01 / 11, HD / VD output is fixed low.
bit 6	TRSVSEL	Time Reference Signal V Select bit	R/W	**Switches shift line of V-bit of EAV / ASAV which is included in TRS:** This register is valid when OFORM [2:0] = 110. NTSC system (525 line input) TRSVSEL=0 : V = 1 when Line 1 ~ Line 9 / Line 264 ~ Line 272 V = 0 when Line 10 ~ Line 263 / Line 272 ~ Line 525 TRSVSEL=1: V = 1 when Line 1 ~ Line 19 / Line 264 ~ Line 282 V = 0 when Line 20 ~ Line 263 / Line 283 ~ Line 525 PAL system (625 line input) Regardless of the set value of the TRSVSEL bit, V = 1 when Line 1 ~ Line 22 / Line 311 ~ Line 355 / Line 624 ~ Line 625 V = 0 when Line 23 ~ Line 310 / Line 336 ~ Line 623
bit 7	VDPSUP	VD Pulse SUPress	R/W	When Frame Rate Variable Function is activated in HD / VD mode and 656 I / F mode, 0 : VD / VAF pulse is not output at the frames that are not active. 1 : VD / VAF pulse is output even at the Frames which are not active.

Output Control 2 Register (R/W) [Sub Address 0x02]

Sets polarity of output pin and to set output condition when no input signal is fed.

Functional modification has been made on bit 7 of this register from the AK8855.

Sub Address 0x02   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NSIGMD1	NSIGMD0	DVALACT	HVACT	CLKINV	DVALIDP	VDP	HDP
Default Value							
0	0	0	0	0	0	0	0

Output Control 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0	HDP	HD pin Polarity set bit	R/W	**Sets polarity of HD signal:** 0: Active Low 1: Active High
bit 1	VDP	VD pin Polarity set bit	R/W	**Sets polarity of VD signal:** 0: Active Low 1: Active High
bit 2	DVALDP	DVALID pin Polarity set bit	R/W	**Sets polarity of DVALID signal:** 0: Active Low 1: Active High
bit 3	CLKINV	CLK invert set bit	R/W	**Sets polarity of CLKO:** 0: normal output (data should be taken at the rising edge) 1: phase relation between data and clock is inverted (data should be taken at the falling edge).
bit 4	HVACT	HD/VD action bit	R/W	**Outputs HD & VD in EAV / SAV Interface mode:** no output (fixed to low) 1 : to output
bit 5	DVALACT	DVALID action bit	R/W	**Outputs DVALID signal in EAV / SAV Interface mode:** 0: no output (fixed to low) 1: to output
bit 6 ~ bit 7	NSIGMD0 ~ NSIGMD1	No SiGnal Output MoDe	R/W	**Sets output condition when no signal input condition is detected:** 　00 : Output Black level 　01 : Output Blue level (Blue back) 　10 : Output input condition directly as is(" Sand-Storm " condition). 　11 : Reserved

Control 1 Register (R/W) [Sub Address 0x03]
Control Register

Sub Address 0x03   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	VDFLD	AGCTR	AGCC1	AGCC0	CKILSEL1	CKILSEL0	YCSEP
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0	YCSEP	YC Separation Set bit	R/W	**Selects YC separation method:** Operation of YC separation is fixed by a selected input signal type and output data size. For NTSC & QVGA,CIF,QCIF, QVGAL,CIFL: 0 : primary YC separation (AK8855 compatible) 1 : Y by primary YC separation filter and C by two dimensional YC separation filter
bit 1 ~ bit 2	CKILSEL0 ~ CKILSEL1	Color killer Select bit	R/W	**Sets " ON " condition of Color-Killer:** 00 : when at [01] condition or at [10] condition 01 : locked Color Decode PLL becomes out-of-lock condition. 10 : Color Burst signal level becomes lower than approximately –23 dB. 11 : Reserved
bit 3 ~ bit 4	AGCC0 ~ AGCC1	AGC Coring Level	R/W	**Sets AGC Coring level** 00 : +/_ 2 LSB Coring level 01 : +/_ 3 LSB Coring level 10 : +/_ 4 LSB Coring level 11 : no Coring level
bit 5	AGCTR	AGC Transient Level	R/W	**Sets transient conditions of Sync AGC and Peak AGC:** 0 : Quick 1 : Slow
bit 6	VDFLD	VD Field Select bit	R/W	**Sets the type of output signal on VD / VAF / FIELD pin:** VAF signal is always output on this pin in Camera interface mode. 0 : VD / VAF signal is output 1 : FIELD signal is output
bit 7	Reserved	Reserved bit	R/W	

Control 2 Register (R/W) [Sub Address 0x04]
Control Register

Sub Address 0x04   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNTSEL	NSIGDEF	ODEV	FRMRT1	FRMRT0	COLKIL	ACC	AGC
Default Value							
0	0	0	0	0	0	0	0

Control 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0	AGC	AGC set bit	R/W	0 : AGC Disable (PGA manual setting is enabled) 1 : AGC Enable
bit 1	ACC	ACC set bit	R/W	0 : ACC Disable 1 : ACC Enable
bit 2	COLKIL	Color Killer Set bit	R/W	0 : Color Killer enabled 1 : Color Killer disabled
bit 3 ~ bit 4	FRMRT0 ~ FRMRT1	Frame Rate Set bit	R/W	Sets Frame Rate [Frames / sec] FRMRT 1:0 (525 / 625) 00: 30/25 01: 15/12.5 10: 7.5/6.25 11: Reserved
bit 5	ODEV	ODD Even Select bit	R/W	**Sets decode field for QVGA / CIF / QCIF decoding:** 0 : Decode Odd Field 1 : Decode Even Field
bit 6	NSIGDEF	NSIG Define Mode	R/W	Sets NSIG pin output condition. 0 : when both Horizontal and Vertical synchronizations lose sync, NSIG goes high (output shifts to self-running mode) 1 : when Vertical synchronization loses sync, NSIG goes high
bit 7	CNTSEL	Contrast mode select bit	R/W	Sets the start point for contrast adjustment 0 : Contrast varies, starting at Luminance level of 128 (gray) as a center value 1 : Contrast varies, starting at Luminance level of 16 (black) as a center value

PGA Control Register (R/W) [Sub Address 0x05]
Sets PGA gain; when the AGC function is enabled, the gain value for the AGC is set by this register.

Sub Address 0x05   **Default Value: 0x15**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PGA6	PGA5	PGA4	PGA3	PGA2	PGA1	PGA0
Default Value							
0	0	0	1	0	1	0	1

PGA Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 6	PGA0 ~ PGA6	PGA Gain Set	R/W	Sets gain of PGA: PGA can be adjusted in approximately 0.1 dB / step.
bit 7	Reserved	Reserved	R/W	Reserved

Note) When reading this register while the AGC is enabled, the PGA value which is set by AGC is returned. It is possible for the user to write a value (user-set-value) while the AGC is enabled, but its value is not written to the PGA. A returned value from the register read operation is the same AGC set value. When the AGC is disabled, the user-set-value is valid, and its value is returned by a Register Read operation.

Contrast Control Register (R/W) [Sub Address 0x06]
This register is for Contrast Adjustment, and the default value (no adjustment) is 0x80.

Sub Address 0x06   **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Default Value							
1	0	0	0	0	0	0	0

Contrast Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CONT0 ~ CONT7	Contrast Control	R/W	Contrast Adjustment: resolution is 1 / 256 step and the range is from 0 to 255 / 128. Default value is 0x80.

Brightness Control Register (R/W) [Sub Address 0x07]
This register is for Brightness Adjustment and the default value (no adjustment) is 0x00.

Sub Address 0x07   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
Default Value							
0	0	0	0	0	0	0	0

Brightness Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	BR0 ~ BR7	Brightness Control	R/W	Brightness Adjustment: Two's complement format

Saturation Control Register (R/W) [Sub Address 0x08]
This register is for Color Saturation Adjustment, and the default value (no adjustment) is 0x80.

Sub Address 0x08   **Default Value: 0x80**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default Value							
1	0	0	0	0	0	0	0

Saturation Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SAT0 ~ SAT7	Saturation Control	R/W	Saturation Adjustment: resolution is 1/256 step and the range is from 0 to 255/128. SAT7:SAT0 0 : 0 x (no color exists) 0xff : 255/128 x 0xff : 255/128 x

HUE Control Register (R/W) [Sub Address 0x09]

This register is for Hue Adjustment, and the default value (no adjustment) is 0x00.

Sub Address 0x09   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
Default Value							
0	0	0	0	0	0	0	0

HUE Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	HUE0 ~ HUE7	HUE Control	R/W	Hue adjustment: two's complement format. Default value is 0x00. Resolution is 1/256 step (approximately 0.35° / step), with a range of ±45°.

Request VBI Info Register (W) [Sub Address 0x0A]

This register is used to decode VBLANK information, including Closed Caption Data, Extended Data, VBID (CGMS), and WSS Data.

When a "1" is written to the decode request bit for VBLANK information, the AK8856 is put into Data Decode Ready state and waits for Data. After decoding is completed, a "1" is written to the CCDET bit, the EXTDET bit, and the VBWSSDET bit. These bits correspond to a **Status Register (R / W) [Sub Address 0x10]** request, and decoded data are written to the Closed Caption Data 1 / 2 Registers, Extended Data 1 / 2 Registers and VBID / WSS Data 1/ 2 Registers respectively.

Sub Address 0x0A   **Default Value: 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	VBWSRQ	EXTRQ	CCRQ
Default Value							
0	0	0	0	0	0	0	0

Request VBI Info Register Definition

BIT	Register Name		R/W	Definition
bit 0	CCRQ	Closed Caption Data Decode Request	W	Request decoding of Closed Caption Data 0 : - 1 : decode request
bit 1	EXTRQ	Extended Data Decode Request	W	Request decoding of Extended Data 0 : - 1 : decode request
bit 2	VBWSRQ	VBID Data Decode Request	W	Request decoding of VBID / WSS Data 0 : - 1 : decode request
bit 3 ~ bit 7	Reserved	Reserved	W	Reserved

Note) When a "1" is written to the RQ-bit, CCDET, EXTDET, and VBWSSDET bits are cleared to "0", which corresponds to a Status Register Request.

YC Delay Control Register (R/W) [Sub Address 0x0B]

YC Delay Control Register Definition

Sub Address 0x0B **Default Value : 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	YCDELAY2	YCDELAY1	YCDELAY0
Default Value							
0	0	0	0	0	0	0	0

YC Delay Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	YCDELAY0 ~ YCDELAY2	Y/C Delay Control	R/W	Adjusts amount of Y/C output delay; Delay amount depends on the selected output mode. VGA/QVGA/QVGA Rotated/CIF Rotated : 12.2727MHz clock cycles per each one delay (81.5ns) 601/CIF/QCIF : 13.5MHz sample clock cycles per each one delay (74 ns) YCDELAY2 : YCDELAY0 101 : Y is delayed from C by 3 clock cycles 110 : Y is delayed from C by 2 clock cycles 111 : Y is delayed from C by 1 clock cycles 000 : no delay between Y and C 001 : Y is advanced from C by 1 clock cycles 010 : Y is advanced from C by 2 clock cycles 011 : Y is advanced from C by 3 clock cycles
bit 3 ~ bit 7	Reserved	Reserved bit	R/W	Reserved

Status Register (R/W) [Sub Address 0x10]
Register to indicate internal conditions of the AK8856.

Sub Address 0x10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBWSSDET	EXTDET	CCDET	AGCSTS	VLOCKSTS	PKWHITE	COLKILST	NSIG

Status Register Definition

BIT	Register Name		R/W	Definition
bit 0	NOSIG	No Signal	R	Detects presence of input signal. 0 : signal is being input 1 : no signal input condition
bit 1	COLKILST	Color killer	R	Status of Color Killer 0 : Color Killer is in-active 1 : Color Killer process is active
bit 2	PKWHITE	Peak White Detection	R	Detects input overflow by monitoring output of ADC 0 : normal 1 : input level overflow
bit 3	VLOCKSTS	VLOCK Status bit	R	VLOCK status 0 : VLOCK is properly operating 1 : VLOCK is out-of-lock condition
bit 4	AGCSTS	AGC Status bit	R	0 : Sync AGC operation 1 : Peak AGC operation
bit 5	CCDET	Closed Caption Detect	R	Detects presence of decoded Closed Caption data in the Closed Caption ½ registers 0 : no Closed Caption Data exists 1 : decoded Closed Caption Data exists
bit 6	EXTDET	Extended Data Detect	R	Detects decoded data in Extended Data 1/2 Registers 0 : no Extended Data exists 1 : decoded Extended Data exists
bit 7	VBWSDET	VBID / WSS Data Detect	R	Detects decoded data in VBID/WSS Data 1/2 Registers. 0 : no VBID / WSS data exists 1 : decoded VBID / WSS data exists

Macrovision Status Register (R/W) [Sub Address 0x11]

Displays result of Macrovision signal detection.

Sub Address 0x11

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	PSPDET	AGCPDET	BPPDET	SYNCRED	CSTYPE	CSDET	AGCDET

Macrovision Status Register Definition

BIT	Register Name		R/W	Definition
bit 0	AGCDET	AGC Process Detect	R	Detects Macrovision AGC Process in input signal. 0 : no Macrovision AGC Process detected 1 : Macrovision AGC Process detected
bit 1	CSDET	Color Stripe Detect	R	Detects Macrovision Color Stripe Process in input signal. 0 : no Color Stripe process 1 : Color Stripe process is detected
bit 2	CSTYPE	Color Stripe Type	R	Displays types of Color Stripe in input signal 0 : Color Stripe Type 2 1 : Color Stripe Type 3
bit 3	SYNCRED	Sync Reduction bit	R	Detects Sync Reduction 0 : - 1 : Sync Reduction is detected
bit 4	BPPDET	Back Porch Pulse Detect bit	R	Detects end of Field Back Porch Pulse 0 : - 1 : end of Field Back Porch Pulse is detected
bit 5	AGCPDET	AGC Pulse Detect bit	R	Detects AGC Pulse 0 : - 1 : AGC Pulse is detected
bit 6	PSPDET	Pseudo Sync Pulse Detect bit	R	Detects Pseudo Sync Pulse 0 : - 1 : Pseudo Sync Pulse is detected
bit 7	Reserved	Reserved bit	R	Reserved

Closed Caption 1 Register (R) [Sub Address 0x12]
Register to store Closed Caption Data.

Sub Address 0x12

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Closed Caption 2 Register (R) [Sub Address 0x13]
Register for storing Closed Caption Data.

Sub Address 0x13

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

Extended Data 1 Register (R) [Sub Address 0x14]
Register for storing Closed Caption Extended Data.

Sub Address 0x14

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0

Extended Data 2 Register (R) [Sub Address 0x15]
Register for storing Closed Caption Extended Data.

Sub Address 0x15

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8

VBID/WSS 1 Register (R) [Sub Address 0x16]
Register for storing VBID data and to store WSS data.

Sub Address 0x16

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6
Reserved	Reserved	G4-13	G4-12	G4-11	G3-10	G3-9	G3-8

VBID/WSS 2 Register (R) [Sub Address 0x17]
Register for storing VBID data and to store WSS data.

Sub Address 0x17

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0

Device & Revision ID Register (R) [Sub Address 0x18]

Register displays Device ID & Revision of the AK8856.
Device ID of the AK8856 is 56 in decimal. (0x38 at Hexadecimal)
Initial Version of the Revision ID is 0x00.
Revision number is modified only when the control software needs to be modified.

Sub Address 0x18   **Default Value 0x38**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Rev1	REV0	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
0	0	1	1	1	0	0	0

Revision Register Definition

| BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	DEV0 ~ DEV5	Revision bit	R	to show Device ID Device ID is 0x38h.
bit 6 ~ bit 7	REV0 ~ REV1	Device ID	R	to show Revision information REV1 - REV0 Initial version is 0x00

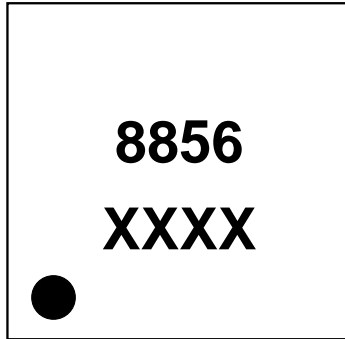# System Connection Example
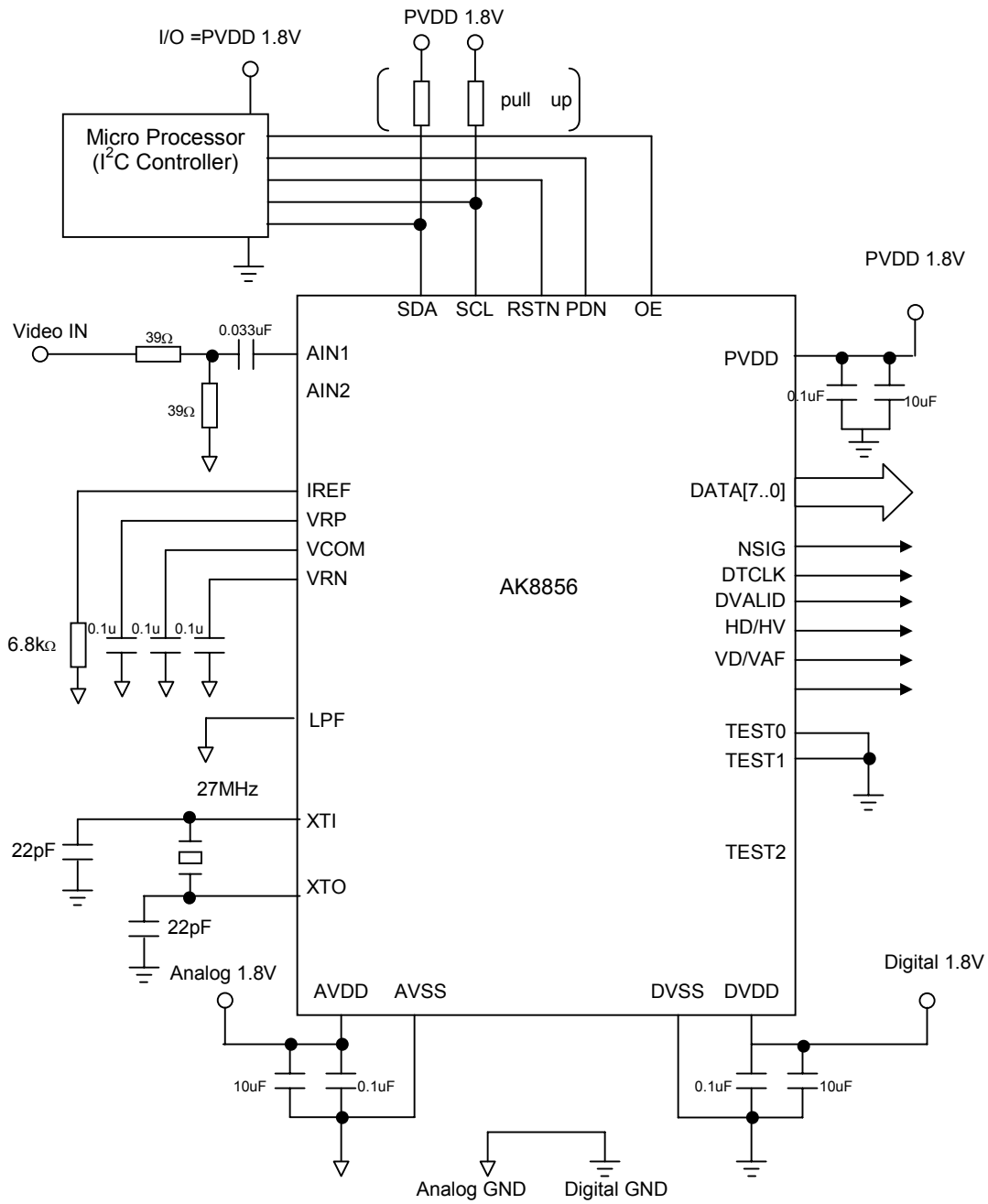
Package Drawing

AK8856VG
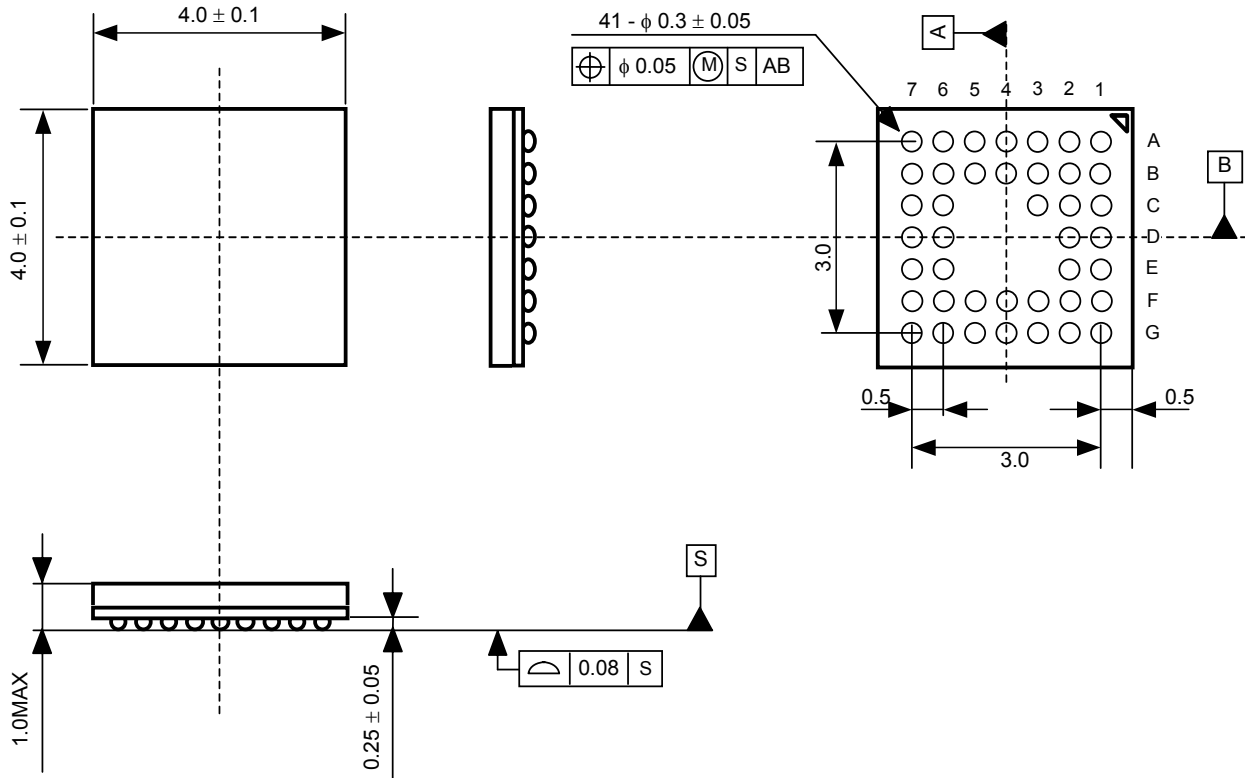
Material : Plating
Package molding compound: Epoxy
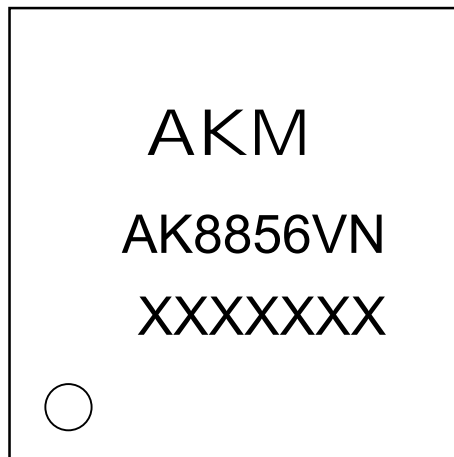Interposer material: BT resin
Solder ball material: SnAgCu

AK8856VN
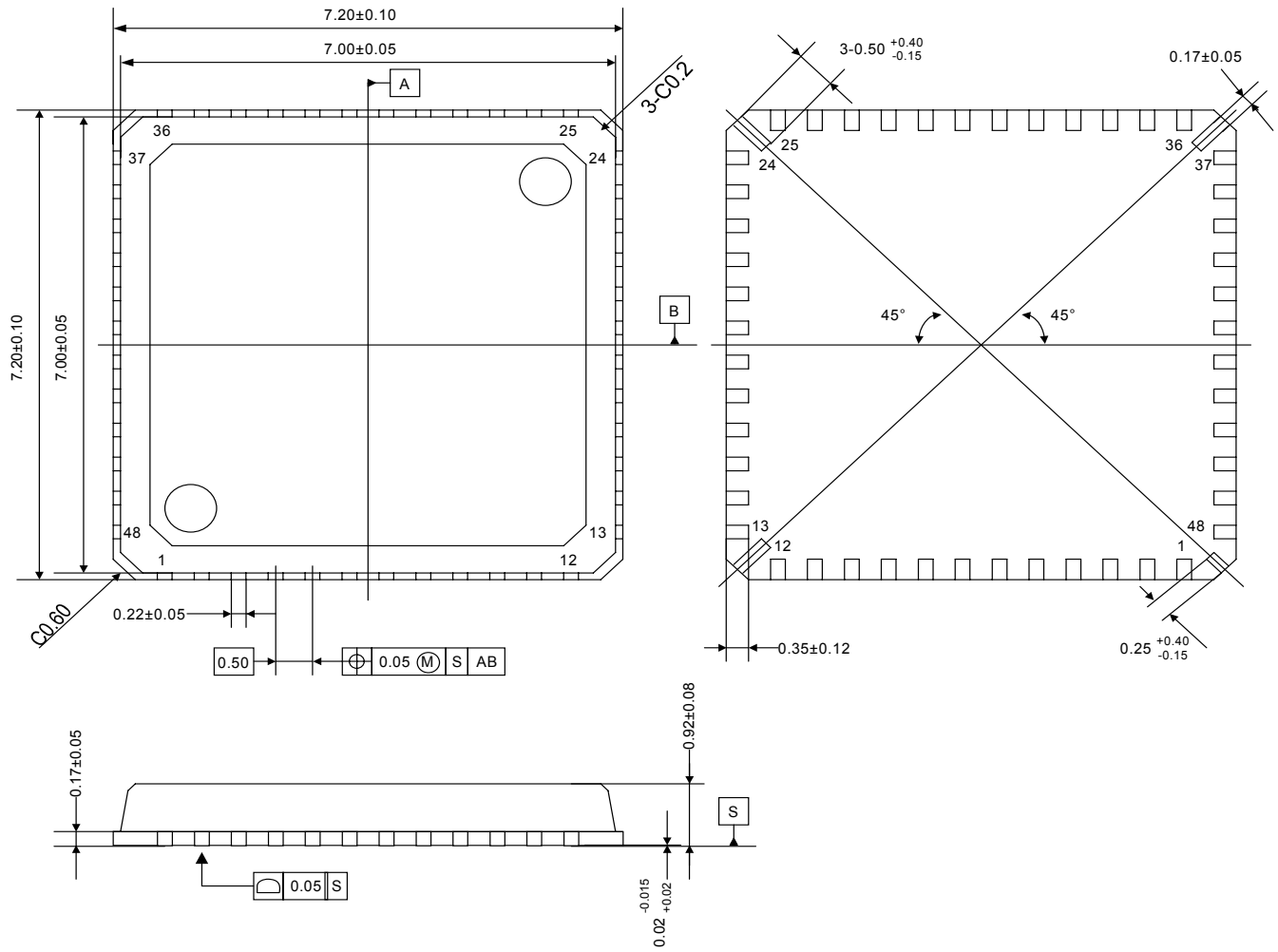
Package Marking Drawing

AK8856VG

```
8856
XXXX
●
```

 a. Package type   : BGA
 b. Number of pins   : 41 pins (including an index pin)
 c. Product number   : 8856
 d. Control Code   : xxxx (4 digit number)

AK8856VN

```
AKM
AK8856VN
XXXXXXX
○
```

 a. Package type   : QFN
 b. Number of pins   : 48 pins
 c. Product number   : AK8856VN
 d. Control Code   : xxxxxxx (7 digit number)

Revised history
Rev.00 -> Rev.01
I/O power supply (PVDD) of AK8856VN is expanding to 3.6V.

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    - (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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