Multi Output Clock Generator with Integrated 2.0GHz VCO
AK8186B

FEATURES

- Low phase noise PLL : RMS Jitter < 300fs
- On-chip VCO tunes from 1.75GHz to 2.25GHz
- External VCO/VCXO to 500MHz optional
- 1 differential or 2 single-ended Inputs
- Reference Switchover/Holdover modes
- Lock Detect
- 3 pairs of 1GHz LVPECL outputs
- 2 pairs of 800MHz LVDS outputs
- 8 250MHz CMOS outputs (two per LVDS)
- Serial control register interface
- 3.3V+/-5% Operating Voltage
- 2.5V-3.3V LVPECL Drive Voltage
- Operating Temperature: -40 to +85°C
- Package: 64-pin Leadless QFN (Pb free)
- Pin compatible with AD9516-3

DESCRIPTION

The AK8186B is a multi-output clock generator with sub-ps jitter performance. The on-chip VCO tunes from 1.75GHz to 2.25GHz.

The distribution section has three pairs of LVPECL buffers (6 outputs) and two pairs of LVDS buffers (4 outputs)/eight CMOS buffers (two per LVDS outputs). The LVPECL outputs operate up to 1GHz, the LVDS outputs operate up to 800MHz and the CMOS outputs operate up to 250MHz.

Each pair of the outputs has a divider. The LVPECL outputs have the division range of 1 to 32. The LVDS and CMOS outputs have the 1 to 1024.

The AK8186B operates at 3.3V and the LVPECL outputs are supplied independently from 2.375V to 3.6V. The operating temperature range is from -40 to +85°C. The part is available in a 9mm 9 mm 64-pin Leadless-QFN (Pb free) package.

ORDERING INFORMATION

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8186B	AK8186B	Tape and Reel	64-pin Leadless QFN	-40 to 85 °C

BLOCK DIAGRAM
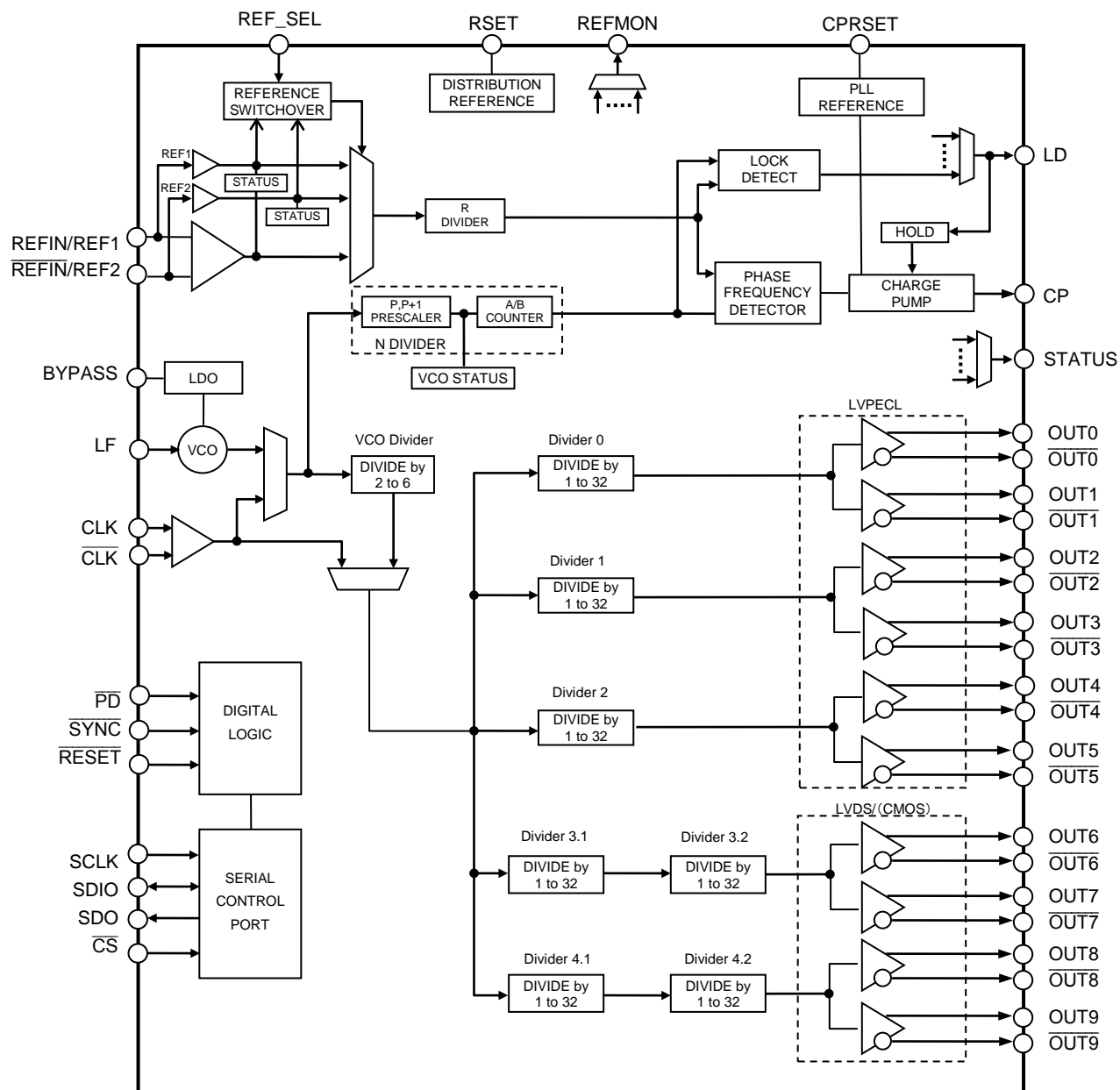
Figure 1. AK8186B Block Diagram

TABLE OF CONTENTS

PIN DESCRIPTION

PIN CONFIGURATION
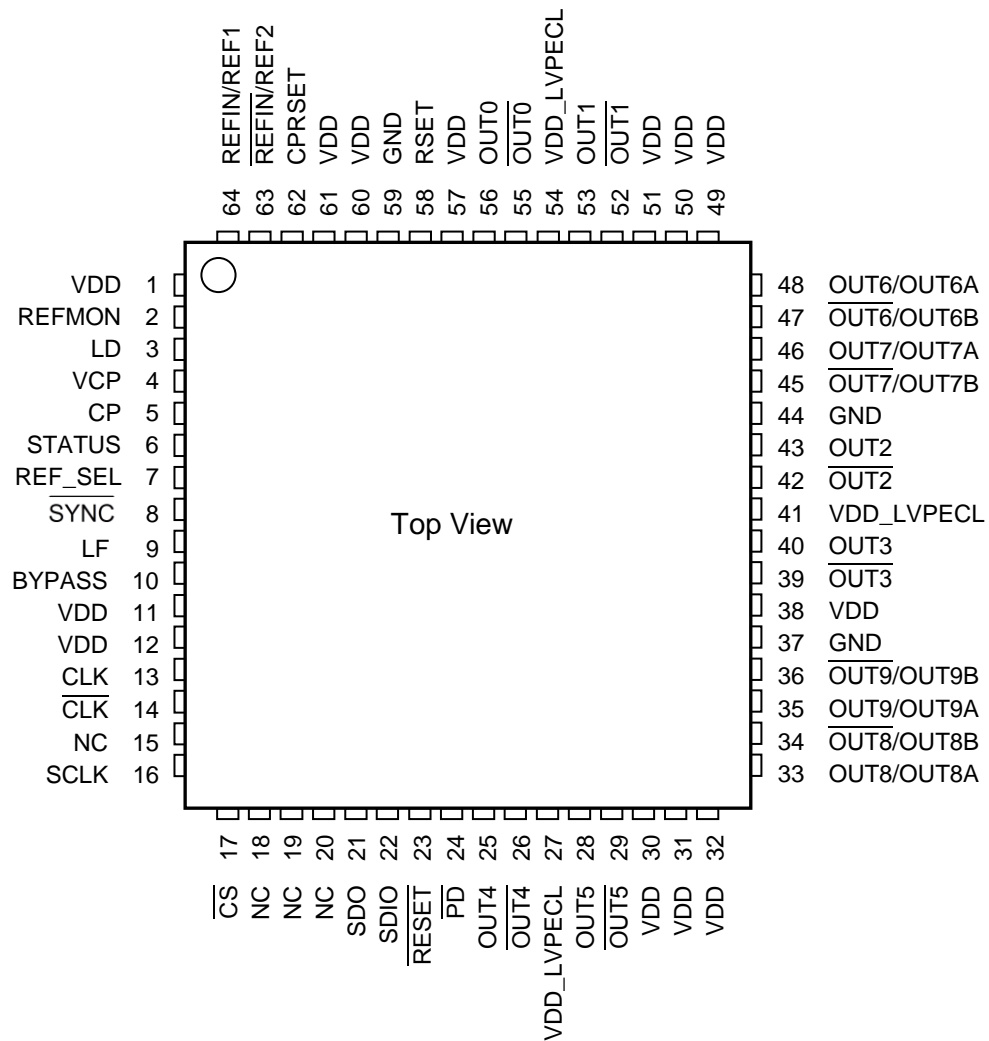
Figure 2.   Pin Configuration

PIN FUNCTION

Pin No.	Pin Name	Pin Type	Description
1	VDD	PWR	3.3V Power Supply.
2	REFMON	OUT	Reference Monitor.
3	LD	OUT	Lock Detect.
4	VCP	---	3.3V Power Supply for Charge Pump (CP)
5	CP	OUT	Charge Pump Output. Connect to external loop filter.
6	STATUS	OUT	Status Indication.
7	REF_SEL	IN	Reference Select. L: REF1 H: REF2. Pulled down with 30kΩ internal resistor.
8,	$\overline{\text{SYNC}}$	IN	Manual Synchronization and Manual Holdover. Active Low. Pulled up with 30 kΩ internal resistor.
9	LF	IN	Loop Filter Input.
10	BYPASS	---	This pin is for bypassing the LDO to ground.
11	VDD	PWR	3.3V Power supply.
12	VDD	PWR	3.3V Power supply.
13	CLK	---	Differential Input for the external VCO/VCXO
14	$\overline{\text{CLK}}$	---	Differential Input for the external VCO/VCXO
15	NC	--	No Connect. Leave open or connected to GND.
16	SCLK	IN	Serial clock for the Serial control port. Pulled down with 30kΩ internal resistor.
17	$\overline{\text{CS}}$	IN	Chip Select for the Serial control port. Active low. Pulled up to VDD with 30 kΩ internal resistor.
18	NC	---	No Connect. Leave open or connected to GND.
19	NC	---	No Connect. Leave open or connected to GND.
20	NC	--	No Connect. Leave open or connected to GND.
21	SDO	OUT	Unidirectional Serial Data Out for Serial Control Port.
22	SDIO	IN/OUT	Bidirectional Serial Data In/Out for Serial Control Port.
23	$\overline{\text{RESET}}$	IN	Reset. Active low. Pulled up with 30 kΩ internal resistor.
24	$\overline{\text{PD}}$	IN	Power Down. Active low. Pulled up with 30 kΩ internal resistor.
25	OUT4	OUT	LVPECL Output 4
26	$\overline{\text{OUT4}}$	OUT	LVPECL Output 4
27	VDD_LVPECL	PWR	2.5V to 3.3V Power Supply for LVPECL Output (OUT4/$\overline{\text{OUT4}}$, OUT5/$\overline{\text{OUT5}}$).
28	OUT5	OUT	LVPECL Output 5
29	$\overline{\text{OUT5}}$	OUT	LVPECL Output 5
30	VDD	PWR	3.3V Power supply
31	VDD	PWR	3.3V Power supply.
32	VDD	PWR	3.3V Power supply for OUT8/$\overline{\text{OUT8}}$ and OUT9/$\overline{\text{OUT9}}$.

(Continued on next page)

Pin No.	Pin Name	Pin Type	Description
33	OUT8/OUT8A	OUT	LVDS/CMOS Output 8
34	$\overline{OUT8}$/OUT8B	OUT	LVDS/CMOS Output 8
35	OUT9/OUT9A	OUT	LVDS/CMOS Output 9
36	$\overline{OUT9}$/OUT9B	OUT	LVDS/CMOS Output 9
37	GND	PWR	Ground. Includes External Pad (EPAD).
38	VDD	PWR	3.3V Power supply.
39	OUT3	OUT	LVPECL Output 3
40	$\overline{OUT3}$	OUT	LVPECL Output 3
41	VDD_LVPECL	PWR	2.5V to 3.3V Power Supply for LVPECL Output (OUT2/$\overline{OUT2}$, OUT3/$\overline{OUT3}$).
42	$\overline{OUT2}$	OUT	LVPECL Output 2
43	OUT2	OUT	LVPECL Output 2
44	GND	PWR	Ground. Includes External Pad (EPAD).
45	$\overline{OUT7}$/OUT7B	OUT	LVDS/CMOS Output 7
46	OUT7/OUT7A	OUT	LVDS/CMOS Output 7
47	$\overline{OUT6}$/OUT6B	OUT	LVDS/CMOS Output 6
48	OUT6 /OUT6A	OUT	LVDS/CMOS Output 6
49	VDD	PWR	3.3V Power supply for OUT6/$\overline{OUT6}$ and OUT7/$\overline{OUT7}$.
50	VDD	PWR	3.3V Power supply.
51	VDD	PWR	3.3V Power supply.
52	$\overline{OUT1}$	OUT	LVPECL Output 1
53	OUT1	OUT	LVPECL Output 1
54	VDD_LVPECL	PWR	2.5V to 3.3V Power Supply for LVPECL Output (OUT0/$\overline{OUT0}$, OUT1/$\overline{OUT1}$).
55	$\overline{OUT0}$	OUT	LVPECL Output 0
56	OUT0	OUT	LVPECL Output 0
57	VDD	PWR	3.3V Power supply.
58	RSET	---	Internal bias current control. Nominal value = 4.12kΩ
59	GND	PWR	Ground.
60	VDD	PWR	3.3V Power supply.
61	VDD	PWR	3.3V Power supply.
62	CPRSET	---	Charge pump current control. Nominal value = 5.1kΩ
63	$\overline{REFIN}$ /REF2	IN	Differential input for the PLL reference. Alternatively single-ended input for REF2.
64	REFIN /REF1	IN	Differential input for the PLL reference. Alternatively single-ended input for REF1.
EPAD	GND	PWR	Ground. The EPAD is connected with other GND pins.

ABSOLUTE MAXIMUM RATING

Table 1   Over operating free-air temperature range unless otherwise noted [1]

Items	Symbol	Min	Max	Unit
Supply voltage(VDD,VDD_LVPECL,VCP)	VDD	-0.3	4.3	V
Input voltage	VIN	GND-0.3	VDD+0.3	V
Input Current	IIN	-10	10	mA
Storage temperature	Tstg	-55	125	°C

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only.   Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device   This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

RECOMMENDED OPERATING CONDITIONS

Table 2

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage [1]	VDD, VCP		3.135	3.3	3.465	V
	VDD_LVPECL		2.375		VDD	V
RSET Pin Resistor	Rr	Connect to GND.	4.08	4.12	4.16	kΩ
CPRSET Pin Resistor	Rc	Connect to GND.	4.3	5.1	6.2	kΩ
BYPASS Pin Capacitor	C_{BP}	Connect to VCOGND.		220		nF

(1) Power of 2.5V or 3.3V requires to be supplied from a single source.   A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

ELECTRICAL CHARACTERISTICS

Power Dissipation

Table 3

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power on default	PD1	*1		0.4	0.52	W
Full Operation	PD2	*2		1.6	2.0	W
Full Operation	PD3	*3		1.4	1.7	W
Power Down	PD4				0.4	mW

(*1)No clock input. Default register values. Not include power dissipation in external resistors.

(*2) REF1/REF2=246.575MHz, Rdiv=16, Ndiv=146, VCO=2.25GHz, VCO div=2, LVPECL=562.5MHz, CMOS(10pF load)=225MHz. Not include power dissipation in external resistors.

(*3) REF1/REF2=246.575MHz, Rdiv=16, Ndiv=146, VCO=2.25GHz, VCO div=2, LVPECL=562.5MHz, LVDS=225MHz. Not include power dissipation in external resistors.

PLL Characteristics

Table 4. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
On Chip VCO					
Frequency Range		1750		2250	MHz
VCO Gain	Fvco=2.25GHz	18	67	146	
	Fvco=1.97GHz	16	52	128	MHz/V
	Fvco=1.75GHz	14	41	114	
Tuning Voltage		1.0		2.5	V
Frequency Pushing	Open Loop	-5		5	MHz/V
Phase Noise@100kHz Offset	Fvco=2.00GHz		-105		dBc/Hz
Phase Noise@1MHz Oddset	Fvco=2.00GHz		-130		dBc/Hz
Reference Inputs (Differential Mode)	REFIN, REFINn				
Input Frequency	Below 1MHz should be dc-coupled	0		250	MHz
Input Duty		40		60	%
Input Sensitivity(AC-Couple)		200			mVpp
Input Slew Rate		0.2			V/ns
Self-Bias Voltage,REFIN		1.35	1.6	1.75	V
Self-Bias Voltage,REFINn		1.3	1.5	1.7	V
Input Resistance,REFIN		3.3	4.8	6.2	kΩ
Input Resistance,REFINn		3.7	5.3	6.9	kΩ
Reference Inputs (Single-Ended Mode)	REF1, REF2				
Input Frequency(AC-Couple)		20		250	MHz
Input Frequency(DC-Couple)		0		250	MHz
Input Sensitivity(AC-Couple)		0.6			Vpp
Input Duty	at VDD/2	40		60	%
Input Slew Rate		0.2			V/ns
Input Logic HIgh		2.0			V
Input Logic Low				0.8	V
Input Logic Current		-100		+100	μA
INPUT Capacitance	REFIN/REF1, REFINn/REF2		5		pF
Phase Frequency Detector					
PFD Input Frequency				100	MHz
Antibacklash Pulse Width			1.4		ns
Charge Pump					
Icp Sink/Source	Programmable				
High Value	CPRSET=5.1kΩ, VCP=3.3V,	4.32	4.8	5.28	mA
Low Value	CP =1.65V, Temp=25℃	0.54	0.60	0.66	mA
Icp Leakage	CP = 0.5 to VCP-0.5V	-1		+1	μA
Sink/Source Matching [1]	CP = 0.5 to VCP-0.5V	-10	2.2	+10	%
Icp vs Vcp [2]	CP = 0.5 to VCP-0.5V	-8	3.6	+8	%
Icp vs Temperature	CP = 0.5*VCP	-5		+5	%

Parameter	Conditions	Min	Typ	Max	Unit
Prescaler (Part of N divider)					
Prescaler Input Frequency					
P = 1 FD	1E1[1]=0			300	MHz
P = 2 FD	1E1[1]=0			500	MHz
P = 3 FD	1E1[1]=0			500	MHz
P = 2 DM (2/3)	1E1[1]=0			500	MHz
P = 4 DM (4/5)	1E1[1]=0			500	MHz
P = 8 DM (8/9)	1E1[1]=0 or 1			2250	MHz
P = 16 DM (16/17)	1E1[1]=0 or 1			2250	MHz
P = 32 DM (32/33)	1E1[1]=0 or 1			2250	MHz
Prescaler Output Frequency	A,B counter input.			300	MHz
Noise Characteristics					
In-Band Phase Noise of the Charge	@500 kHz PFD Frequency		-169		dBc/Hz
Pump/Phase Frequency Detecter	@1MHz PFD Frequency		-166		dBc/Hz
	@10MHz PFD Frequency		-155		dBc/Hz
	@50MHz PFD Frequency		-147		dBc/Hz
PLL Figure of Merit (FOM)	FOM $= $ Phase Noise $- 10\log(f_{PFD})$ $- 20\log(Ndiv) + 20\log(Odiv)$; where Ndiv = N divider ratio, Odiv = VCO divider ratio * Channel divider ratio.		-226		dBc/Hz
PLL Digital Lock Detect Window					
Required to Lock	0x18[4] = 1		3.5		ns
	0x18[4] = 0		7.5		ns
To Unlock After Lock (Hysteresis)	0x18[4] = 1		7		ns
	0x18[4] = 0		15		ns

*1) [(|Isink|-|Isource|)/{(|Isink|+|Isource|)/2}] * 100 [%]

*2) (|I1-I2|)/(|I1+I2|/2)*100 [%]

Clock Input Characteristics

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
CLOCK INPUTS (CLK, $\overline{CLK}$)					
Input Frequency	Below 1MHz should be dc-coupled.	0		500	MHz
Input Sensitivity, Differential			150		mVpp
Input Level, Differential				2	Vpp
Input Common-Mode Voltage, Vcm		1.3	1.57	1.8	V
Input Common-Mode Range, Vcm	With 200mVpp signal applied. dc-coupled	1.3		1.8	V
Input Sensitivity, Single-Ended	CLK ac-coupled, $\overline{CLK}$ ac-bypassed to RF ground.		150		mVpp
Input Resistance	Self-biased	3.2	4.7	6.1	kΩ
Input Capacitance			2		pF

Clock Output Characteristics

Table 6. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVPECL CLOCK OUTPUT		Vterm = 50Ω to				
Output Frequency		VDD_LVPECL-2V			1000	MHz
Output High Voltage(VOH)		0xFn[3:2] = 00 (n=0 to 5) 0xFn[3:2] = 01 (n=0 to 5) 0xFn[3:2] = 10 (n=0 to 5) 0xFn[3:2] = 11 (n=0 to 5)	VDD_LVPECL -1.23	VDD_LVPECL -0.98	VDD_LVPECL -0.73	V
Output High Voltage(VOL)		0xFn[3:2] = 00 (n=0 to 5)	VDD_LVPECL -1.67	VDD_LVPECL -1.38	VDD_LVPECL -1.10	V
		0xFn[3:2] = 01 (n=0 to 5)	VDD_LVPECL -1.86	VDD_LVPECL -1.58	VDD_LVPECL -1.31	
		0xFn[3:2] = 10 (n=0 to 5)	VDD_LVPECL -2.03	VDD_LVPECL -1.77	VDD_LVPECL -1.49	
		0xFn[3:2] = 11 (n=0 to 5)	VDD_LVPECL -2.20	VDD_LVPECL -1.94	VDD_LVPECL -1.65	
Differential Output Voltage		0xFn[3:2] = 00 (n=0 to 5)	250	400	550	
		0xFn[3:2] = 01 (n=0 to 5)	430	600	770	
		0xFn[3:2] = 10 (n=0 to 5)	550	790	980	mV
		0xFn[3:2] = 11 (n=0 to 5)	740	960	1180	
LVDS CLOCK OUTPUT						
Output Frequency Maximum					800	MHz
Differential Output Voltage		0x14n[2:1] = 00 (n=0 to 3)	124	180	227	
		0x14n[2:1] = 01 (n=0 to 3)	247	360	454	mV
		0x14n[2:1] = 10 (n=0 to 3)	186	270	340	
		0x14n[2:1] = 11 (n=0 to 3)	247	360	454	
Delta V_{OD}		0x14n[2:1] = 01 (n=0 to 3)			25	mV
Output Offset Voltage		0x14n[2:1] = 01 (n=0 to 3)	1.125	1.24	1.375	V
Delta V_{OD}		0x14n[2:1] = 01 (n=0 to 3)			25	mV
Short-Circuit Current		0x14n[2:1] = 01 (n=0 to 3) Output shorted to GND.		3.5	24	mA
CMOS CLOCK OUTPUTS						
Output Frequency Maximum		load=10pF			250	MHz
Output High Voltage(VOH)		Ioh=1mA	VDD-0.2			V
Output High Voltage(VOL)		Iol=1mA			0.2	V

Timing Characteristics

Table 7. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
LVPECL Output Rise/Fall time		Termination = 50Ω to VDD-LVPECL-2V 0xFn[3:2] = 10 (n=0 to 5) 20% to 80% / 80% to 20%		 175	 225	 ps

Propagation Delay,
  CLK-to-LVPECL Ouput
  Variation with Temperature
				TBD
				TBD
						ns
						ps/°C

Output Skew [1]		Same Divider Different Dividers		5 13	40 40	ps ps
Output Duty		750MHz ≤ Fout 500M ≤ Fout < 750MHz 250M ≤ Fout < 500MHz [2] Fout < 250MHz [2][3] Fout<1000MHz, VDD_LVPECL=3.3V±5%	30 35 40 45 45	50 50 50 50 50	70 65 60 55 55	% % % % %
LVDS Output Rise/Fall time		Termination = 100Ω @3.5mA 0x14n[2:1] = 01 (n=0 to 3) 20% to 80% / 80% to 20%		 190	 350	 ps

Propagation Delay,
  CLK-to-LVPECL Ouput
  Variation with Temperature
		For All Device Values		TBD
				TBD
						ns
						ps/°C

Output Skew [1]		Same Divider Different Dividers		6 25	62 150	ps ps
Output Duty		[2][3]	45	50	55	%
CMOS Output Rise/Fall time		20% to 80% / 80% to 20% Cload = 10pF		 400	 1000	 ps

Propagation Delay,
  CLK-to-LVPECL Ouput
  Variation with Temperature
		For All Device Values		TBD
				TBD
						ns
						ps/°C

Output Skew [1]		Same Divider Different Dividers		4 28	66 180	ps ps
Output Duty		[2][3]	45	50	55	%

[1] Skew: The Difference between any two similar delay paths while operating at the same voltage and temperature.
[2] Differential input through CLK/$\overline{CLK}$ pins: Clock input is assumed to be 50% duty.
[3] Single-end input through CLK pin: Clock input is assumed to be 50% duty and Fout < 150 MHz.

Clock Output Additive Phase Noise (Distribution Only; VCO Divider Not Used)

Table 8. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL Additive Phase Noise					Does not include PLL and VCO
CLK=500MHz, Output=500MHz, Divider=1					Input slew rate > 1 V/ns
At 1 kHz Offset		-108		dBc/Hz	
At 10 kHz Offset		-130		dBc/Hz	
At 100 kHz Offset		-142		dBc/Hz	
At 1 MHz Offset		-149		dBc/Hz	
At 10 MHz Offset		-150		dBc/Hz	
CLK=500MHz, Output=250MHz, Divider=2					Input slew rate > 1 V/ns
At 1 kHz Offset		-114		dBc/Hz	
At 10 kHz Offset		-133		dBc/Hz	
At 100 kHz Offset		-143		dBc/Hz	
At 1 MHz Offset		-151		dBc/Hz	
At 10 MHz Offset		-152		dBc/Hz	
CLK-TO-LVDS Additive Phase Noise					Does not include PLL and VCO
CLK=500MHz, Output=500MHz, Divider=1					Input slew rate > 1 V/ns
At 1 kHz Offset		-106		dBc/Hz	
At 10 kHz Offset		-126		dBc/Hz	
At 100 kHz Offset		-141		dBc/Hz	
At 1 MHz Offset		-145		dBc/Hz	
At 10 MHz Offset		-147		dBc/Hz	
CLK=500MHz, Output=250MHz, Divider=2					Input slew rate > 1 V/ns
At 1 kHz Offset		-114		dBc/Hz	
At 10 kHz Offset		-133		dBc/Hz	
At 100 kHz Offset		-143		dBc/Hz	
At 1 MHz Offset		-150		dBc/Hz	
At 10 MHz Offset		-152		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-CMOS Additive Phase Noise					Dose not include PLL and VCO
CLK=500MHz, Output=250MHz, Divider=2					Input slew rate > 1 V/ns
At 1 kHz Offset		-113		dBc/Hz	
At 10 kHz Offset		-135		dBc/Hz	
At 100 kHz Offset		-143		dBc/Hz	
At 1 MHz Offset		-149		dBc/Hz	
At 10 MHz Offset		-152		dBc/Hz	
CLK=500MHz, Output=50MHz, Divider=10					Input slew rate > 1 V/ns
At 1 kHz Offset		-129		dBc/Hz	
At 10 kHz Offset		-139		dBc/Hz	
At 100 kHz Offset		-149		dBc/Hz	
At 1 MHz Offset		-156		dBc/Hz	
At 10 MHz Offset		-160		dBc/Hz	

Clock Output Phase Noise (Internal VCO Used)

Table 9. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL Phase Noise					through VCO divider and channel divider
Fvco=2.24256GHz, Fout=280.32MHz					REF=122.88MHz
At 1 kHz Offset		-94		dBc/Hz	
At 10 kHz Offset		-103		dBc/Hz	
At 100 kHz Offset		-105		dBc/Hz	
At 1 MHz Offset		-125		dBc/Hz	
At 10 MHz Offset		-135		dBc/Hz	
At 40 MHz Offset		-136		dBc/Hz	
Fvco=1.96608GHz, Fout=245.76MHz					REF=122.88MHz
At 1 kHz Offset		-89		dBc/Hz	
At 10 kHz Offset		-102		dBc/Hz	
At 100 kHz Offset		-106		dBc/Hz	
At 1 MHz Offset		-127		dBc/Hz	
At 10 MHz Offset		-136		dBc/Hz	
At 40 MHz Offset		-137		dBc/Hz	
Fvco=1.75104GHz, Fout=218.88MHz					REF=122.88MHz
At 1 kHz Offset		-96		dBc/Hz	
At 10 kHz Offset		-105		dBc/Hz	
At 100 kHz Offset		-108		dBc/Hz	
At 1 MHz Offset		-129		dBc/Hz	
At 10 MHz Offset		-137		dBc/Hz	
At 40 MHz Offset		-138		dBc/Hz	

Clock Output Absolute Time Jitter (Clock Generation Using Internal VCO)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL Output Absolute Time Jitter					Internal VCO; through dividers
Fvco=1.96608GHz, Fout=245.76MHz					REF=122.88MHz, PLL BW=140kHz
		156		fs rms	200kHz to 10MHz
		284		fs rms	12kHz to 20MHz
Fvco=1.96608GHz, Fout=122.88MHz					REF=122.88MHz, PLL BW=140kHz
		169		fs rms	200kHz to 10MHz
		293		fs rms	12kHz to 20MHz
Fvco=1.96608GHz, Fout=61.44MHz					REF=122.88MHz, PLL BW=140kHz
		193		fs rms	200kHz to 10MHz
		325		fs rms	12kHz to 20MHz

Clock Output Absolute Time Jitter (Clock Generation Using External VCXO)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL Output Absolute Time Jitter					External VCXO: Reference = 15.36MHz, R=1
LVPECL=245.76MHz, PLLBW=125Hz				fs rms	Integration BW = 200kHz to 5MHz
		TBD		fs rms	Integration BW = 200kHz to 10MHz
				fs rms	Integration BW = 12kHz to 20MHz
LVPECL=122.88MHz, PLLBW=125Hz				fs rms	Integration BW = 200kHz to 5MHz
		TBD		fs rms	Integration BW = 200kHz to 10MHz
				fs rms	Integration BW = 12kHz to 20MHz
LVPECL=61.44MHz, PLLBW=125Hz				fs rms	Integration BW = 200kHz to 5MHz
		TBD		fs rms	Integration BW = 200kHz to 10MHz
				fs rms	Integration BW = 12kHz to 20MHz

Clock Output Additive Time Jitter (VCO Divider Not Used)

Table 12

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL Output Additive Time Jitter					Distribution Section Only
CLK=500MHz,Output=500MHz,Divider=1		39		fs rms	12kHz to 20MHz
CLK=500MHz,Output=250MHz,Divider=2		92		fs rms	12kHz to 20MHz
CLK=500MHz,Output=100MHz,Divider=5		137		fs rms	12kHz to 20MHz
LVDS Output Additive Time Jitter					Distribution Section Only
CLK=500MHz,Output=500MHz,Divider=1		76		fs rms	12kHz to 20MHz
CLK=500MHz,Output=250MHz,Divider=2		92		fs rms	12kHz to 20MHz
CLK=500MHz,Output=100MHz,Divider=5		237		fs rms	12kHz to 20MHz
CMOS Output Additive Time Jitter					Distribution Section Only
CLK=500MHz,Output=100MHz,Divider=5		131		fs rms	12kHz to 20MHz

Clock Output Additive Time Jitter (VCO Divider Used)

Table 13

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL Output Additive Time Jitter					Distribution Section Only
CLK=500MHz,Output=100MHz,Divider=5		129		fs rms	12kHz to 20MHz
LVDS Output Additive Time Jitter					Distribution Section Only
CLK=500MHz,Output=100MHz,Divider=5		219		fs rms	12kHz to 20MHz
CMOS Output Additive Time Jitter					Distribution Section Only
CLK=500MHz,Output=100MHz,Divider=5		120		fs rms	12kHz to 20MHz

Serial Control Port

Table 14. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
$\overline{CS}$ (INPUT)		internal 30kΩ pull-up resistor				
Input High Level Voltage	V_{IH}		2.0			V
Input Low Level Voltage	V_{IL}				0.8	V
Input High Level Current	I_{IH}		-3		3	μA
Input Low Level Current	I_{IL}		45	110	220	μA
Input Capacitance	C_{IN}			5		pF
SCLK (INPUT)		internal 30kΩ pull-down resistor				
Input High Level Voltage	V_{IH}		2.0			V
Input Low Level Voltage	V_{IL}				0.8	V
Input High Level Current	I_{IH}		45	110	220	μA
Input Low Level Current	I_{IL}		-3		3	μA
Input Capacitance	C_{IN}			5		pF
SDIO (INPUT)						
Input High Level Voltage	V_{IH}		2.0			V
Input Low Level Voltage	V_{IL}				0.8	V
Input High Level Current	I_{IH}		-3		3	μA
Input Low Level Current	I_{IL}		-3		3	μA
Input Capacitance	C_{IN}			11		pF
SDIO, SDO (OUTPUT)						
High Level Output Voltage	V_{OHS}	SDO,SDIO(OUT), I_{OH} =-1mA	2.7			V
Low level Output Voltage	V_{OLS}	SDO,SDIO(OUT) , I_{OL} =1mA			0.4	V
TIMING		Load=100pF				
Clock Rate(SCLK)	1/ t_{SCLK}				20	MHz
Pulse Width High	t_{HI}		20			ns
Pulse Width Low	t_{LO}		20			ns
SDIO to SCLK Setup	t_{DS}		8			ns
SCLK to SDIO Hold	t_{DH}		8			ns
SCLK to Valid SDIO and SDO	t_{OV}				15	ns
$\overline{CS}$ to SCLK Setup and Hold	t_{S}		12			ns
SCLK to $\overline{CS}$ Holdup and Hold	t_{H}		8			ns
$\overline{CS}$ Minimum Pulse Width High	t_{PWH}		5			ns

$\overline{PD}$, $\overline{SYNC}$ and $\overline{RESET}$

Table 15. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
INPUT		internal 30kΩ pull-up resistor				
Input High Level Voltage	V_{IH}		2.0			V
Input Low Level Voltage	V_{IL}				0.8	V
Input High Level Current	I_{IH}		-3		3	μA
Input Low Level Current	I_{IL}		45	110	220	μA
Input Capacitance	C_{IN}			5		pF
$\overline{RESET}$ TIMING						
Pulse Width Low	t_{LO}		50			ns
$\overline{SYNC}$ TIMING						
Pulse Width Low	t_{LO}	Refer to Input signal cycle	1.5			Cycle

LD, STATUS and REFMON

Table 16. All specifications at VDD=3.3V±5%, VDD_LVPECL= 2.375V to VDD,   Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
OUTPUT						
High Level Output Voltage	V_{OH}	I_{OH} =-1mA	2.7			V
Low level Output Voltage	V_{OL}	I_{OL} =1mA			0.4	V
LD Output Current	ILD	0x1A[5:0]=04h 0V < LD Output voltage < 2V,	88	110	132	μA
MAXIMUM TOGGLE RATE		Load=10pF	50	100		MHz
ANALOG LOCK DETECT						
Capacitance				9		pF
FREQUENCY STATUS MONITOR						
REF1, REF2, VCO		0x1A[6]=0 (Default)	1.02	2.00	4.00	MHz
REF1, REF2		0x1A[6]=1	8	16	32	MHz
LD COMPARATOR						
Trip Point L to H			1.58	1.73	1.88	V
Trip Point H to L			1.32	1.47	1.62	V
Hysteresis			170	260	350	mV

TIMING DIAGRAMS
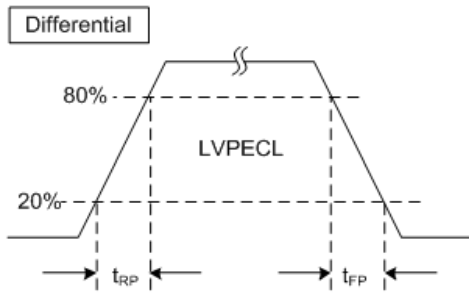
Figure 3. LVPECL Timing, Differential
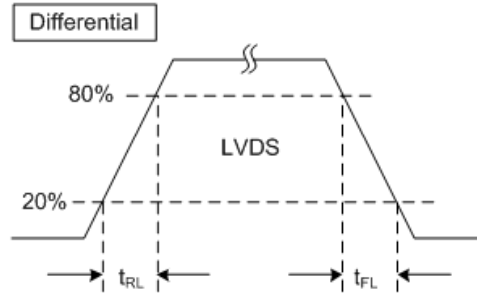
Figure 4. LVDS Timing, Differential
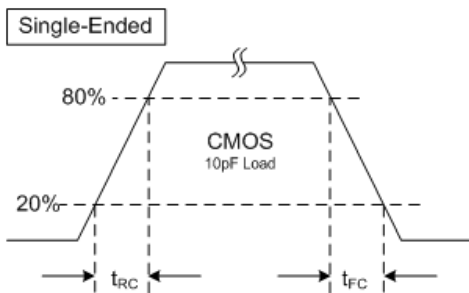
Figure 5. CMOS Timing, Single-Ended, 10pF Load
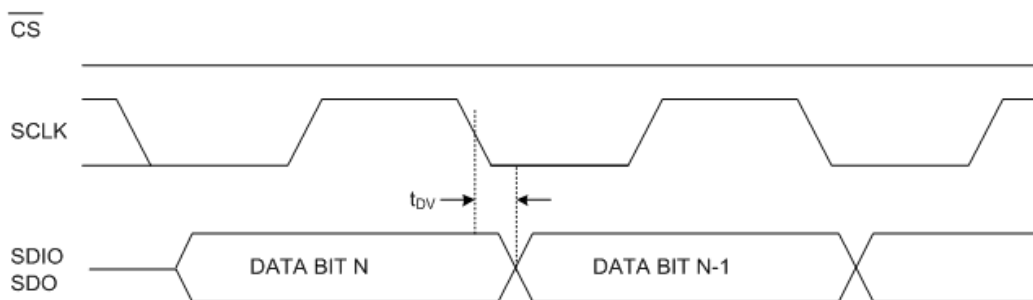
Figure 6. Serial Control Port   - READ -
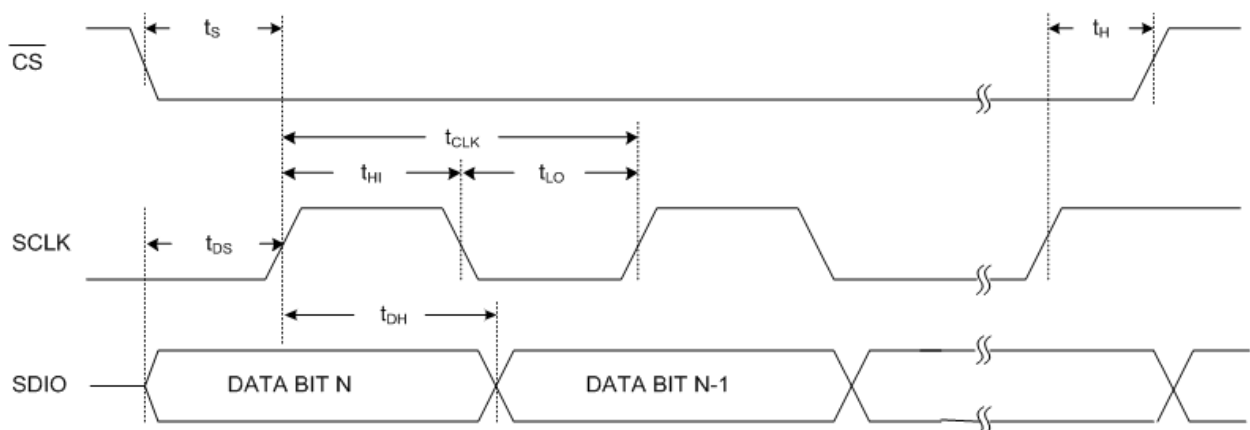
Figure 7. Serial Control Port   - WRITE -

THEORY OF OPERATION

OPERATIONAL CONFIGURATIONS

The AK8186B can be configured in two ways below.
- ➢ Internal VCO and Clock Distribution
- ➢ External VCO and Clock Distribution

Each functional block must be set by the registers through a serial control port.

Internal VCO and Clock Distribution

When using the internal VCO and PLL, the things below are to be cared.
- Prescaler divide ratio : 8/9, 16/17 and 32/33 can be used to meet the maximum input frequency of A,B counter, 300MHz.
- VCO calibration must be executed after the internal VCO is enabled.

Table 17 Settings for Internal VCO

Register	Function
0x10[1:0] = 00b	PLL normal operation (PLL on).
0x10 to 0x1E	PLL settings. Select and enable a reference input; set R, N(P,A,B) PFD polarity, and Icp according to the intended loop configuration.
0x18[0] = 0	Reset VCO calibration.
0x232[0] = 1	Register Update.
0x18[0] = 1	Initiate VCO calibration.
0x232[0] = 1	Register Update.
0x1E0[2:0]	Set VCO divider ratio.
0x1E1[0] = 0	Use the VCO divider as source for distribution section.
0x1E1[1] = 1	Select VCO as the source.
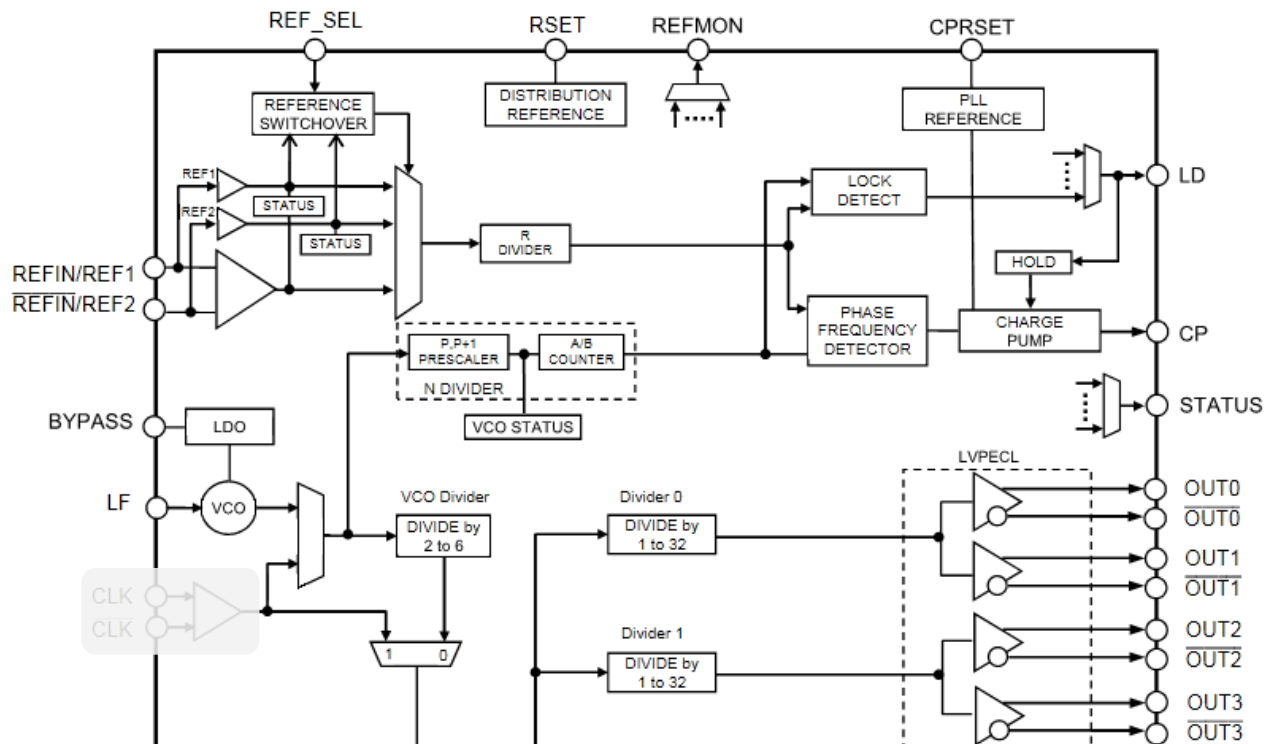
Figure 8 Internal VCO and Clock Distribution

External VCO and Clock Distribution

When using the external VCO and PLL, the things below are to be cared.
- Prescaler divide ratio : 1, 2/3, 4/5, 8/9, 16/17 and 32/33 can be used to meet the maximum input frequency of A,B counter, 300MHz.
- Maximum frequency of the External VCXO is 500MHz.

Table 18 Settings for External VCO

Register	Function
0x10[1:0] = 00b	PLL normal operation (PLL on).
0x10[7] = 0 or 1	PFD polarity　0: positive　1:negative
0x10 to 0x1E	PLL settings. Select and enable a reference input; set R, N(P,A,B) PFD polarity, and Icp according to the intended loop configuration.
0x1E0[2:0]	Set VCO divider ratio.
0x1E1[0] = 0 or 1	Select the source for distribution section. 0: VCO divider　1: CLK input
0x1E1[1] = 0	Select the CLK input as the source.
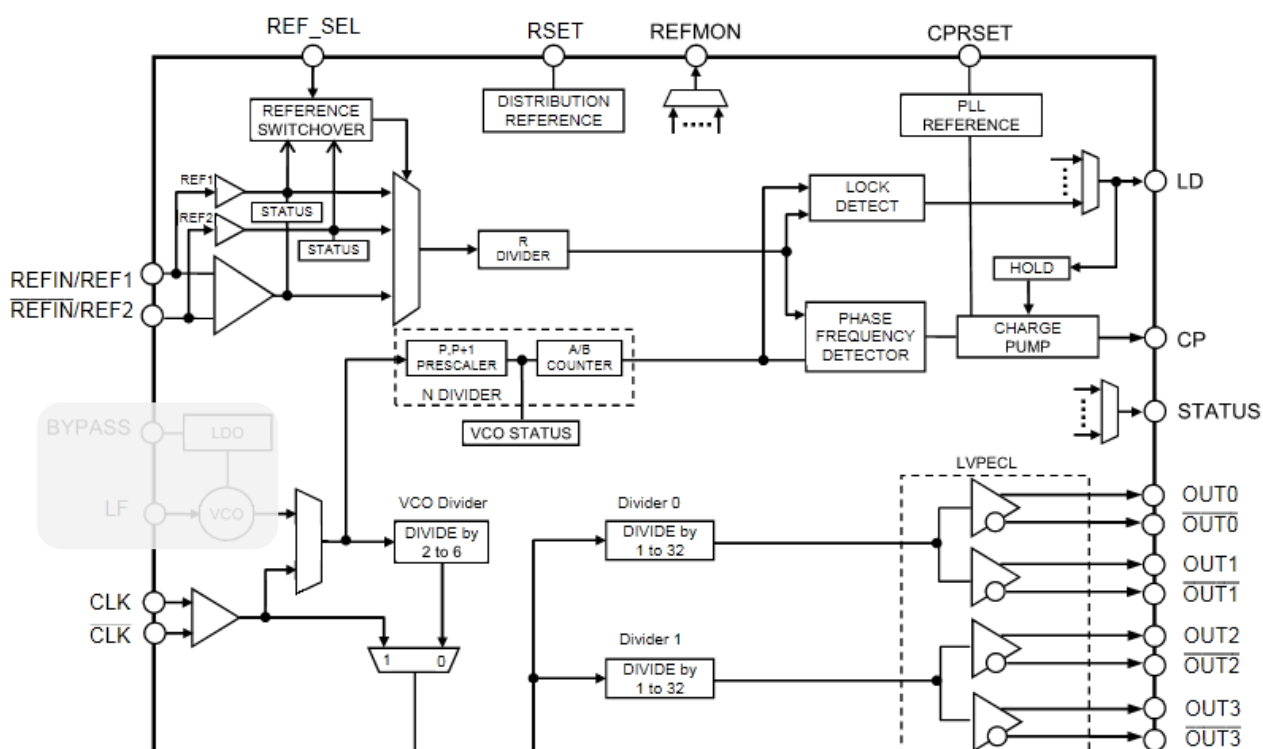
Figure 9 External VCO and Clock Distribution

PLL

The AK8186B integrates a PLL with a VCO which can be configured to meet user's application. The following functions are set through a serial control port. The setting registers are mapped into 0x10 to 0x1F in a register.

- PLL Power down
- Charge pump current
- R counter for Reference input
- A counter, B counter and Prescaler in loopback path
- Pin function of STATUS,LD and REFMON pins
- VCO calibration
- Lock Detect
- Frequency monitor of REF1, REF2 and VCO
- Switchover
- Holdover
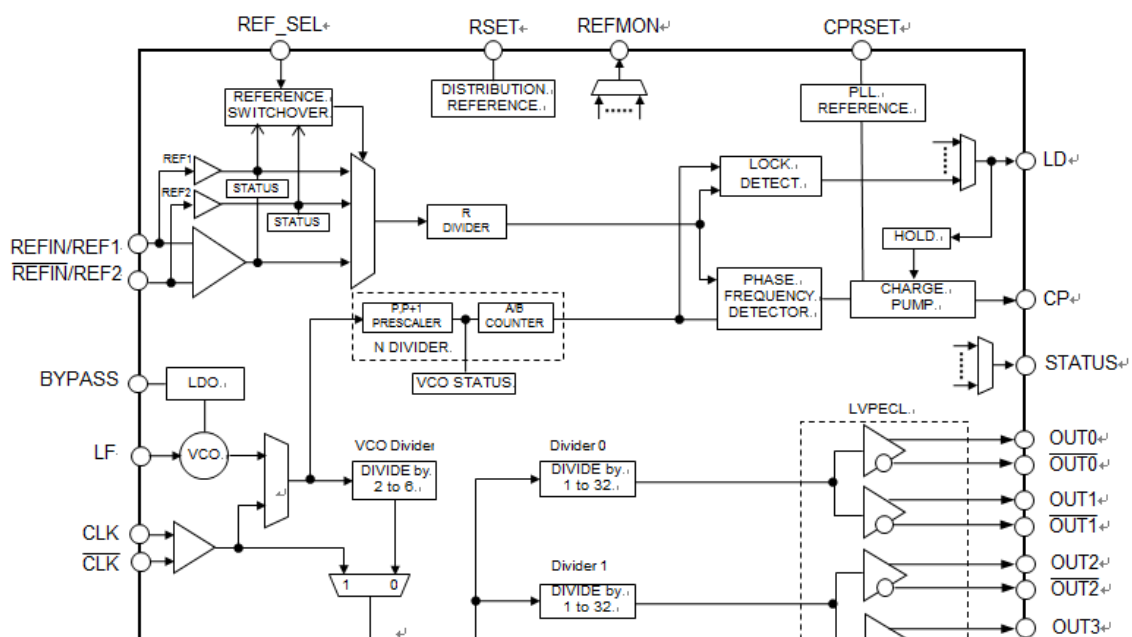
Figure 10. PLL

REFERENCE INPUT

The reference input section of the AK8186B allows a differential input or two single-ended inputs. Both types of inputs are self-biased. It allows easy ac-coupled input signals. The desired reference input is selected by 0x1C[2:0].

Single-ended input

A dc-coupled CMOS level signal or an ac-coupled sinewave or square wave signal can be input.

Differential input

An ac-coupled signal or a dc-coupled signal can be input. If a single-ended signal is applied to the differential REFIN, the REFINn should be decoupled through a capacitor to a ground.

Note

All reference inputs are powered down by default.
When PLL is powered down, all the reference inputs are powered down.
When the differential mode is selected, the single-ended inputs are powered down and vice versa.

The maximum input frequency of both type of inputs is 250MHz.

REFERENCE SWITCHOVER

When dual single-ended CMOS inputs are imposed to REF1 and REF2, the AK8186B could support automatic and manual PLL reference clock switching between REF1 and REF2. The automatic switchover is enabled by setting 0x1C[4].

0x1C[4] =   0 : manual switchover
             1 : automatic switchover

Note;
The single-ended inputs should be dc-coupled CMOS levels and not go to high impedance. If these go to high impedance, input buffers may cause chattering due to noise. A false detection might occur.

Manual Switchover

A PLL reference input can be selected by a register or a pin.
0x1C[5] assigns the register 0x1C[6] or the REF_SEL pin to select a PLL reference input.

Automatic Switchover

Automatic switchover has two modes of operation. Both of them switch from REF1 to REF2 when REF1 is lost. The difference of the two modes is whether the AK8186B would stay on REF2 or not when REF1 returns. 0x1C[3] selects one of the two modes.

0x1D[3] =   0 : Switch to REF1.
             1 : Stay on REF2. It can be switched to REF1 manually.

Condition to switch from REF1 to REF2

If the reference switchover circuit detects three consecutive rising edges of REF2 without any REF1 rising edges, the REF1 is considered to be lost. On the 2nd subsequent rising edge of REF2, the reference clock input to PLL is switched from REF1 to REF2.

Condition to switch back to REF1 when 0x1D[3]=0

If the reference switchover circuit detects four consecutive rising edges of REF1 without three consecutive REF2 rising edges between REF1 edges, the REF1 is considered to be returned. On the 2nd subsequent rising edge of REF2, the reference clock input to PLL is switched from REF2 to REF1.

R DIVIDER (REFERENCE DIVIDER)

The reference input goes into the R divider (a 14-bit counter). It can be set to any value from 0 to 16383 by 0x11 and 0x12. When 0 is set, the input is divided by 1.

Maximum output frequency

The output of the R divider goes to one of the PFD inputs which is compared to the output of the N divider. The frequency applied to the PFD must not exceed 100MHz.

Reset

The R is divider can be reset under the following conditions.
 1) Power on reset
 2) When $\overline{RESET}$ is asserted low.
 3) When 0x16[6] is set to 1 (reset of the R divider)
 4) When 0x16[5] is set to 1 (shared reset bit of the R, A and B counter)
 5) When $\overline{SYNC}$ is released from L to H.

PHASE FREQUENCY DETECTOR (PFD)

The PFD has two inputs of R divider and N divider. It outputs an up/down signal for the charge pump, which is proportional to the phase and frequency difference between the inputs. Both input frequencies must not exceed the maximum frequency of 100MHz.

CHARGE PUMP (CP)

The charge pump pumps up/down controlled by the output of the PFD. The output current of the CP goes out through the CP pin and integrated and filtered by the external loop filter, then is finally turned into a voltage. The voltage goes into the VCO via the LF pin to tune the VCO frequency.

The CP has four modes of operation and eight current values. Each of them can be set by the registers below.

Table 19 Register for Charge Pump Operation Mode

Item	Register	Description
Operation Mode	0x10[3:2]	Normal, High Impedance, Pump up, Pump down
CP Current	0x10[6:4]	0.6 to 4.8 mA with 0.6mA step (CPRSET=5.1kΩ)

On-Chip VCO

The AK8186B integrates a VCO working in the range of 1.75GHz to 2.25GHz. The VCO requires a calibration to achieve optimal operation around the REFIN frequency. After power-up or reset. a initial calibration is required along with the procedure shown below. The calibration can be executed at anytime after power-up or reset from the step marked (*). SYNC function is executed during the VCO calibration. Distribution outputs remain static in this period. Maximum time of the VCO calibration is 4400 cycles of a VCO calibration clock supplied by a VCO calibration divider. The VCO calibration divider divides the R divider output (= the PFD input clock) with the divider value of 2,4,8 or 16 set to 0x18[2:1]. When the calibration is finished, a logic true (1b) is returned to a readback bit 0x1F[6].
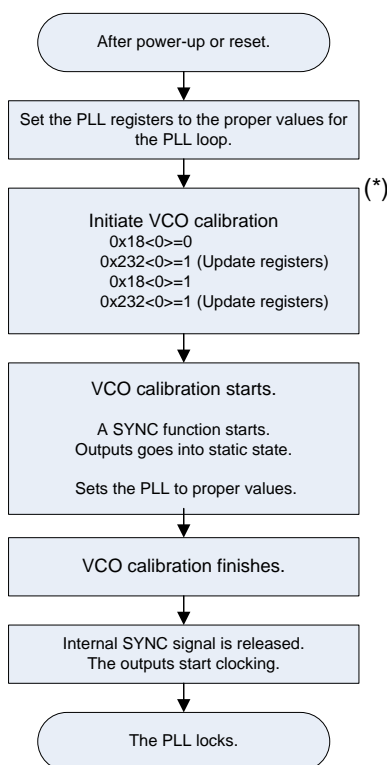
Figure 11. Procedure of VCO calibration

External VCO/VCXO

The AK8186B supports an external VCO/VCXO. The CLK/CLK input can be used as a differential feedback for an external VCO/VCXO. The input frequency is up to 500MHz.

PLL EXTERNAL LOOP FILTER

The loop filter supplies a voltage to the VCO via the LF pin to move the VCO frequency up or down. When using the internal VCO, the external loop filter should be referenced to the BYPASS pin for optimal noise and spurious performance. An example is shown in Fig.13. The values of loop filter must be calculated for each PLL. It depends on the VCO frequency, the Kvco, the PFD frequency, the CP current, the desired loop bandwidth and the desired phase margin.
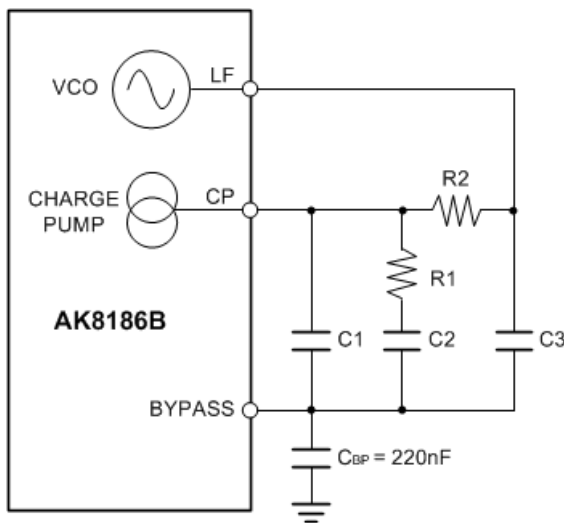
Figure 12 Example of External Loop Filter for the Internal VCO   **Figure 13 Example of External Loop Filter for an External VCO**
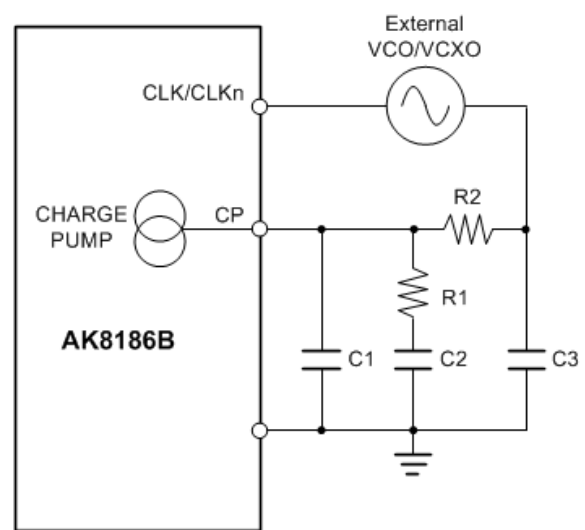
FEEDBACK DIVIDER (N DIVIDER)

The N divider consists of a prescaler (P), A and B counters.
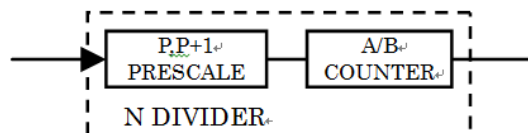
Figure 14. N divider

PRESCALER

The prescaler is a dual modulus counter which has two modes of operation. Division value of A counter defines the mode as below.

1) When A = 0:   a fixed divide (FD) mode where the prescaler divides by P.
2) When A ≠ 0:   dual modulus (DM) mode where the prescaler divides by P and (P+1).

Since the maximum output frequency of the prescaler is 300MHz, the prescaler input frequency is limited by the modes as shown in Table 4. The prescaler must divide its input frequency by appropriate divide ratio defined by Register 0x016[2:0]. In case of using the internal VCO, its output (1.75GHz min) must be divided by P = 8, 16 and 32. (See the "PLL Configuration in Register Map Function Descriptions")

FD mode (A=0)

The Prescaler divider value is P. It is divided by B counter.

$N = P \times B$

Where   P = 1, 2, 4, 8, 16 or 32 for an external VCO/VCXO.

              P = 8, 16 or 32 for an internal VCO.

B : 3 to 8191   when B = 1, B counter is bypassed. Not allowed for B = 0 and 2.

DM mode (A≠0)

The prescaler divider value is P for (B-A) times and P+1 for A times.

$N = P \times B + A$

Where   P = 1, 2/3, 4/5, 8/9, 16/17 or 32/33 for an external VCO/VCXO.

              P = 8/9, 16/17 or 32/33 for an internal VCO.

B : 3 to 8191   when B = 1, B counter is bypassed. Not allowed for B = 0 and 2.

The output frequency of the N divider f_{VCO}/N is equated to the output of the R divider f_{REF}/R at the PFD. Then the VCO frequency is

1) When A = 0: $f_{VCO} = f_{REF} \times N/R$ where $N = P \times B$
2) When A ≠ 0: $f_{VCO} = f_{REF} \times N/R$ where $N = P \times B + A$

A and B COUNTERS

The division value of the A and B counters is defined by the registers below.

        A counter :   0x13[5:0]

        B counter :   0x14[7:0] and 0x15[4:0]

Note;

- Both division values should be set A ≤ B.
- P = 1, 2, 4, 8, 16 or 32 when A=0.
- B = 0 and B = 2 are not allowed.
- Maximum input frequency of A/B counters is 300MHz.

Reset Counters

$\overline{SYNC}$ pin resets all of P, A and B counters simultaneously. This is allowed by the register 0x19[7:6]. A/B counters can be reset by the register 0x16[5][4].

LOCK DETECT

The AK8186B has three kinds of lock detect function. Each Lock Detect function is able to report to LD, STATUS and REFMON pins.

.Table 20 Registers for Lock Detect

Mode	Enable/Disable Register	OUTPUT pin		
		LD 0x1A[5:0]	STATUS 0x17[7:2]	REFMON 0x1B<4:0>
Digital Lock Detect (DLD)	0x18[3]	√	√	√
Current Source DLD (CLD)	---	√		
Analog Lock Detect (ALD)	---	√		

Digital Lock Detect (DLD)

The Digital Lock Detect function detects a lock when the phase difference of the rising edges at the PFD inputs is less than the Lock Detect Window (3.5ns typical). The lock is indicated when the number of consecutive "lock detection" reaches the threshold of the Lock Detect Counter defined by 0x18<6:5>.
The "unlock" is indicated when the DLD function detects the larger phase difference at the PFD inputs than the Lock Detect Window. The unlock threshold is just one value.
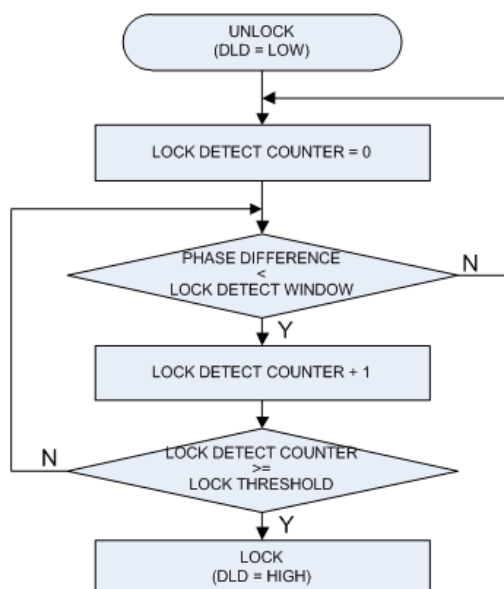
Figure 15. Digital Lock Detect

Current Source Digital Lock Detect (CLD)

The lock indication by the DLD is normally not stable until the PLL gets in lock completely. In some application, it might be required to get a lock detect after the PLL gets solidly locked. The Current Source DLD function (CLD) could be useful for that requirement.

The CLD provides a current of 110uA to LD pin when the DLD detects a lock (DLD = H). While the PLL continues to be in lock state, the voltage of LD is going up with the current. But if the PLL is back to unlock state, the charge on a capacitor externally connected to LD is discharged instantly.

The voltage of LD can be sensed by an internal or external comparator. When the internal LD pin comparator is used (0x1D[3]=1b), its output can be read at STATUS pin (0x17[7:2]) or REFMON pin

(0x1B[4:0]). Selecting a properly value of capacitor allows a lock detect indication to be delayed. The LD pin comparator trip point is shown in Table 16.
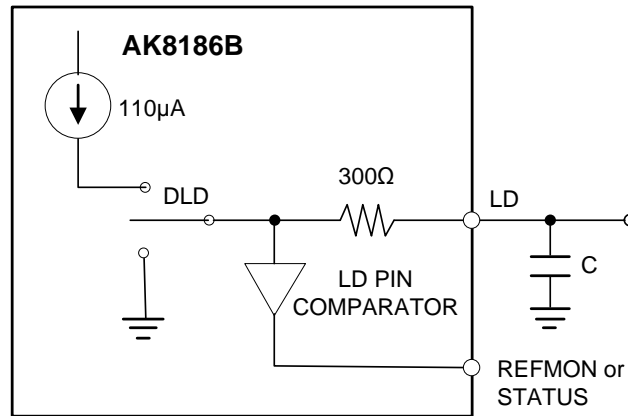
Figure 16. Current Source Lock Detect

Analog Lock Detect (ALD)

When 0x1A[5:0] is set to the value shown below, the Analog Lock Detect is indicated at the LD pin. The ALD function requires a external R-C filter to indicate lock/unlock state.

    0x1A[5:0] = 01h   : P-channel open drain ALD (Active Low)
    0x1A[5:0] = 02h   : N-channel open drain ALD (Active High)
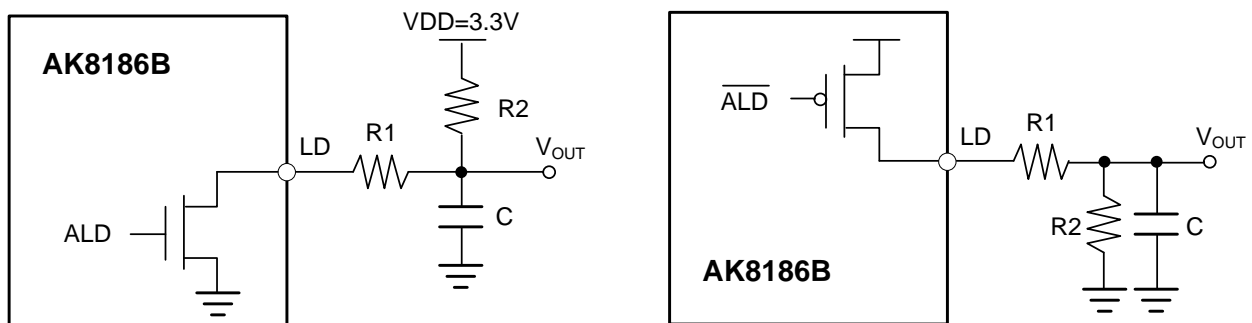
Figure 17. Analog Lock Detect (N/P-channel open drain)

N-channel open drain

The ALD signal is derived from the up/down control outputs of the PFD.
- When the PLL is in lock, the ALD signal is mainly low with minimum high-going pulse. This leads the voltage of LD to getting up to VDD.
- When the PLL in in unlock, the ALD signal has a wider high-going pulse. This leads the voltage of LD to getting down to ground.

P-channel open drain

The ALD signal is the inverting of the ALD.
- When the PLL is in lock, the ALD signal is mainly high with minimum low-going pulse. This leads the voltage of LD to getting down to ground.
- When the PLL in in unlock, the ALD signal has a wider high-going pulse. This leads the voltage of LD getting up to VDD.

HOLDOVER

Some application requires holding the output frequency to be constant even though the REF input is lost out. A holdover function is for such a requirement. In the AK8186B, the holdover function puts the charge pump into high-impedance state so that the VCO keeps its frequency constant. However, any leakage could occur at the charge pump output, which leads the unwanted VCO frequency shift. Adequate capacitive value in the loop filter should be selected to avoid shifting the VCO frequency out of the required limit.

The AK8186B has two modes of holdover function, manual or automatic mode. Manual holdover is activated by the $\overline{\text{SYNC}}$ pin. Automatic holdover is activated by the voltage of LD pin. Both holdover modes are enabled with 0x1D[2:0].

Table 21 Setting Holdover

Mode	Holdover Enable 0x1D[2]	Mannual/Automatic 0x1D[1]	Holdover Enable 0x1D[0]
Manual Holdover	1	1	1
Automatic Holdover	1	0	1

Manual Holdover Mode

A manual holdover puts the charge pump into a high impedance state immediately when the $\overline{\text{SYNC}}$ pin is asserted low. This is trigged by the falling edge of the $\overline{\text{SYNC}}$.

Getting into the holdover

Condition   : the falling edge of the $\overline{\text{SYNC}}$
Operation Timing   : immediately
Operation   : puts the charge pump into a high impedance state

Leaving the holdover

Condition   : the $\overline{\text{SYNC}}$ = High
Operation Timing   : synchronous with the first PFD rising edge after the $\overline{\text{SYNC}}$ goes high.
Operation   : puts the charge pump into a normal state, resets the B-counter.
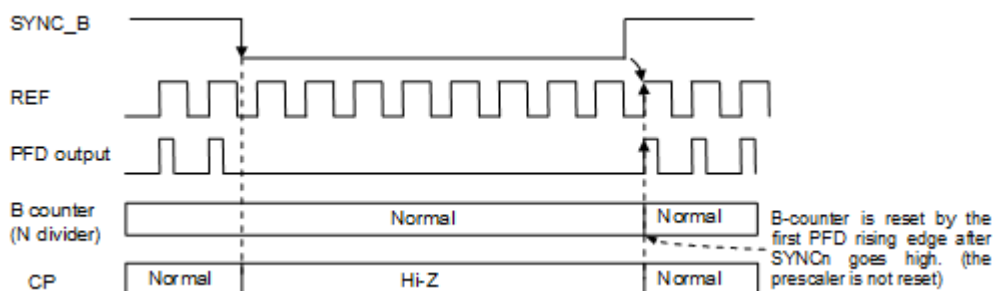
Figure 18. Manual Holdover

Note: Set the channel divider to ignore the $\overline{\text{SYNC}}$ pin at least after an initial SYNC event. Otherwise, every time $\overline{\text{SYNC}}$ is asserted low to invoke the manual holdover, the distribution outputs become DC output state.

Table 22 Setting the channel divider to ignore the SYNC

Divider	Nosync register bit	Value to ignore $\overline{SYNC}$ pin
0	0x191[6]	1
1	0x194[6]	1
2	0x197[6]	1
3	0x19C[3]	1
4	0x1A1[3]	1

Automatic Holdover Mode

An automatic holdover puts the charge pump into a high impedance state immediately when the unlock state is detected. A flow chart of the automatic holdover function is shown in Figure 16.

Getting into the holdover

Condition   : LD pin = H when DLD = low (false)
Operation Timing : immediately
Operation   : puts the charge pump into a high impedance state

Leaving the holdover

Condition   : DLD = High (true)
Operation Timing : synchronous with a first PFD rising edge after DLD goes high.
Operation   : puts the charge pump into a normal state, resets the B-counter.

LD pin is able to report the status of DLD, ALD and CLD. The CLD is recommended to use for the automatic holdover to avoid re-triggering a holdover due to chattering on the LD. The register 0x1A[5:0] defines the function of the LD.

The auto holdover function uses the LD pin comparator to sense the status of the LD pin. When the register 0x1D[3]=0, the LD comparator is disabled and the LD pin is treated as always high by the automatic holdover function. When 0x1D[3]=1, the LD comparator is enabled and can be used for DLD, ALD and CLD.

The registers shown in Table are required to be set to use the automatic holdover function.

Table 23 Setting Automatic Holdover Function

| Register	Name	Description
0x18<6:5>	Lock Detect Counter	Select PFD cycles to determine lock.
0x18[3]	Disable Digital Lock Detect	Set 0 to operate normally.
0x1A[5:0]	LD pin Control	Set 04h to select Current source lock detect if using the LD pin comparator.
0x1D[3]	LD pin Comparator Enable	Set 1 if using. When set 0 (disabled), the automatic holdover function treats the LD pin as always high.
0x1D[1]	External Holdover Control	Set 0 to use the automatic holdover function.
0x1D[2][0]	Holdover Enable	Set 1 to enable holdover.
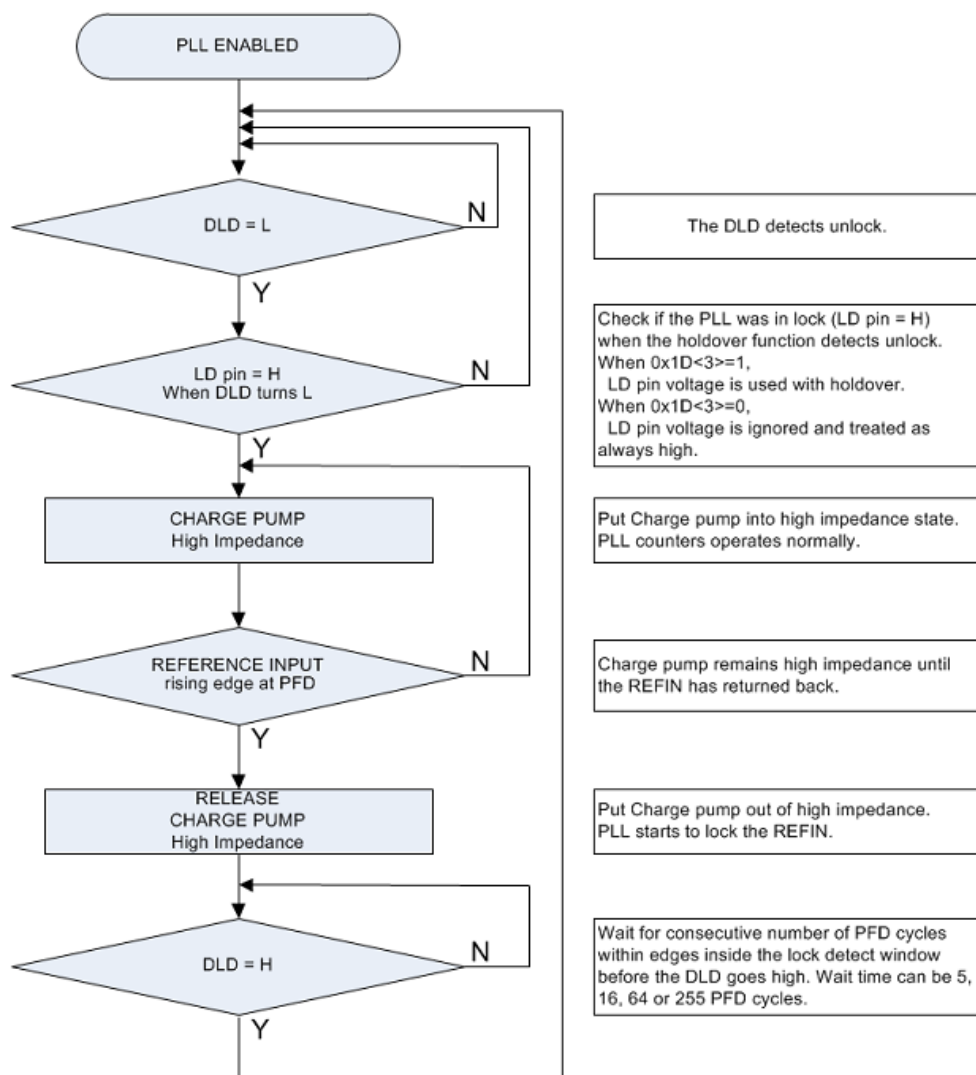
Figure 19. Automatic Holdover

Frequency Status Monitors

The AK8186B has a frequency status monitor to indicate if the REF1/2 and the VCO frequency below a threshold frequency. There are two threshold frequencies such as normal and extended for REF1/2. The VCO frequency is monitored at the output of the prescaler.

Table 24 Setting Frequency Status Monitors

Monitored signal	Monitor Enable register	Minimum threshold frequency		Status indication register
VCO	0x1B[7]=1	0.5 MHz		0x1F[3]
REF2	0x1B[6]=1	normal	0.5 MHz (0x1A[6]=0)	0x1F[2]
REF1	0x1B[5]=1	extended	4 kHz (0x1A[6]=1)	0x1F[1]

CLOCK DISTRIBUTION

VCO DIVIDER

The VCO divider provides frequency division between the internal VCO and the clock distribution section. The VCO divider can be set to divide by 2,3,4,5 and 6 (0x1E0[2:0]). The output of the VCO divider has 50% duty even though the division is 3 and 5 due to the duty cycle compensation circuit. VCO divider can be bypassed when using an external VCO/VCXO. When bypassed, the input duty through CLK/$\overline{\text{CLK}}$ pins is not compensated.

Channel Dividers for LVPECL OUTPUTS

There are three channel dividers for LVPECL outputs. Each divider drives a pair of LVPECL outputs. The divider value Dx can be set 1 to 32.

$$Dx : M + N + 2 \quad (M,N : 0 \text{ to } 15, \quad Dx = 1 \text{ when the bypass bit is set.})$$

Table 25 Registers for LVPECL Channel Divider 0,1 and 2

Channel Divider	Low Cycles M	High Cycles N	Bypass	LVPECL outputs
0	0x190[7:4]	0x190[3:0]	0x191[7]	OUT0, OUT1
1	0x193[7:4]	0x193[3:0]	0x194[7]	OUT2, OUT3
2	0x196[7:4]	0x196[3:0]	0x197[7]	OUT4, OUT5

The divider has the duty cycle correction. It always operates and outputs 50% duty clocks.

Channel Dividers for LVDS/CMOS OUTPUTS

There are two channel dividers for LVDS/CMOS outputs. Each divider drives a pair of LVDS outputs(or two pair of CMOS outputs). The divider value Dx can be set 1 to 32.

$$Dx : M + N + 2 \quad (M,N : 0 \text{ to } 15, \quad Dx = 1 \text{ when the bypass bit is set.})$$

Table 26 Registers for LVPECL Channel Divider 3 and 4

Channel Divider		Low Cycles M	High Cycles N	Bypass	LVDS/LVCMOS outputs
3	3.1	0x199[7:4]	0x199[3:0]	0x19C[4]	OUT6(A,B), OUT7(A,B)
	3.2	0x19B[7:4]	0x19B[3:0]	0x19C[5]	
4	4.1	0x19E[7:4]	0x19E[3:0]	0x1A1[4]	OUT8(A,B), OUT9(A,B)
	4.2	0x1A0[7:4]	0x1A0[3:0]	0x1A1[5]	

The divider has the duty cycle correction. It always operates and outputs 50% duty clocks.

Synchronizing the Outputs: SYNC FUNCTION

The AK8186B clock outputs can be synchronized to each other. The SYNC function starts to operate by the following conditions.

1) The $\overline{SYNC}$ pin is forced low and then released (Manual sync).
2) By setting and then resetting the soft sync bit 0x230[0]
3) After a VCO calibration is completed.

The channel divider output status depends on the register setting of the channel divider such as Bypass bit, NoSync bit, Force High bit, Start High bit and Phase offset bits.
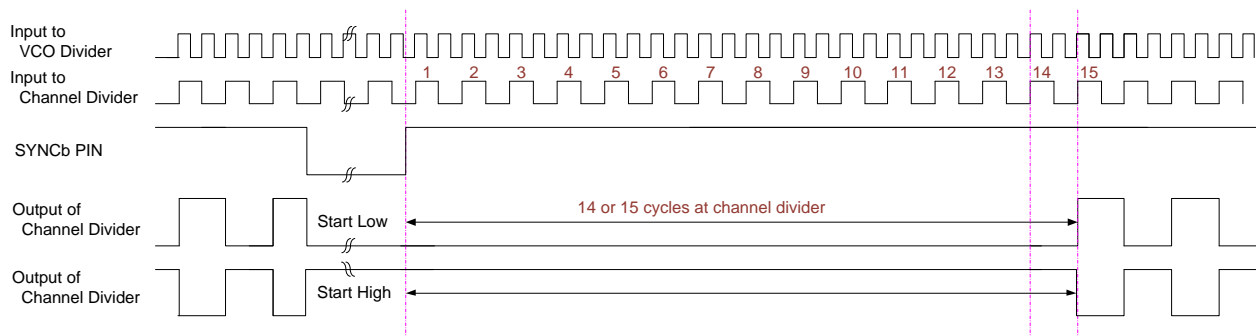
Figure 20. SYNC timing

Sync function can be disabled by NOSYNC bit. When the NOSYNC bit is set to 1, the SYNC function is disabled.

Table 27 SYNC Disable on Channel Divider

Channel Divider	NOSYNC bit
0	0x191[6]
1	0x194[6]
2	0x197[6]
3.1, 3.2	0x19C[3]
4.1, 4.2	0x1A1[3]

Phase Offset

Each channel divider has a programmable phase offset function. Phase offset means a delay to rising edge of output clock from zero offset output. Two kinds of bits such as Start High bit and Phase Offset bits affect Total Phase Offset. The phase offset is effective when the SYNC function is invoked.

Table 28 Start High and Phase Offset Registers on Channel Divider

Channel Divider	Start High	Phase Offset
0	0x191[4]	0x191[3:0]
1	0x194[4]	0x194[3:0]
2	0x197[4]	0x197[3:0]
3.1	0x19C[0]	0x19A[3:0]
3.2	0x19C[1]	0x19A[7:4]
4.1	0x1A1[0]	0x19F[3:0]
4.2	0x1A1[1]	0x19F[7:4]

When the Start High bit =1, the default phase offset exists before the phase offset defined by the phase offset bits. The default phase offset varies depending on the divider ratio. When the divider is bypassed, the Default Offset is equal to zero.

Total Phase Offset = Default Phase Offset + Phase Offset bits

Default Phase Offset
   Start High bit = 0 :   Zero
   Start High bit = 1 :   Roundup(Divider Ratio/2)   where Divider Ratio >=2

Example;
   Divider ratio = 3, Phase Offset bits = 2, then Default phase offset = 2
   Total Phase Offset = 2 + 2 = 4 clock cycles

Figure 21, 22 shows how those offsets work.
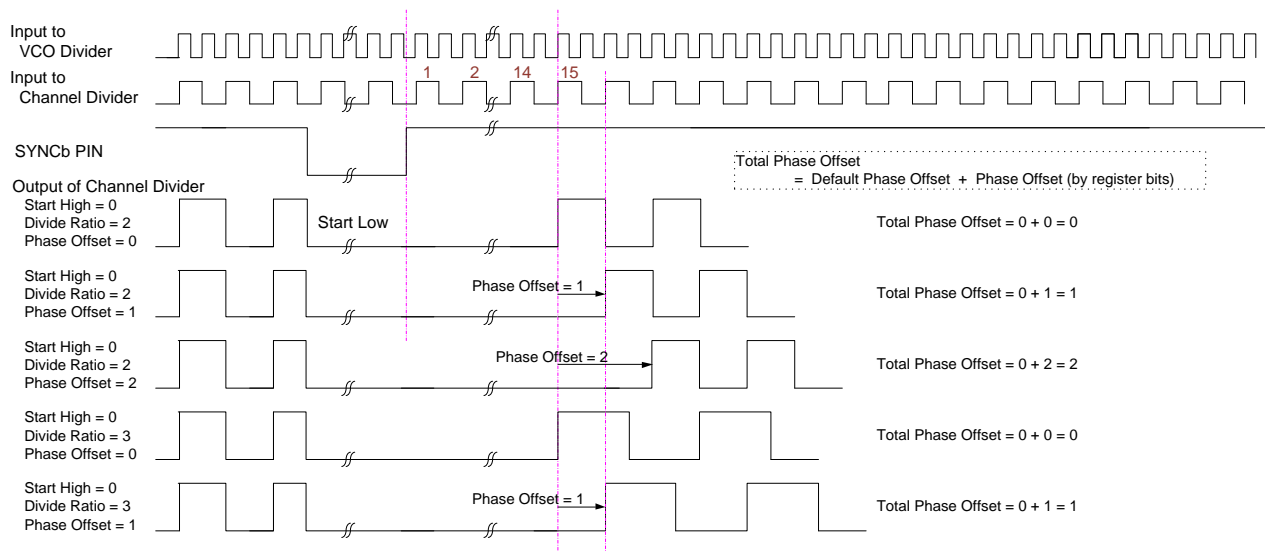
Figure 21. Channel Divider Phase Offset with Start High bit = 0 (Start Low)
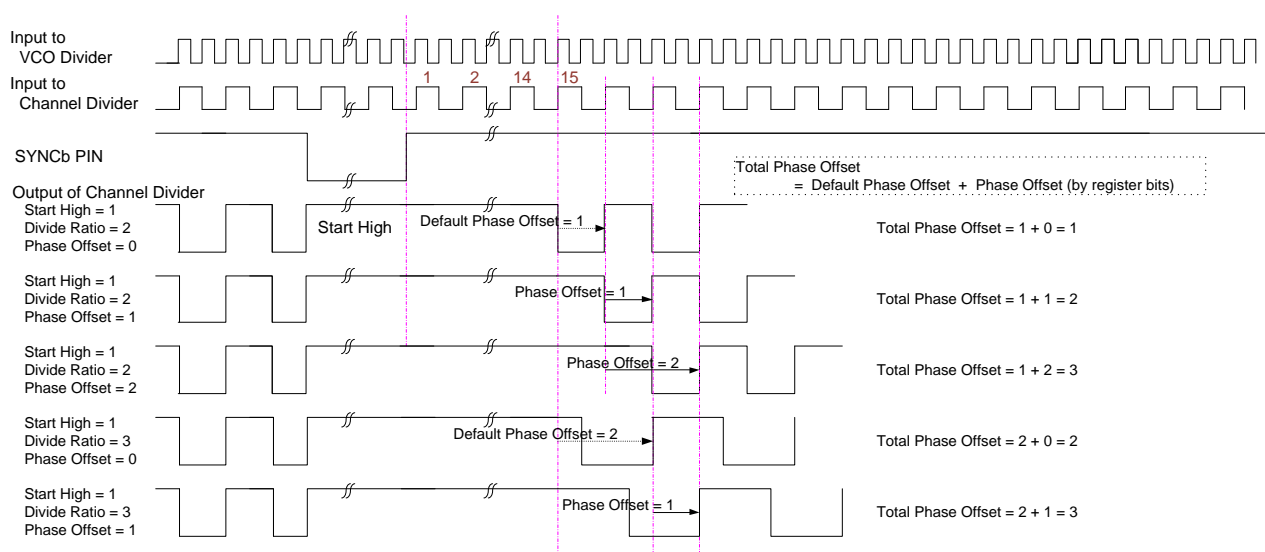
Figure 22 Channel Divider Phase Offset with Start High bit = 1 (Start High)

LVPECL OUTPUTS : OUT0 to OUT5

The AK8186B has three pair of LVPECL buffers. Each pair has dedicated VDD supply pin, VDD_LVPECL, allowing for a separate power supply to be used. VDD_LVPECL can be from 2.5V to 3.3V.

Table 29 LVPECL OUTPUTS Control Register

Control Item	Register
Invert Polarity	0xF0 to F5 [4]
Differential Voltage	0xF0 to F5 [3:2]
Power down*	0xF0 to F5 [1:0]

*)LVPECL outputs Hi-Z.

There are two modes of power down.
- Partial power down
- Power down

In Partial power down, an output stage is off but a differential input stage is on.
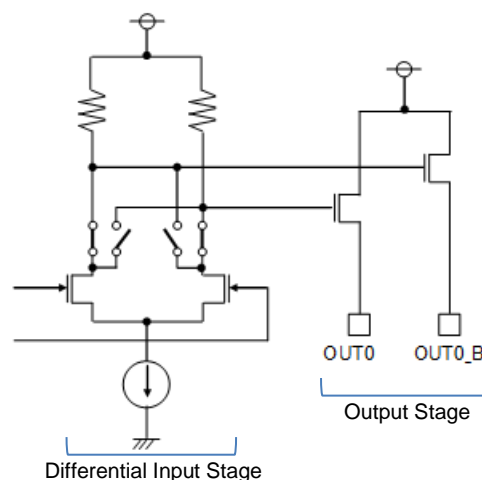
Figure 23. LVPECL Equivalent Circuit

LVDS/CMOS OUTPUTS : OUT6 to OUT9

OUT6 to OUT9 can be configured as an LVDS output or a pair of CMOS outputs.

Table 30 LVDS/CMOS outputs control register

Control Item	Register
Output Polarity	0x140 to 143 [7:5]
CMOS B turn on/off	0x140 to 143 [4]
Select LVDS/CMOS	0x140 to 143 [3]
LVDS Output Current	0x140 to 143 [2:1]
Power down*	0x140 to 143 [0]

*)LVDS outputs Hi-Z. CMOS outputs Low.
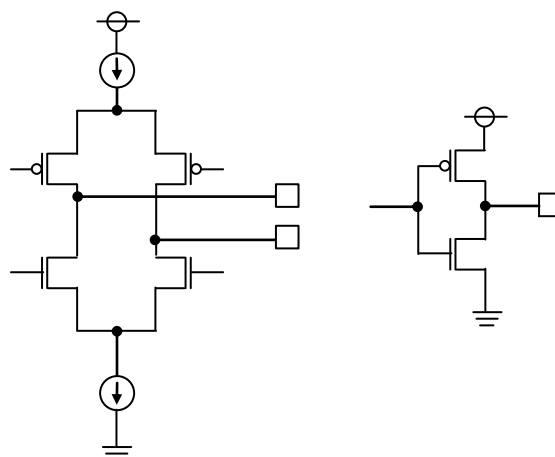
Figure 24. LVDS/CMOS Equivalent Circuit

RESET

The AK8186B has three types of reset as below.
1) Power-on reset
2) Asynchronous reset by $\overline{\text{RESET}}$ pin
3) Soft Reset by 0x00[5]

Power-on reset (POR)

At power on, an internal power-on reset signal is generated which initializes the register to the default settings. Note that the AK8186B does not execute the SYNC operation after power-on reset. To synchronize the clock outputs by SYNC function after power-up, SYNC_B pin must be released more than 0.5µs after starting a VCO calibration.
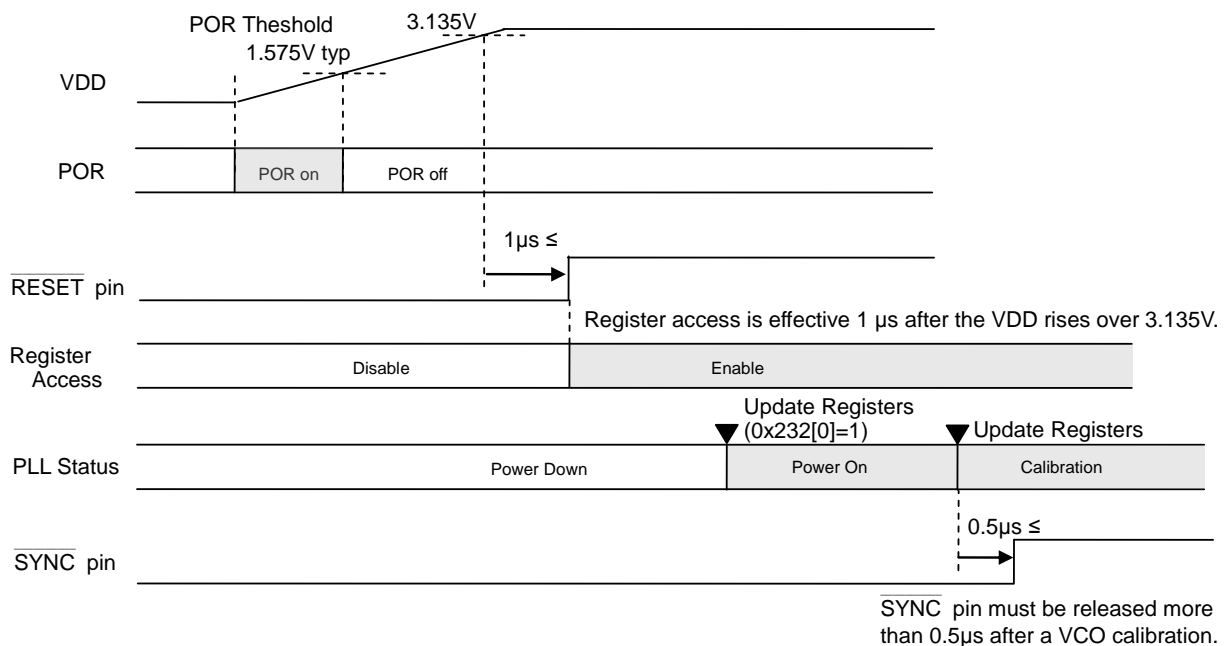
Figure 25. Recommended Power-up Sequence

Asynchronous reset by $\overline{\text{RESET}}$ pin

When the $\overline{\text{RESET}}$ pin is asserted, the AK8186B is immediately initialized to the default settings.

Soft reset by 0x00[5]

When the Soft reset bits 0x00[5] and [2] are set to 1, the AK8186B is immediately initialized to the default settings except the Soft reset bits without setting the update register 0x232[0] to 1. Both soft reset bits must be cleared by setting 0 since they are not self-cleaning bits.

POWER DOWN MODES

The AK8186B has two modes of power down.
 1) Chip power down
 2) Block power down (PLL, REF1/2, VCO, VCO divider, CLK Input, OUT0 to 9)

Chip Power Down by PDn pin

Operation   : Puts all the blocks except the bias to the analog block into power down mode.
Condition   : PDn pin is asserted low
Operation Timing : immediately
Note   : The registers are not reset. Serial Control Port is active. If the AK8186B clock outputs
                     must be synchronized to each other, a SYNC is required upon exiting power down (see
                     the SYNCHRONIZING THE OUTPUTS – SYNC FUNCTION). A VCO calibration is not
                     required when exiting power down.

PLL Power Down

Operation   : The PLL goes into power-down.
Condition   : Write 0x10[1:0] = 01b or 11b, then updates the register (0x232[0] =1b).
Operation Timing :
    Asychronous power-down mode : 0x10[1:0] = 01b
        immediately after the register update is executed.
    Synchronous power-down mode : 0x10[1:0] = 11b
        synchronized with the up/down signal for the CP after the register update is executed.
        This is for preventing the unwanted frequency jumps.

REF1, REF2 Power Down

Operation   : The REF1and/or REF2 goes into power-down.
Condition   : REF1: Write 0x1C[1] = 0b, then updates the register (0x232[0] =1b).
                      REF2: Write 0x1C[2] = 0b, then updates the register (0x232[0] =1b).
Operation Timing : immediately after the register update is executed.
Note   : The REF1/REF2 can not be powered down when Automatic Switchover is active.

VCO and CLK Input Power Down

Operation   : The VCO, VCO divider and CLK input section can be power down by 0x1E1[4:1]..
Condition   : Set 0x1E1[4:1] to the adequate value depending on your need, then updates the
                      register (0x232[0] =1b). See the register map function description of VCO, VCO divider
                      and CLK Input register (0x1E1).
Operation Timing : immediately after the register update is executed.

Distribution Power Down

Operation   : All of output buffers go into power-down.
Condition   : Write 0x230[1] = 1b, then updates the register (0x232[0] =1b).
Operation Timing : immediately after the register update is executed.

Individual Clock Output Power Down (OUT0 to OUT9)

Operation   : Any of the clock outputs goes into power-down.
Condition   : Write the appropriate registers below, then updates the register (0x232[0] =1b).
Operation Timing   : immediately after the register update is executed.

Table 31 Power down register for OUTPUTS

Output	Port	Register
LVPECL	OUT0	0xF0[1:0]
	OUT1	0xF1[1:0]
	OUT2	0xF2[1:0]
	OUT3	0xF3[1:0]
	OUT4	0xF4[1:0]
	OUT5	0xF5[1:0]
LVDS/ CMOS	OUT6	0x140[0]
	OUT7	0x141[0]
	OUT8	0x142[0]
	OUT9	0x143[0]

SERIAL CONTROL PORT

The AK8186B has a 3 or 4-wire serial control port which is compatible with both the Motorola SPI® and Intel SSR® protocols. The function of the serial control port is as follows.

- Read/write access to all registers
- Single/Multiple byte access
- MSB/LSB first transfer format
- Data output on SDIO pin (3-wire access: default) or SDO pin (4-wire access)
- Long instruction only (16 bits)

SERIAL CONTROL PORT PIN DESCRIPTIONS
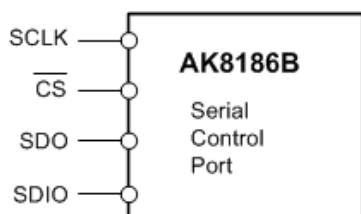
Figure 26. Serial Control Port

Table 32 Serial Control Port Pin Descriptions

Pin No.	Pin Name	Descriptions
16	SCLK	Serial Clock Input. Write data bits are sampled at the rising edge of this clock. Read data bits are sampled at the falling edge of this clock. Pulled down by an internal 30kΩ resistor.
17	$\overline{CS}$	Chip Select. An active low input. When $\overline{CS}$=low, read/write access is allowed. When $\overline{CS}$=high, SDIO and SDO become high impedance. Pulled up by an internal 30kΩ resistor.
21	SDO	Serial Data Output. Used only in the unidirectional mode (0x00[7]=1,[0]=1).
22	SDIO	Serial Data Input/Output. When 0x00[7]=0,[0]=0, this works in the bidirectional mode. When 0x00[7]=1,[0]=1, this works in the unidirectional mode.

GENERAL DESCRIPTION OF SERIAL CONTROL PORT

The following section describes the function of the serial control port.

Communication Cycle

Serial communication cycle consists of two parts. The first one is a 16-bit instruction section. The second one is a data section. Multibyte data can be transferred.
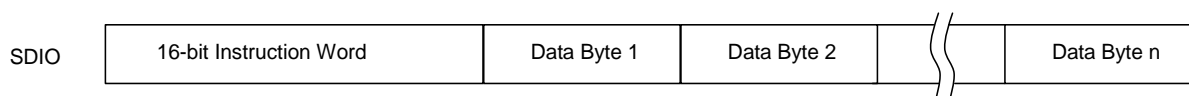
Figure 27. Serial Port Communication Cycle

Since the AK8186B supports only the long instruction (16 bits) mode, the register 0x00[4:3] must be 11b.

The Instruction Word (16 bits)

The instruction consists of 3 parts; Read/Write command, Byte to transfer and Address. See below.

MSB   LSB

I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/W̄	W1	W0	A12=0	A11=0	A10=0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
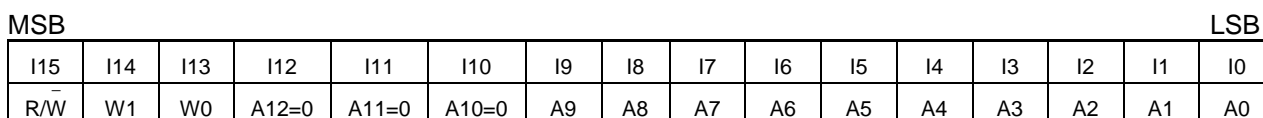
Figure 28. 16-bit Instruction Word

Table 33 16-bit Instruction Word

Bit	Name	Description
I15	R/W̄	Read or Write
I14 - I13	W1 - W0	Length of a transfer in bytes (See Table 34)
I12 - I0	A12 - A0	Address For multibyte transfers, this address is the starting byte address.

Table 34 Byte Transfer Count

W1	W0	Byte to transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Streaming mode is to transfer more than three bytes. It does not skip over reserved or blank registers.

WRITE

When I15=0, write operation is executed. The timing chart of 2-byte data write is shown below. Write data is sampled at the rising edge of SCLK.
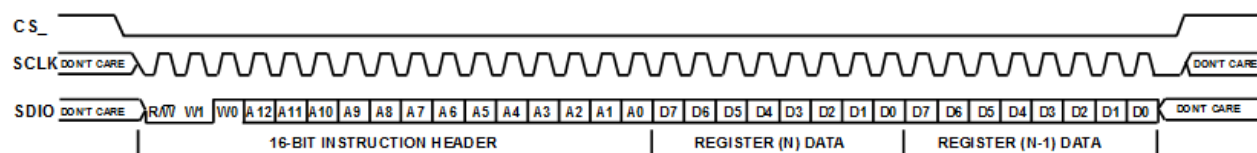
Figure 29. Serial Contorl Port - WRITE - MSB First

Write in Streaming mode

When data is transferred in streaming mode, the reserved and blank registers are not skipped over. Any data written to those registers does not affect the operation of the AK8186B.

Update Register

The serial control port has a two-step registers. It consists of a buffer register and an active register.
When data is transferred to the serial control port, the data is written into the buffer register. At this point, the written data is not active. To make this data active, an update register operation is needed. When set 0x232[0]=1, the data in the buffer register is transferred to the active register. This is called "update register" and makes the data active. Any number of data can be written into the buffer register before executing the update register. 0x232[0] is self-clear bit register.

Update register operation is executed
when set 0x232<0>=1.
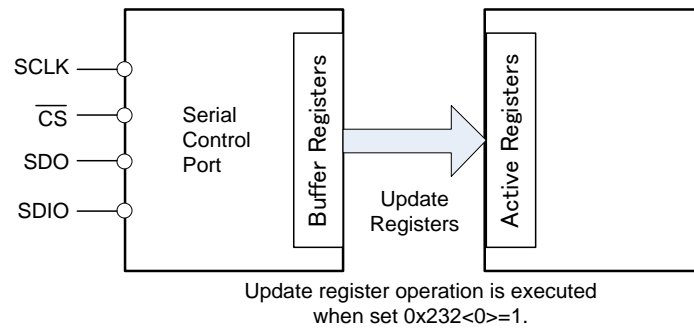
Figure 30. Buffer/Active Register

The serial control port configuration registers of 0x00 and 0x04 does not require the update register. The written data is immediately effective.

READ

When I15=1, read operation is executed. The timing chart of 3-byte data read is shown below. Read data is valid at the falling edge of SCLK.
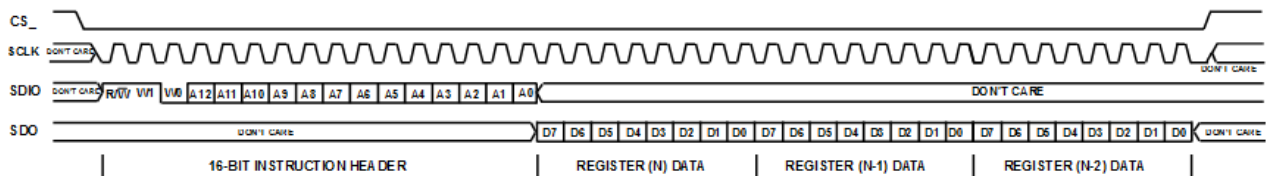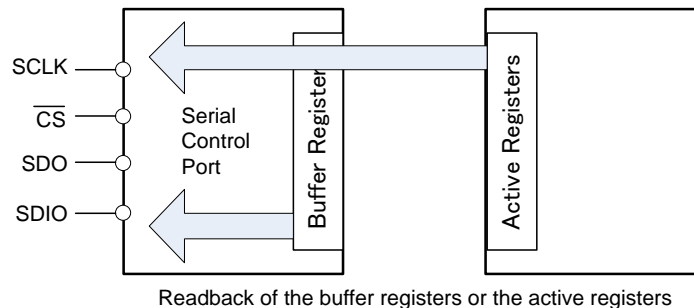

Figure 31. Serial Control Port - READ - MSB First

The serial control port can read back the data in the buffer registers or in the active registers. 0x04[0] selects which register is read.

Readback of the buffer registers or the active registers

Figure 32. Readback Registers

Read in Streaming mode

When data is transferred in streaming mode, the reserved and blank registers are not skipped over.

Bidirectional/Unidirectional mode

By default, the serial control port operates in the bidirectional mode. Both write data and readback data are transferred on the SDIO pin. In unidirectional mode, the readback data is on the SDO pin. 0x00[7][0] enables the SDO pin.

BUS STALLING IN READ/WRITE ACCESS

When 1, 2 or 3-byte transfer, but not streaming, $\overline{CS}$ can rise up on boundary of every data byte to stall the bus. While $\overline{CS}$ is high, read/write operation is suspended and the state machine of the serial control port stays in wait state. The operation resumes after $\overline{CS}$ goes down.
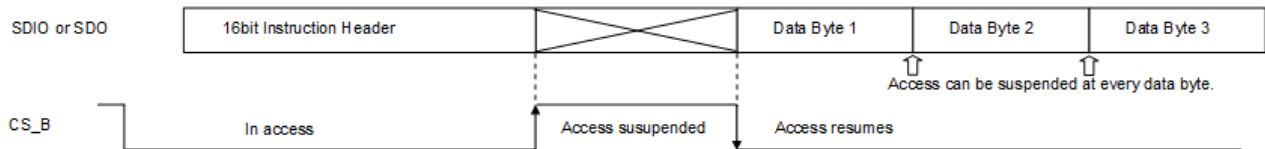
Figure 33. Bus Stalling

If the system gets out of the wait state, the state machine should be reset by the following procedure.
Return $\overline{CS}$ low and complete the transfer of remained data.
Return $\overline{CS}$ low for at least one complete SCLK cycle (but less than 8 cycles).

If $\overline{CS}$ goes high on non-boundary area, the read/write access is immediately cancelled.

MSB/LSB FIRST TRANSFERS

The AK8186B serial control port transfer the data by MSB first or LSB first. 0x00[6][1] selects one of which. Default is MSB first.

MSB first

The instruction and data are transferred from MSB. When the AK8186B executes multibyte access, the address included in the instruction is the start address. Address decrements at every data byte access.
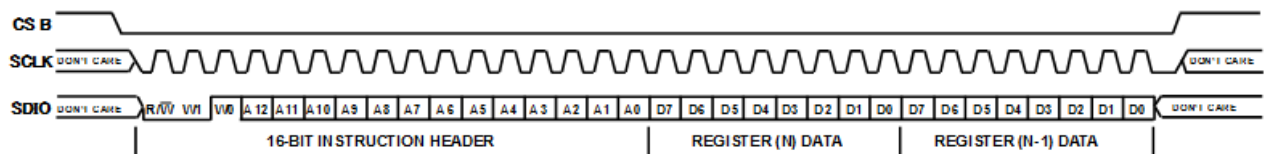
Figure 34. MSB First Transfers

LSB first

The instruction and data are transferred from LSB. When the AK8186B executes multibyte access, the address included in the instruction is the start address. Address increments at every data byte access.
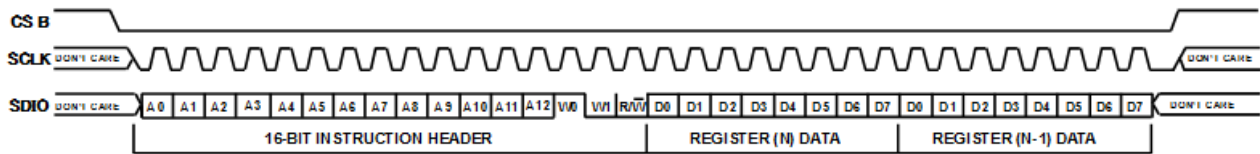
Figure 35. LSB First Transfers

In both MSB and LSB first modes, streaming mode stops at the address of 0x232. Note that the reserved and blank registers are not skipped.

Table 35 Stop Sequence in Streaming mode

Mode	Address Direction	Stop Sequence
LSB first	Increment	0x230, 0x231, 0x232, Stop
MSB first	Decrement	0x001, 0x000, 0x232, Stop

The serial control port is configured by the register 0x00[7:4]. 0x00[3:0] should be mirrored to 0x00[7:4]. This makes it no matter whether the data is written from MSB or LSB.

REGISTER MAP

Addr (HEX)	Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
Serial Control Port										
00	Serial Port Configuration	SDO Active	LSB First	Soft Reset	Long Instruction	Long Instruction	Soft Reset	LSB First	SDO Active	18
01		Blank								
02		Reserved								
03		Part ID (read only)								43
04	Read Back Control	Blank							Read Back Active Registers	00
PLL										
10	PFD & CP	PFD Polarity	Charge Pump Current			Charge Pump Mode		PLL Power Down		7D
11	R Counter	14-bit R Divider Bits<7:0>								01
12		Blank		14-bit R Divider Bits<13:8>						00
13	A Counter	Blank		6-bit A counter						00
14	B Counter	13-bit B counter Bits<7:0>								03
15		Blank		13-bit B counter Bits<12:8>						00
16	PLL Control 1	Set CP Pin To VDD/2	Reset R Counter	Reset A&B Counters	Reset All Counters	B Counter Bypass	Prescaler P			06
17	PLL Control 2	STATUS Pin Control						Reserved		00
18	PLL Control 3	Reserved	Lock Detect Counter		Digital Lock Detect Window	Disable Digital Lock Detect	VCO Calibration Divider		VCO Cal Now	06
19	PLL Control 4	R,A,B Counters SYNC Pin Reset	Reserved				Reserved			00
1A	PLL Control 5	Reserved	Reference Frequency Monitor Threshold	LD Pin Control						00
1B	PLL Control 6	VCO Frequency Monitor	REF2 Frequency Monitor	REF1 Frequency Monitor	REFMON Pin Control					00
1C	PLL Control 7	Blank	Select REF2	Use REF_SEL Pin	Automatic Reference Switchover	Stay on REF2	REF2 Power On	REF1 Power On	Differential Reference	00
1D	PLL Control 8	Reserved			PLL Status Register Disable	LD Pin Comparator Enable	Holdover Enable	External Holdover Control	Holdover Enable	00
1E	PLL Control 9	Reserved								00
1F	PLL Readback	Reserved	VCO Cal Finished	Holdover Active	REF2 Selected	VCO Frequency Threshold	REF2 Frequency Threshold	REF1 Frequency Threshold	Digital Lock Detect	--
20 to 4F		Blank								

Addr (HEX)	Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
A0		Blank								Reserved	01
A1		Blank		Reserved							00
A2		Blank		Reserved							00
A3		Blank								Reserved	01
A4		Blank		Reserved							00
A5		Blank		Reserved							00
A6		Blank								Reserved	01
A7		Blank		Reserved							00
A8		Blank		Reserved							00
A9		Blank								Reserved	01
AA		Blank		Reserved							00
AB		Blank		Reserved							00
AC to EF		Blank									
LVPECL Outputs											
F0	OUT0	Blank			OUT0 Invert	OUT0 LVPECL Differential Voltage		OUT0 Power-Down			08
F1	OUT2	Blank			OUT1 Invert	OUT1 LVPECL Differential Voltage		OUT1 Power-Down			0A
F2	OUT2	Blank			OUT2 Invert	OUT2 LVPECL Differential Voltage		OUT2 Power-Down			08
F3	OUT3	Blank			OUT3 Invert	OUT3 LVPECL Differential Voltage		OUT3 Power-Down			0A
F4	OUT4	Blank			OUT4 Invert	OUT4 LVPECL Differential Voltage		OUT4 Power-Down			08
F5	OUT5	Blank			OUT5 Invert	OUT5 LVPECL Differential Voltage		OUT5 Power-Down			0A
F6-13F		Blank									
LVDS/CMOS Outputs											
140	OUT6	OUT6 CMOS Output Polarity		OUT6 LVDS/CMOS Output Polarity	OUT6 CMOS B	OUT6 Select LVDS/CMOS	OUT6 LVDS Output Current		OUT6 Power-Down		42
141	OUT7	OUT7 CMOS Output Polarity		OUT7 LVDS/CMOS Output Polarity	OUT7 CMOS B	OUT7 Select LVDS/CMOS	OUT7 LVDS Output Current		OUT7 Power-Down		43
142	OUT8	OUT8 CMOS Output Polarity		OUT8 LVDS/CMOS Output Polarity	OUT8 CMOS B	OUT8 Select LVDS/CMOS	OUT8 LVDS Output Current		OUT8 Power-Down		42
143	OUT6	OUT9 CMOS Output Polarity		OUT9 LVDS/CMOS Output Polarity	OUT9 CMOS B	OUT9 Select LVDS/CMOS	OUT9 LVDS Output Current		OUT9 Power-Down		43
144-18F		Blank									
LVPECL Channel Dividers											
190	Divider 0 (PECL)	Divider 0 Low Cycles				Divider 0 High Cycles					00
191		Divider 0 Bypass	Divider 0 No Sync	Divider 0 Force High	Divider 0 Start High	Divider 0 Phase Offset					80
192		Blank		Reserved				Reserved			00
193	Divider 1 (PECL)	Divider 1 Low Cycles				Divider 1 High Cycles					BB
194		Divider 1 Bypass	Divider 1 No Sync	Divider 1 Force High	Divider 1 Start High	Divider 1 Phase Offset					00
195		Blank		Reserved				Reserved			00
196	Divider 2 (PECL)	Divider 2 Low Cycles				Divider 2 High Cycles					00
197		Divider 2 Bypass	Divider 2 No Sync	Divider 2 Force High	Divider 2 Start High	Divider 2 Phase Offset					00
198		Blank		Reserved				Reserved			00

Addr (HEX)	Parameter	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
LVDS/CMOS Channel Dividers										
199	Divider 3 (LVDS/CMOS)	Low Cycles Divider 3.1				High Cycle Divider 3.1				22
19A		Phase Offset Divider 3.2				Phase Offset Divider 3.1				00
19B		Low Cycles Divider 3.2				High Cycles Divider 3.2				11
19C		Reserved		Bypass Divider3.2	Bypass Divider 3.1	Divider 3 No Sync	Divider 3 Force High	Start High Divider 3.2	Start High Divider 3.1	00
19D		Blank		Reserved					Reserved	00
19E	Divider 4 (LVDS/CMOS)	Low Cycles Divider 4.1				High Cycle Divider 4.1				22
19F		Phase Offset Divider 4.2				Phase Offset Divider 4.1				00
1A0		Low Cycles Divider 4.2				High Cycles Divider 4.2				11
1A1		Reserved		Bypass Divider4.2	Bypass Divider 4.1	Divider 4 No Sync	Divider 4 Force High	Start High Divider 4.2	Start High Divider 4.1	00
1A2		Blank		Reserved					Reserved	00
1A3		Reserved								
1A4 to 1DF		Blank								
VCO Divider and CLK Input										
1E0	VCO Divider	Blank				Reserved	VCO Divider			02
1E1	Input CLKs	Reserved			Power-Down Clock Input Section	Power-Down VCO clock interface	Power-down VCO & CLK	Select VCO or CLK	Bypass VCO Divider	00
1E2 to 22A		Blank								
System										
230	Power Down and Sync.	Reserved					Power-Down Sync	Power-Down Distribution	Soft Sync	00
231		Blank				Reserved				00
Update All Registers										
232	Update all Registers	Blank							Update All Registers	00

REGISTER MAP FUNCTION DESCRIPTIONS

Serial Port Configuration

Register Address (Hex)	Bit(s)	Name	Description

0x000	7	SDO Active	Selects unidirectional or bidirectional data transfer mode.
			  0: Bidirectional mode: (default)
			    SDIO pin used for write and read; SDO set high impedance.
			  1: Unidirectional mode:
			    SDO pin used for read; SDIO pin used for write.

	6	LSB First	MSB or LSB data orientation
			  0: data-oriented MSB first: addressing decrements. (default)
			  1: data-oriented LSB first: addressing increments.

	5	Soft Reset	Soft Reset
			  1: Soft Rest (not self-clearing); restores default values to internal registers.
			    Must be cleared to "0" to complete operation.

	4	Long Instruction	Should be always "1": 16bit instruction(long).

	3:0	Mirror[7:4]	Bit[3:0] should be always mirror [7:4] so that it does not matter whether the part is in MSB or LSB first mode(see Register 0x00[6]). User should set bits as follows.
			  [0]=[7]
			  [1]=[6]
			  [2]=[5]
			  [3]=[4]

0x003	7:0	Part ID	Part ID of the AK8186B. (read only) AK8186B : 0x43

0x004	0	Read Back Active Reg.	Select register bank used for read back.
			  0: read back buffer registers (default)
			  1: read back active registers

PLL Configuration

Register Address (Hex)	Bit(s)	Name	Description
0x010	7	PFD Polarity	Sets the PFD Polarity. The on-chip VCO requires positive polarity. 0 : Positive ; higher control voltage produces higher frequency (default) 1 : Negative; higher control voltage produces lower frequency
	6:4	CP Current	Charge Pump current (with CPRSET=5.1kΩ). **[6:5:4] Icp(mA)** 0 0 0 0.6 0 0 1 1.2 0 1 0 1.8 0 1 1 2.4 1 0 0 3.0 1 0 1 3.6 1 1 0 4.2 1 1 1 4.8 (default)
	3:2	CP Mode	Charge pump operating mode. **[3:2] Charge pump mode** 0 0 High impedance state 0 1 Force source current (pump up) 1 0 Force sink current(pump down) 1 1 Normal operation. (default)
	1:0	PLL Power Down	PLL operating mode. **[1:0] PLL Mode** 0 0 Normal operation. 0 1 Asynchronous power-down. (default) 1 0 Normal operation. 1 1 Synchronous power-down.
0x011	7:0	14-Bit R Divider Bits[7:0] (LSB)	R divider LSBs, lower eight bits (default=0x01).
0x012	5:0	14-Bit R Divider Bits[13:8] (MSB)	R divider MSBs, upper six bits (default=0x00).
0x013	5:0	6-Bit A Counter	A counter (part of N divider) (default=0x00).
0x014	7:0	13-Bit B Counter Bits[7:0]	B counter (part of N divider). Lower eight bits (default=0x03).
0x015	4:0	13-Bit B Counter Bits[12:8]	B counter (part of N divider). Upper eight bits (default=0x00).
0x016	7	Set CP pin To VDD/2	Sets the CP pin to one-half of the VDD supply voltage. 0: CP normal operation (default). 1: CP pin set to VDD/2.
	6	Rest R Counters	Resets R counter (R divider) 0: normal (default) 1: reset R counter.

Register Address (Hex)	Bit(s)	Name	Description

0x016	5	Reset A&B Counters	Resets A&B counters (part of N divider)
			   0: normal (default)
			   1: reset A & B counter.

	4	Reset All Counters	Resets R, A&B counters.
			   0: normal (default)
			   1: reset R, A & B counter.

	3	B Counter Bypass	B counter bypass. This is valid only when operating the prescaler in FD mode.
			   0: normal mode (default)
			   1: B counter is set to divide-by-1. This allows the prescaler setting to determine the divide for the N divider.

	2:0	Prescaler P	Prescaler: DM=Dual modulus and FD = fixed divide. **External VCO/VCXO** ; 1E1[1]=0 **[2:1:0] Mode Prescaler** 0 0 0 FD Divide-by-1 0 0 1 FD Divide-by-2 0 1 0 DM Divide-by-2 (2/3 mode) 0 1 1 DM Divide-by-4 (4/5 mode) 1 0 0 DM Divide-by-8 (8/9 mode) 1 0 1 DM Divide-by-16 (16/17 mode) 1 1 0 DM Divide-by-32 (32/33 mode) (default) 1 1 1 FD Divide-by-3 **Internal VCO** ; 1E1[1]=1 **[2:1:0] Mode Prescaler** 0 X X DM Divide-by-32 (32/33 mode) 1 0 0 DM Divide-by-8 (8/9 mode) 1 0 1 DM Divide-by-16 (16/17 mode) 1 1 X DM Divide-by-32 (32/33 mode)

0x017	7:2	STATUS Pin Control	Selects the signal that is connected to the STATUS pin.
			
			                  Level or
			                  Dynamic
			[7:6:5:4:3:2] Signals Signal at STATUS Pin
			 0 0 0 0 0 0 LVL Ground(dc) (default).
			 0 0 0 0 0 1 DYN N divider output
			 0 0 0 0 1 0 DYN R divider output
			 0 0 0 0 1 1 DYN A divider output.
			 0 0 0 1 0 0 DYN Prescaler output.
			 0 0 0 1 0 1 DYN PFD up pulse
			 0 0 0 1 1 0 DYN PFD down pulse
			 0 x x x x x LVL Ground(dc);for all other cases 0xxxxx not specified Above.
			The selections that follow are the same as REFMON.
			 1 0 0 0 0 0 LVL Ground(dc).
			 1 0 0 0 0 1 DYN REF1 clock
			 1 0 0 0 1 0 DYN REF2 clock (N/A differential mode)
			 1 0 0 0 1 1 DYN Selected reference to PLL
			 1 0 0 1 0 0 DYN Unselected reference to PLL
			 1 0 0 1 0 1 LVL Status of selected reference
			 1 0 0 1 1 0 LVL Status of unselected reference
			 1 0 0 1 1 1 LVL Status REF1 frequency.(active high)

Register Address (Hex)	Bit(s)	Name	Description
0x017	7:2	STATUS Pin Control	**Level or Dynamic**

[7:6:5:4:3:2]	Signals	Signal at STATUS Pin
1 0 1 0 0 0	LVL	Status REF2 frequency. (active high)
1 0 1 0 0 1	LVL	(Status REF1 Freq.) AND (Status REF2 Freq.)
1 0 1 0 1 0	LVL	(DLD) AND (Status of selected reference) AND (status of VCO)
1 0 1 0 1 1	LVL	Status of VCO Frequency (active high)
1 0 1 1 0 0	LVL	Selected reference (Low=REF1,High=REF2)
1 0 1 1 0 1	LVL	Digital Lock Detect(DLD); active High
1 0 1 1 1 0	LVL	Holdover active(active high)
1 0 1 1 1 1	LVL	LD pin comparator output (active high).
1 1 0 0 0 0	LVL	VDD (PLL supply)
1 1 0 0 0 1	DYN	(REF1 Clock)n
1 1 0 0 1 0	DYN	(REF2 Clock)n
1 1 0 0 1 1	DYN	(Selected reference to PLL)n
1 1 0 1 0 0	DYN	(Unselected reference to PLL)n
1 1 0 1 0 1	LVL	Status of selected reference: active low
1 1 0 1 1 0	LVL	Status of unselected reference: active low
1 1 0 1 1 1	LVL	Status of REF1 frequency(active low)
1 1 1 0 0 0	LVL	Status of REF2 frequency(active low)
1 1 1 0 0 1	LVL	((Status REF1 Freq.) AND (Status REF2 Freq.))n
1 1 1 0 1 0	LVL	((DLD) AND (Status of selected reference) AND (status of VCO))n
1 1 1 0 1 1	LVL	Status of VCO Frequency (Active low)
1 1 1 1 0 0	LVL	Selected reference (Low=REF2,High=REF1).
1 1 1 1 0 1	LVL	Digital Lock Detect(DLD): Active Low
1 1 1 1 1 0	LVL	Holdover active(active low)
1 1 1 1 1 1	LVL	LD Pin comparator output(Active low)

Register Address (Hex)	Bit(s)	Name	Description
0x018	6:5	Lock Detect Counter	**[6:5]** **PFD Cycles Determine Lock**
			0 0 5 (default)
			0 1 16
			1 0 64
			1 1 255
	4	Digital Lock Detect Window	Digital Lock Detect Window Size

	Lock	Unlock	
0 : High Range	7.5ns	15ns	(default)
1 : Low Range	3.5ns	7ns	

Register Address (Hex)	Bit(s)	Name	Description

0x018	3	Disable DLD	Digital Lock Detect operation
			  0: normal lock detect operation (default)
			  1: disable lock detect

	2:1	VCO Cal Divider	VCO Calibration Divider. Divider used to generate the VCO calibration clock from the PLL reference clock.
			  [2:1] **VCO Calibration Clock Divider**
			  0 0 2
			  0 1 4
			  1 0 8
			  1 1 16 (default)

	0	VCO Cal Now	Bit used to initiate the VCO calibration. This bit must be toggled from 0 to 1 in the active registers. The sequence to initiate a calibration is: program to 0, followed by an update bit(Register 0x232[0]),; then programmed to 1, followed by another update bit(Register 0x232[0]). This sequence gives complete control over when the VCO calibration occurs relative to the programming of other registers that can impact the calibration.

0x019	7:6	R,A,B Counters $\overline{\text{SYNC}}$ Pin RESET	**[7:6]** **Action**
			  0 0 Do nothing on $\overline{\text{SYNC}}$(default)
			  0 1 Asynchronous reset
			  1 0 Synchronous reset
			  1 1 Do nothing on $\overline{\text{SYNC}}$

0x01A	6	Reference Frequency Monitor Threshold	Sets the reference (REF1/REF2) frequency monitor's detection threshold frequency. This does not affect the VCO frequency monitor's detection threshold. See Table 16: REF1, REF2 and VCO Frequency Status Monitor parameter.
			  0: frequency valid if frequency is above the higher frequency threshold (default).
			  1: frequency valid if frequency is above the lower frequency threshold.

Register Address (Hex)	Bit(s)	Name	Description
0x01A	5:0	LD Pin Control	Selects the signal that is connected to the LD pin. **[5:4:3:2:1:0] Signals Signal at LD Pin** 0 0 0 0 0 0 LVL DLD (High=lock, Low=unlock) (default) 0 0 0 0 0 1 DYN P-Channel, open-drain lock detect(analog LD) 0 0 0 0 1 0 DYN N-Channel, open-drain lock detect(analog LD) 0 0 0 0 1 1 HIZ High-Z LD pin. 0 0 0 1 0 0 CUR Current source LD(110uA when DLD is true). 0 x x x x x LVL Ground(dc);for all other cases 0xxxxx not specified Above. The selections that follow are the same as REFMON except 101111 and 111111. 1 0 0 0 0 0 LVL Ground(dc). 1 0 0 0 0 1 DYN REF1 clock 1 0 0 0 1 0 DYN REF2 clock (N/A differential mode) 1 0 0 0 1 1 DYN Selected reference to PLL 1 0 0 1 0 0 DYN Unselected reference to PLL 1 0 0 1 0 1 LVL Status of selected reference 1 0 0 1 1 0 LVL Status of unselected reference 1 0 0 1 1 1 LVL Status REF1 frequency.(active high) 1 0 1 0 0 0 LVL Status REF2 frequency.(active high) 1 0 1 0 0 1 LVL (Status REF1 Freq.) AND (Status REF2 Freq.) 1 0 1 0 1 0 LVL (DLD) AND (Status of selected reference) AND (status of VCO) 1 0 1 0 1 1 LVL Status of VCO Frequency (Active high) 1 0 1 1 0 0 LVL Selected reference (Low=REF1,High=REF2) 1 0 1 1 0 1 LVL Digital Lock Detect(DLD): Active High 1 0 1 1 1 0 LVL Holdover active(active high) 1 0 1 1 1 1 LVL N/A do not use. 1 1 0 0 0 0 LVL VDD (PLL supply) 1 1 0 0 0 1 DYN (REF1 Clock)n 1 1 0 0 1 0 DYN (REF2 Clock)n 1 1 0 0 1 1 DYN (Selected reference to PLL)n 1 1 0 1 0 0 DYN (Unselected reference to PLL)n 1 1 0 1 0 1 LVL Status of selected reference: active low 1 1 0 1 1 0 LVL Status of unselected reference: active low 1 1 0 1 1 1 LVL Status of REF1 frequency(active low) 1 1 1 0 0 0 LVL Status of REF2 frequency(active low) 1 1 1 0 0 1 LVL ((Status REF1 Freq.) AND (Status REF2 Freq.))n 1 1 1 0 1 0 LVL ((DLD) AND (Status of selected reference) AND (status of VCO))n 1 1 1 0 1 1 LVL Status of VCO Frequency (active low) 1 1 1 1 0 0 LVL Selected reference (Low=REF2,High=REF1). 1 1 1 1 0 1 LVL Digital Lock Detect(DLD): active low 1 1 1 1 1 0 LVL Holdover active(active low) 1 1 1 1 1 1 LVL N/A do not use.

Register Address (Hex)	Bit(s)	Name	Description
0x01B	7	VCO Frequency Monitor	Enable or disable VCO frequency monitor. 0: disable VCO frequency monitor (default). 1: enable VCO frequency monitor.
	6	REF2(REFINn) Frequency Monitor	Enable or disable REF2 frequency monitor. 0: disable REF2 frequency monitor (default). 1: enable REF2 frequency monitor.
	5	REF1(REFIN) Frequency Monitor	Enable or disable REF1(REFIN) frequency monitor. 0: disable REF1(REFIN) frequency monitor (default). 1: enable REF1(REFIN) frequency monitor.
	4:0	REFMON Pin Control	**[4:3:2:1:0] Signals Signal at REFMON Pin** 0 0 0 0 0 LVL Ground(dc) (default). 0 0 0 0 1 DYN REF1 clock 0 0 0 1 0 DYN REF2 clock (N/A differential mode) 0 0 0 1 1 DYN Selected reference to PLL 0 0 1 0 0 DYN Unselected reference to PLL 0 0 1 0 1 LVL Status of selected reference 0 0 1 1 0 LVL Status of unselected reference 0 0 1 1 1 LVL Status REF1 frequency.(active high) 0 1 0 0 0 LVL Status REF2 frequency.(active high) 0 1 0 0 1 LVL (Status REF1 Freq.) AND (Status REF2 Freq.) 0 1 0 1 0 LVL (DLD) AND (Status of selected reference) AND (status of VCO) 0 1 0 1 1 LVL Status of VCO Frequency (Active high) 0 1 1 0 0 LVL Selected reference (Low=REF1,High=REF2) 0 1 1 0 1 LVL Digital Lock Detect(DLD): Active High 0 1 1 1 0 LVL Holdover active(active high) 0 1 1 1 1 LVL LD Pin comparator output(Active high) 1 0 0 0 0 LVL VDD (PLL supply) 1 0 0 0 1 DYN (REF1 Clock)n 1 0 0 1 0 DYN (REF2 Clock)n 1 0 0 1 1 DYN (Selected reference to PLL)n 1 0 1 0 0 DYN (Unselected reference to PLL)n 1 0 1 0 1 LVL Status of selected reference: active low 1 0 1 1 0 LVL Status of unselected reference: active low 1 0 1 1 1 LVL Status of REF1 frequency(active low) 1 1 0 0 0 LVL Status of REF2 frequency(active low) 1 1 0 0 1 LVL ((Status REF1 Freq.) AND (Status REF2 Freq.))n 1 1 0 1 0 LVL ((DLD) AND (Status of selected reference) 1 1 0 1 1 LVL Status of VCO Frequency (Active low) 1 1 1 0 0 LVL Selected reference (Low=REF2,High=REF1). 1 1 1 0 1 LVL Digital Lock Detect(DLD): Active Low 1 1 1 1 0 LVL Holdover active(active low) 1 1 1 1 1 LVL LD Pin comparator output(Active low)

Register Address (Hex)	Bit(s)	Name	Description

0x01C	6	Select REF2	If Register 0x1C[5]=0, select reference for PLL.
			  0: select REF1 (default)
			  1: select REF2

	5	Use REF_SEL Pin	If Register 0x1C[4]=0, set method of PLL reference selection.
			  0: use Register 0x1C[6] (default).
			  1: use REF_SEL pin.

	4	Automatic Reference Switchover	Automatic or manual reference selection switchover. Single-ended reference mode must be selected by Register 0x1C[0]=0.
			  0: manual reference switchover (default).
			  1: automatic reference switchover.

	3	Stay on REF2	Stays on REF2 after switchover
			  0: return to REF1 automatically when REF1 status good again (default).
			  1: stay on REF2 after switchover. Do not automatically return to REF1 .

	2	REF2 Power On	When automatic reference switchover is disabled, this bit returns the REF2 power on.
			  0: REF2 Power off (default).
			  1: REF2 Power on.

	1	REF1 Power On	When automatic reference switchover is disabled, this bit returns the REF1 power on.
			  0: REF1 Power off (default).
			  1: REF1 Power on.

	0	Differential Reference	Selects the PLL reference mode, differential or single-ended. Single-ended must be selected for the automatic switchover or REF1 and REF2 to work.
			  0: single-ended reference mode (default).
			  1: differential reference mode.

Register Address (Hex)	Bit(s)	Name	Description
0x01D	4	PLL Status Register Disable	Disable the PLL status register read-back. 0: enable (default) 1: disable
	3	LD Pin Comparator Enable	Enable the LD pin voltage comparator, This function is used with the LP pin current source lock detect mode. When in the automatic holdover mode, this enables the use of the voltage on the LD pin to determine if the PLL was previously in a locked state. Otherwise, this can be used with the REFMON and STATUS pins to monitor the voltage on this PIN. 0: disable (default) 1: enable
	2	Holdover Enable	Along with[0] enables the holdover function. 0: holdover disabled (default) 1: holdover enabled
	1	Manual Holdover Control	Enable the manual hold control through the $\overline{\text{SYNC}}$ pin. (This disables the automatic holdover mode.) 0: automatic holdover mode-holdover controlled by automatic holdover circuit. (default) 1: manual holdover mode-holdover controlled by $\overline{\text{SYNC}}$ pin.
	0	Holdover Enable	Analog with[2] enables the holdover function. 0: holdover disabled (default) 1: holdover enabled

Register Address (Hex)	Bit(s)	Name	Description
0x01F	6	VCO Cal Finished	Read-only register: status of the VCO calibration. 　0: VCO calibration not finished 　1: VCO calibration finished
	5	Holdover Active	Read-only register: indicates if the part is in the holdover state(see Fig.19). This is not same as holdover enable. 　0: not in holdover. 　1: holdover state active.
	4	REF2 Selected	Read-only register: indicates which PLL reference is selected as the input to PLL. 　0: REF1 selected (or differential reference if in differential mode.) 　1: REF2 selected.
	3	VCO Frequency > Threshold	Read-only register: indicates if the VCO frequency is greater than the threshold (see Table 16, REF1, REF2, and VCO Frequency Status Monitor.). 　0: VCO frequency is less than threshold frequency. 　1: VCO frequency greater the threshold frequency.
	2	REF2 Frequency > Threshold	Read-only register: indicates if the frequency REF2 is greater than the threshold frequency set by Register 0x1A[6]. 　0: REF2 frequency is less than threshold frequency. 　1: REF2 frequency greater the threshold frequency.
	1	REF1 Frequency > Threshold	Read-only register: indicates if the frequency REF1 is greater than the threshold frequency set by Register 0x1A[6]. 　0: REF1 frequency is less than threshold frequency. 　1: REF1 frequency greater the threshold frequency.
	0	Digital Lock Detect	Read-only register: digital lock detect 　0: PLL is not locked. 　1: PLL is locked.

LVPECL Outputs

Register Address (Hex)	Bit(s)	Name	Description
0x0F0	4	Output Invert	Selects the output polarity. 0: non-inverting (default) 1: inverting
	3:2	OUT0 LVPECL Differential Voltage	Sets the LVPECL output differential voltage(Vod) **[3:2] Vod(mV)** 0 0 400 0 1 600 1 0 780 (default) 1 1 960
	1:0	OUT0 Power-Down	LVPECL power-down modes. **[1:0] Out Mode** 0 0 On Normal operation (default) 0 1 Off Partial Power-down (Outputs Hi-Z). 1 0 Off Partial Power-down (Outputs Hi-Z). 1 1 Off Power-down (Outputs Hi-Z)
0x0F1	4	Output Invert	Selects output polarity. 0: non-inverting (default) 1: inverting
	3:2	OUT1 LVPECL Differential Voltage	Sets the LVPECL output differential voltage(Vod) **[3:2] Vod(mV)** 0 0 400 0 1 600 1 0 780 (default) 1 1 960
	1:0	OUT1 Power-Down	LVPECL power-down modes. **[1:0] Out Mode** 0 0 On Normal operation 0 1 Off Partial Power-down (Outputs Hi-Z). 1 0 Off Partial Power-down (Outputs Hi-Z). (default) 1 1 Off Power-down (Outputs Hi-Z).
0x0F2	4	Output Invert	Selects output polarity. 0: non-inverting (default) 1: inverting
	3:2	OUT2 LVPECL Differential Voltage	Sets the LVPECL output differential voltage(Vod) **[3:2] Vod(mV)** 0 0 400 0 1 600 1 0 780 (default) 1 1 960
	1:0	OUT2 Power-Down	LVPECL power-down modes. **[1:0] Out Mode** 0 0 On Normal operation (default) 0 1 Off Partial Power-down (Outputs Hi-Z). 1 0 Off Partial Power-down (Outputs Hi-Z). 1 1 Off Power-down (Outputs Hi-Z).

Register Address (Hex)	Bit(s)	Name	Description

0x0F3	4	Output Invert	Selects output polarity.
			  0: non-inverting (default)
			  1: inverting

	3:2	OUT3 LVPECL Differential Voltage	Sets the LVPECL output differential voltage(Vod) **[3:2] Vod(mV)** 0 0 400 0 1 600 1 0 780 (default) 1 1 960
	1:0	OUT3 Power-Down	LVPECL power-down modes. **[1:0] Out Mode** 0 0 On Normal operation 0 1 Off Partial Power-down (Outputs Hi-Z). 1 0 Off Partial Power-down (Outputs Hi-Z). (default) 1 1 Off Power-down (Outputs Hi-Z).

0x0F4	4	Output Invert	Selects output polarity.
			  0: non-inverting (default)
			  1: inverting

	3:2	OUT4 LVPECL Differential Voltage	Sets the LVPECL output differential voltage(Vod) **[3:2] Vod(mV)** 0 0 400 0 1 600 1 0 780 (default) 1 1 960
	1:0	OUT4 Power-Down	LVPECL power-down modes. **[1:0] Out Mode** 0 0 On Normal operation (default) 0 1 Off Partial Power-down (Outputs Hi-Z). 1 0 Off Partial Power-down (Outputs Hi-Z). 1 1 Off Power-down (Outputs Hi-Z).

0x0F5	4	Output Invert	Selects output polarity.
			  0: non-inverting (default)
			  1: inverting

	3:2	OUT5 LVPECL Differential Voltage	Sets the LVPECL output differential voltage(Vod) **[3:2] Vod(mV)** 0 0 400 0 1 600 1 0 780 (default) 1 1 960
	1:0	OUT5 Power-Down	LVPECL power-down modes. **[1:0] Out Mode** 0 0 On Normal operation 0 1 Off Partial Power-down (Outputs Hi-Z). 1 0 Off Partial Power-down (Outputs Hi-Z). (default) 1 1 Off Power-down (Outputs Hi-Z).

LVDS/CMOS Outputs

Register Address (Hex)	Bit(s)	Name	Description
0x140	7:5	OUT6 Output Polarity	In CMOS mode,[7:5] select the output polarity of each CMOS output. In LVDS mode, only [5] determines LDVS polarity. **[7:6:5] OUT6(CMOS) OUT6n(CMOS) OUT6(LVDS)** 0 0 0 Non-inverting. Inverting. Non-inverting. 0 1 0 Non-inverting. Non-inverting. Non-inverting (default) 1 0 0 Inverting. Inverting. Non-inverting 1 1 0 Inverting. Non-inverting. Non-inverting 0 0 1 Inverting. Non-inverting. Inverting 0 1 1 Inverting. Inverting. Inverting 1 0 1 Non-inverting. Non-inverting. Inverting 1 1 1 Non-inverting. Inverting. Inverting
	4	OUT6 CMOS B	In CMOS mode, turn on/off the OUT6n output. There is no effect in LDVS mode. 0: turn off the OUT6n output. (default) 1: turn on the OUT6n output..
	3	OUT6 Select LVDS/CMOS	Selects LVDS or CMOS logic levels. 0: LVDS. (default) 1: CMOS.
	2:1	OUT6 LVDS Output Current	Sets output current level in LVDS mode. This has no effect CMOS mode, **[2:1] Current (mA) Recommend Termination (Ω)** 0 0 1.75 100 0 1 3.5 100 (default) 1 0 5.25 50 1 1 7.0 50
	0	OUT6 Power-Down	Power-down output(LVDS/CMOS). 0: Power on. 1: Power off. (default) LVDS: Outputs Hi-Z CMOS: Outputs Low
0x141	7:5	OUT7 Output Polarity	In CMOS mode,[7:5] select the output polarity of each CMOS output. In LVDS mode, only [5] determines LDVS polarity. **[7:6:5] OUT7(CMOS) OUT7n(CMOS) OUT7(LVDS)** 0 0 0 Non-inverting. Inverting. Non-inverting. 0 1 0 Non-inverting. Non-inverting. Non-inverting (default) 1 0 0 Inverting. Inverting. Non-inverting 1 1 0 Inverting. Non-inverting. Non-inverting 0 0 1 Inverting. Non-inverting. Inverting 0 1 1 Inverting. Inverting. Inverting 1 0 1 Non-inverting. Non-inverting. Inverting 1 1 1 Non-inverting. Inverting. Inverting
	4	OUT7 CMOS B	In CMOS mode, turn on/off the OUT7n output. There is no effect in LDVS mode. 0: turn off the OUT7n output. (default) 1: turn on the OUT7n output..
	3	OUT7 Select LVDS/CMOS	Selects LVDS or CMOS logic levels. 0: LVDS. (default) 1: CMOS.
	2:1	OUT7 LVDS Output Current	Sets output current level in LVDS mode. This has no effect CMOS mode, **[2:1] Current (mA) Recommend Termination (Ω)** 0 0 1.75 100 0 1 3.5 100 (default) 1 0 5.25 50 1 1 7.0 50

Register Address (Hex)	Bit(s)	Name	Description
141	0	OUT7 Power-Down	Power-down output(LVDS/CMOS). 　0: Power on. 　1: Power off. (default)　LVDS: Outputs Hi-Z　CMOS: Outputs Low
0x142	7:5	OUT8 Output Polarity	In CMOS mode,[7:5] select the output polarity of each CMOS output. In LVDS mode, only [5] determines LDVS polarity. **[7:6:5]**　**OUT8(CMOS)**　**OUT8n(CMOS)**　**OUT8(LVDS)** 0 0 0　Non-inverting.　Inverting.　Non-inverting. 0 1 0　Non-inverting.　Non-inverting.　Non-inverting (default) 1 0 0　Inverting.　Inverting.　Non-inverting 1 1 0　Inverting.　Non-inverting.　Non-inverting 0 0 1　Inverting.　Non-inverting.　Inverting 0 1 1　Inverting.　Inverting.　Inverting 1 0 1　Non-inverting.　Non-inverting.　Inverting 1 1 1　Non-inverting.　Inverting.　Inverting
	4	OUT8 CMOS B	In CMOS mode, turn on/off the OUT8n output. There is no effect in LDVS mode. 　0:　turn off the OUT8n output. (default) 　1:　turn on the OUT8n output..
	3	OUT8 Select LVDS/CMOS	Selects LVDS or CMOS logic levels. 　0:　LVDS. 　1:　CMOS.
	2:1	OUT8 LVDS Output Current	Sets output current level in LVDS mode. This has no effect CMOS mode, **[2:1]**　**Current (mA)**　**Recommend Termination (Ω)** 0 0　1.75　100 0 1　3.5　100 (default) 1 0　5.25　50 1 1　7.0　50
	0	OUT8 Power-Down	Power-down output(LVDS/CMOS). 　0: Power on. 　1: Power off. (default)　LVDS: Outputs Hi-Z　CMOS: Outputs Low
0x143	7:5	OUT9 Output Polarity	In CMOS mode,[7:5] select the output polarity of each CMOS output. In LVDS mode, only [5] determines LDVS polarity. **[7:6:5]**　**OUT9(CMOS)**　**OUT9n(CMOS)**　**OUT9(LVDS)** 0 0 0　Non-inverting.　Inverting.　Non-inverting. 0 1 0　Non-inverting.　Non-inverting.　Non-inverting (default) 1 0 0　Inverting.　Inverting.　Non-inverting 1 1 0　Inverting.　Non-inverting.　Non-inverting 0 0 1　Inverting.　Non-inverting.　Inverting 0 1 1　Inverting.　Inverting.　Inverting 1 0 1　Non-inverting.　Non-inverting.　Inverting 1 1 1　Non-inverting.　Inverting.　Inverting
	4	OUT9 CMOS B	In CMOS mode, turn on/off the OUT9n output. There is no effect in LDVS mode. 　0:　turn off the OUT9n output. (default) 　1:　turn on the OUT9n output..
	3	OUT9 Select LVDS/CMOS	Selects LVDS or CMOS logic levels. 　0:　LVDS. (default) 　1:　CMOS.

Register Address (Hex)	Bit(s)	Name	Description
0x143	2:1	OUT9 LVDS Output Current	Sets output current level in LVDS mode. This has no effect CMOS mode, **[2:1]** **Current (mA)** **Recommend Termination (Ω)** 0 0 1.75 100 0 1 3.5 100 (default) 1 0 5.25 50 1 1 7.0 50
	0	OUT9 Power-Down	Power-down output(LVDS/CMOS). 0: Power on. 1: Power off. (default) LVDS: Outputs Hi-Z CMOS: Outputs Low

LVPECL Channel Dividers

Register Address (Hex)	Bit(s)	Name	Description
0x190	7:4	Divider 0 Low Cycles M	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 0. Dx = M+N+2.
	3:0	Divider 0 High Cycles N	Note) The M and N does not affect the duty of LVPECL output. The DCC(Duty Cycle Correction) always works.
0x191	7	Divider 0 Bypass	Bypasses and power-down the divider; route input to divider output. 0: use divider. 1: bypass divider. (default)
	6	Divider 0 Nosync	Nosync. 0: obey chip-level SYNC signal. (default) 1: ignore chip-level SYNC signal.
	5	Divider 0 Force High	Forces divider output to high. This requires that nosync also be set. 0: divider output force to low. (default) 1: divider output force to high.
	4	Divider 0 Start High	Selects clock output to start high or start low. 0: start low. (default) 1: start high.
	3:0	Divider 0 Phase Offset	Phase offset. (default=0x0)
0x193	7:4	Divider 1 Low Cycles M	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 1. Dx = M+N+2.
	3:0	Divider 1 High Cycles N	Note) The M and N does not affect the duty of LVPECL output. The DCC(Duty Cycle Correction) always works.
0x194	7	Divider 1 Bypass	Bypasses and power-down the divider; route input to divider output. 0: use divider. (default) 1: bypass divider.
	6	Divider 1 Nosync	Nosync. 0: obey chip-level SYNC signal. (default) 1: ignore chip-level SYNC signal.
	5	Divider 1 Force High	Forces divider output to high. This requires that nosync also be set. 0: divider output force to low. (default) 1: divider output force to high.

Register Address (Hex)	Bit(s)	Name	Description

0x194	4	Divider 1 Start High	Selects clock output to start high or start low.
			  0: start low. (default)
			  1: start high.

	3:0	Divider 1 Phase Offset	Phase offset. (default=0x0)
0x196	7:4	Divider 2 Low Cycles M	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 2. $Dx = M+N+2$.
	3:0	Divider 2 High Cycles N	Note) The M and N does not affect the duty of LVPECL output. The DCC(Duty Cycle Correction) always works.

0x197	7	Divider 2 Bypass	Bypasses and power-down the divider; route input to divider output.
			  0: use divider. (default)
			  1: bypass divider.

	6	Divider 2 Nosync	Nosync.
			  0: obey chip-level SYNC signal. (default)
			  1: ignore chip-level SYNC signal.

	5	Divider 2 Force High	Forces divider output to high. This requires that nosync also be set.
			  0: divider output force to low. (default)
			  1: divider output force to high.

	4	Divider 2 Start High	Selects clock output to start high or start low.
			  0: start low. (default)
			  1: start high.

	3:0	Divider 2 Phase Offset	Phase offset. (default=0x0)

LVDS/CMOS Channel Dividers

Register Address (Hex)	Bit(s)	Name	Description
0x199	7:4	Divider 3.1 Low Cycles M	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 3.1. Dx = M+N+2.
	3:0	Divider 3.1 High Cycles N	Note) The M and N does not affect the duty of LVDS/CMOS output. The DCC(Duty Cycle Correction) always works.
0x19A	7:4	Divider 3.2 Phase Offset	Refer to LVDS/CMOS channel divider function description.
	3:0	Divider 3.1 Phase Offset	Refer to LVDS/CMOS channel divider function description.
0x19B	7:4	Divider 3.2 Low Cycles	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 3.2. Dx = M+N+2.
	3:0	Divider 3.2 High Cycles	Note) The M and N does not affect the duty of LVDS/CMOS output. The DCC(Duty Cycle Correction) always works.
0x19C	5	Divider 3.2 Bypass	Bypasses (and power-down)3.2 divider logic, route input to 3.2 output. 0: do not bypass. (default) 1: bypass.
	4	Divider 3.1 Bypass	Bypasses (and power-down)3.1 divider logic, route input to 3.2 output. 0: do not bypass. (default) 1: bypass.
	3	Divider 3 Nosync	Nosync. 0: obey chip-level SYNC signal. (default) 1: ignore chip-level SYNC signal.
	2	Divider 3 Force High	Forces divider 3 output to high. Requires that nosync also be set. 0: force low. (default) 1: force high.
	1	Divider 3.2 Start High	Divider3.2 start high or start low. 0: start low. (default) 1: start high.
	0	Divider 3.1 Start High	Divider3.1 strat high or start low. 0: start low. (default) 1: start high.

Register Address (Hex)	Bit(s)	Name	Description
0x19E	7:4	Divider 4.1 Low Cycles M	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 4.1. Dx = M+N+2.
	3:0	Divider 4.1 High Cycles N	Note) The M and N does not affect the duty of LVDS/CMOS output. The DCC(Duty Cycle Correction) always works.
0x19F	7:4	Divider 4.2 Phase Offset	Refer to LVDS/CMOS channel divider function description.
	3:0	Divider 4.1 Phase Offset	Refer to LVDS/CMOS channel divider function description.
0x1A0	7:4	Divider 4.2 Low Cycles	Number of Low clock cycles (M) and High clock cycles (N) of the divider input define a frequency division, Dx, of the Divider 4.2. Dx = M+N+2.
	3:0	Divider 4.2 High Cycles	Note) The M and N does not affect the duty of LVDS/CMOS output. The DCC(Duty Cycle Correction) always works.

0x1A1	5	Divider 4.2 Bypass	Bypasses (and power-down)4.2 divider logic, route input to 4.2 output.
			  0: do not bypass. (default)
			  1: bypass.

	4	Divider 4.1 Bypass	Bypasses (and power-down)4.1 divider logic, route input to 4.2 output.
			  0: do not bypass. (default)
			  1: bypass.

	3	Divider 4 Nosync	Nosync.
			  0: obey chip-level SYNC signal. (default)
			  1: ignore chip-level SYNC signal.

	2	Divider 4 Force High	Forces divider 4 output to high. Requires that nosync also be set.
			  0: force low. (default)
			  1: force high.

	1	Divider 4.2 Start High	Divider4.2 start high or start low.
			  0: start low. (default)
			  1: start high.

	0	Divider 4.1 Start High	Divider4.1 strat high or start low.
			  0: start low. (default)
			  1: start high.

VCO Divider and CLK Input

Register Address (Hex)	Bit(s)	Name	Description
0x1E0	2:0	VCO Divider	**[2:1:0]** **Divide** 0 0 0 2 0 0 1 3 0 1 0 4 (default) 0 1 1 5 1 0 0 6 1 0 1 Output Static 1 1 0 Output Static 1 1 1 Output Static
0x1E1	4	Power-Down Clock Input Section	Powers down the clock input section (including CLK buffer, VCO dividers and CLK tree). 0 : normal operation (default). 1 : Power-down.
	3	Power-Down VCO clock interface	Powers down the interface block between VCO and clock distribution. 0 : normal operation (default). 1 : power-down.
	2	Power-Down VCO and CLK	Powers down both VCO and CLK input. 0 : normal operation (default). 1 : power-down.
	1	Select VCO or CLK	Powers down the clock input section (including CLK buffer, VCO dividers and CLK tree). 0 : Selects external CLK as input to VCO divider (default). 1 : Selects VCO as input to VCO divider; cannot bypass VCO divider when this is selected.
	0	Bypass VCO divider	Bypasses or uses the VCO divider. 0 : Uses VCO divider (default). 1 : Bypasses VCO divider; cannnot select VCO as input when this is selected.

System

Register Address (Hex)	Bit(s)	Name	Description
0x230	2	Power-Down SYNC	Powers down the SYNC function. 0: normal operation of SYNC function (default). 1: Power-down SYNC circuitry.
	1	Power down distribution reference	Powers down the output buffers. 0 : normal operation (default). 1 : power down the output buffers. Buffers output as follows in power down. LVPECL: Hi-Z (same state with 0xFn[1:0]=01 or 10b, n=0 to 5) LVDS: Hi-Z CMOS: Low
	0	Soft SYNC	The soft SYNC works the same as the $\overline{\text{SYNC}}$ pin. Expect that the polarity of the bit is reversed. That is, a high level forces selected channels into a predetermined static state, and 1-to-0 transition triggers a SYNC. 0: same as $\overline{\text{SYNC}}$ high (default). 1: same as $\overline{\text{SYNC}}$ low.

Update All Registers

Register Address (Hex)	Bit(s)	Name	Description
0x232	0	Update All Registers	This bit must be set to 1 to transfer the contents of the buffer registers into the active registers. This happens on the next SCLK rising edge. This bit is self-cleaning; that is, it does not have to be set back to 0. 1: (self-cleaning); update all active registers to the contents of the buffer registers.

PACKAGE INFORMATION

Mechanical data
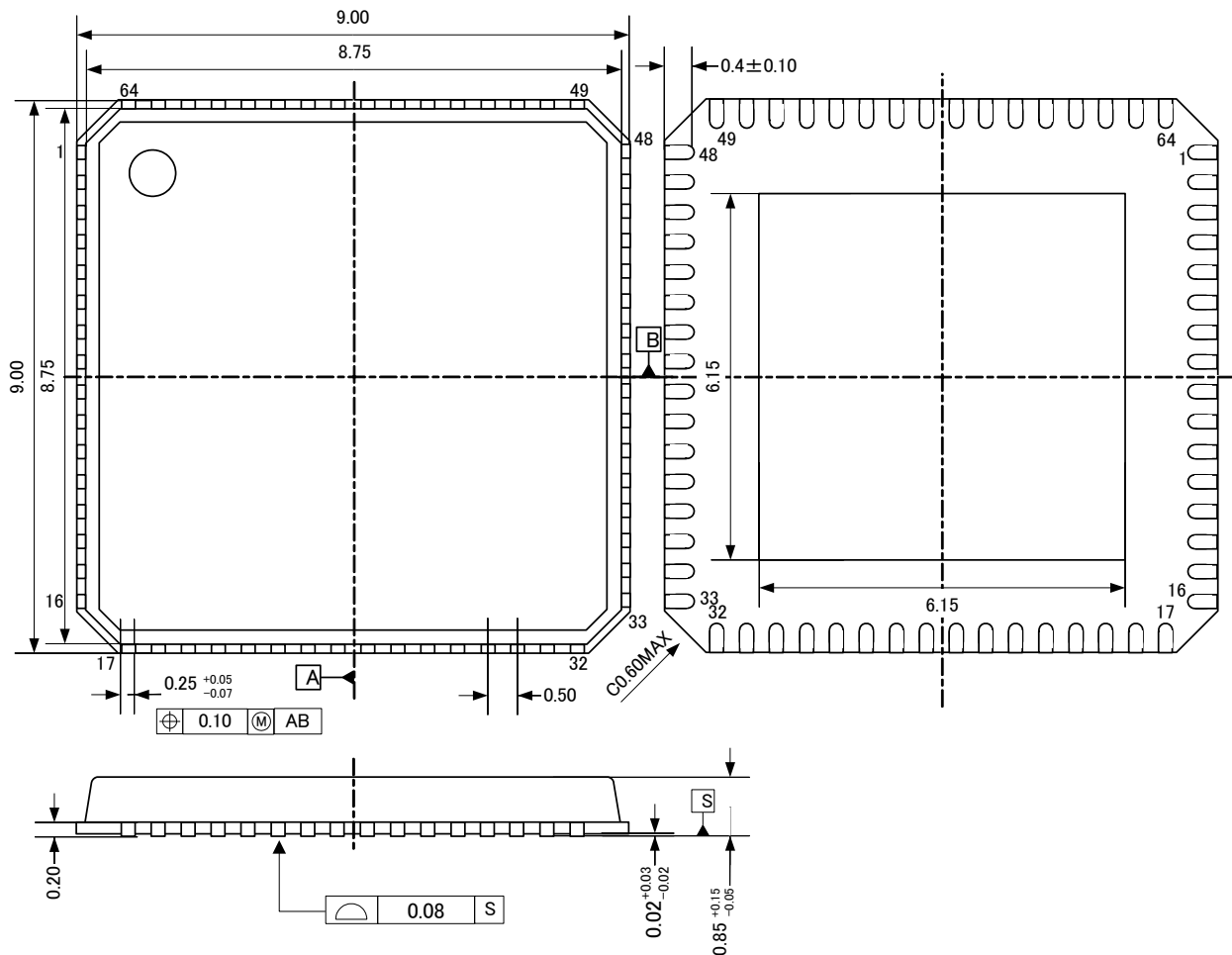
Marking

a: #1 Pin Index

b: Part number

c: Date code
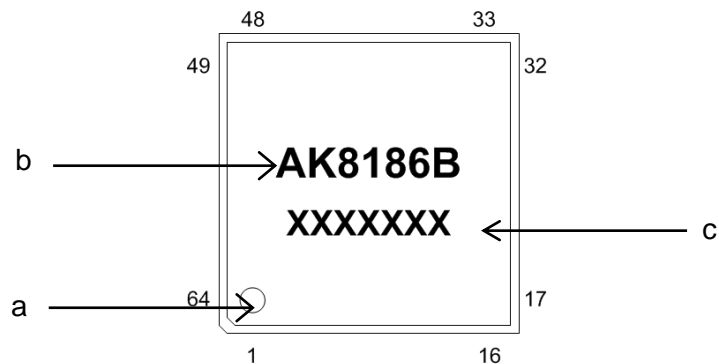
RoHS Compliance
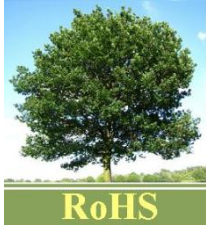
All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in "lead-free" packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

REVISION HISTORY

31/August/2012   Draft-E00 to E01
P.3   Adds Table of contents.
P.8   Change to On chip VCO.
P.9   Change to Input Capacitance.
P.25   Change to Prescaler division in FD and DM mode.
P.27   Change to p-channel open drain in Figure17.
P.49   Change to Lock Detect Counter.

28/September/2012   Draft-E01 to E02
P.12-15   Change to Table 8,9,10,12 and 13.