

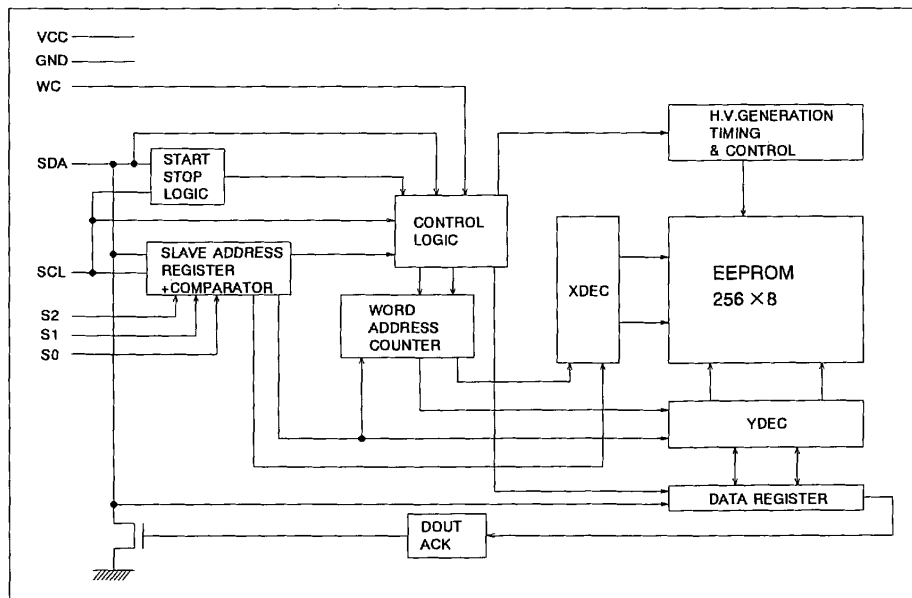


# AK6003A

## Software Write Protect I<sup>2</sup>C bus 2Kbit EEPROM

Features

- ADVANCED CMOS EEPROM TECHNOLOGY
- READ/WRITE NON-VOLATILE MEMORY
- WIDE VCC OPERATION ... V<sub>cc</sub> = 1.8V ~ 5.5V
- 2048 bits, 256×8 organization
- I<sup>2</sup>C™ SERIAL INTERFACE
- LOW POWER CONSUMPTION
  - 0.8μA Max. Standby
- HIGH RELIABILITY
  - Endurance : 100K cycles
  - Data Retention : 10 years
- 16 byte page write mode
- Software Write Protection (lower 128 bytes)  
Hardware Write Protection (entire array)
- Automatic write cycle time-out with auto-ERASE
- IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package (TSSOP)



Block Diagram

I<sup>2</sup>C™ is a registered trademark of Philips Corporation.

<b>General Description</b>
----------------------------

The AK6003A is a 2048-bit serial CMOS E<sup>2</sup>PROM divided into 256 registers of 8 bits each. The AK6003A can operate full function under wide operating voltage range from 1.8V to 5.5V. The charge up circuit is integrated for high voltage generation that is used for write operation.

The AK6003A conforms to all specifications in the 2 wire protocol and is controlled by serial clock (SK) and serial data (SDA) line.

Some devices can be connected to the same bus. Each device connected to the bus is software addressable by a unique address, and can operate as either a transmitter or receiver. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table1). The master is the device which initiates a data transfers on the bus and generates the clock signals to permit that transfer. At that time, the device addressed is considered as the slave.

TERM	DESCRIPTION
Transmitter	The device which sends the data to the bus
Receiver	The device which receives the data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master

Table 1. Definitions

**■ Write protection**

• Hardware Write Protection

If  $\overline{WC}$  pin is High level, WRITE operations onto the entire array will not be executed. If the  $\overline{WC}$  pin is Low level, the AK6003A will be enabled to perform WRITE operation.

As the  $\overline{WC}$  pin is internally pulled down to GND, the AK6003A will be enabled to perform WRITE operation if the  $\overline{WC}$  pin is left floating.

• Software Write Protection

The software write protect register is programmed by sending a software write protect command and the software write protection is enabled.

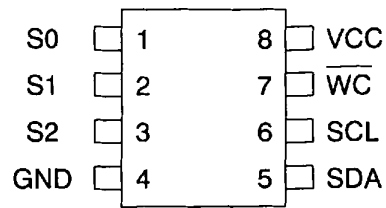
If the software write protection is enabled, Write operations onto the lower half of the array(\$00~\$7F) will not be executed permanently. Once the software write protect register has been programmed, the write protection can not be reversed. The software write protection can not be reversed even if the AK6003A is powered down.

If the  $\overline{WC}$  pin is high level, WRITE operations onto the entire array will not be executed regardless of the status of the software protection.

**■ Type of Products**

Model	Memory size	Temp.Range	Vcc	Package
AK6003AV	2Kbits	-40°C~85°C	1.8V~5.5V	8pin Plastic TSSOP

■ Pin arrangement



Pin Name	Function
S0,S1,S2	Device Address Inputs
SCL	Clock Input
SDA	Data Input / Output
$\overline{WC}$	Write Control
Vcc	Power Supply
GND	Ground

**■ DATA TRANSFER**

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK6003A recognizes the START condition, the devices interfaced to the bus wait for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the device, the designated slave pulls the SDA line to LOW (ACKNOWLEDGE) . The data transfer is always terminated by a STOP condition generated by the master.

[ Data validity ]

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

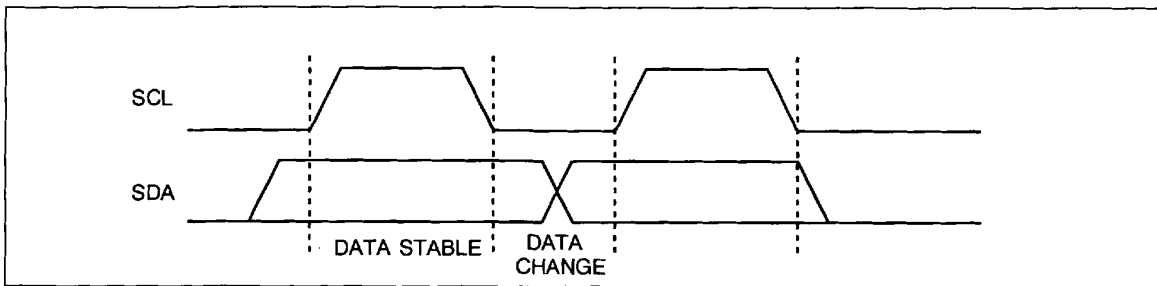


Figure1. Data transfer

[ START and STOP condition]

A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. All commands are preceded by the START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All communications are terminated by the STOP condition. After a read sequence, the STOP condition will place the EEPROM in a standby power mode.

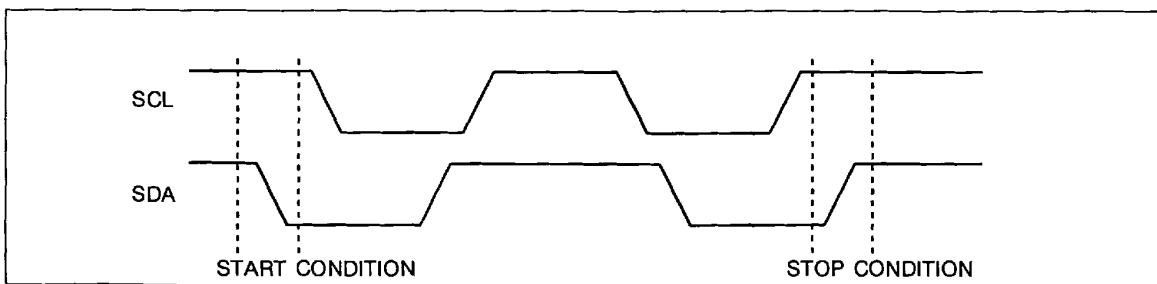


Figure2. Start and STOP Definition

[ACKNOWLEDGE]

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the next clock (ninth clock), the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data.

The AK6003A will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the AK6003A will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the AK6003A slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition to return to the standby power mode.

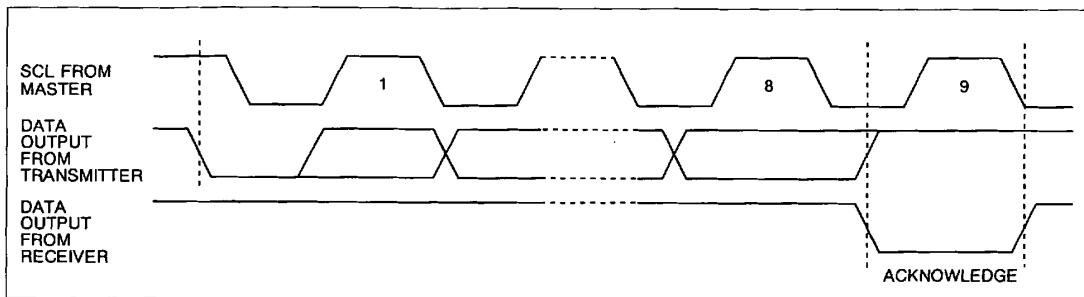


Figure3. Acknowledge Response from Receiver

[SLAVE ADDRESS]

After the START condition, a SLAVE ADDRESS is sent. If the transmitted slave address matches an address of one of the device, the designated slave pulls the SDA line to LOW .

The most significant four bits of the slave address are "1010" or "0110". The next three bits are S0, S1 and S2 device address bits. These three bits identify the specific device on the bus. They is set by the hard wired input pins (S0 pin, S1 pin and S2 pin). Therefore a total of eight devices can be connected to the same bus.

The last bit of the slave address ( $R/\bar{W}$  bit) defines whether a write or read condition is requested by the master. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

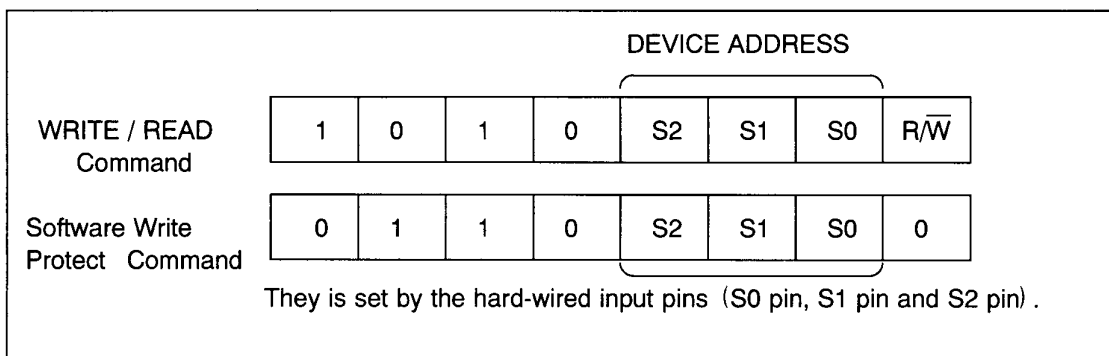


Figure4. Slave Address

<b>Pin Descriptions</b>
-------------------------

**SCL**(Serial Clock)

The SCL input is used to clock all data into and out of the device.

**SDA**(Serial Data)

The SDA is a bidirectional pin used to transfer data into and out of the device.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

**S0, S1, S2**(Device Address)

The S0, S1 and S2 are device address inputs that are used to set three bits of the slave address. A total of eight devices can be connected to the same bus.

 $\overline{WC}$  (Write Control)

If the  $\overline{WC}$  is High level, WRITE operations will not be executed. If the  $\overline{WC}$  is Low level, the AK6003A will be enabled to perform WRITE operation.

As the  $\overline{WC}$  is internally pulled down to GND, the AK6003A will be enabled to perform WRITE operation if the  $\overline{WC}$  is left floating.

$\overline{WC}$  must not change from the start condition input to the stop condition input.

**VCC**(Power Supply)**GND**(Ground)

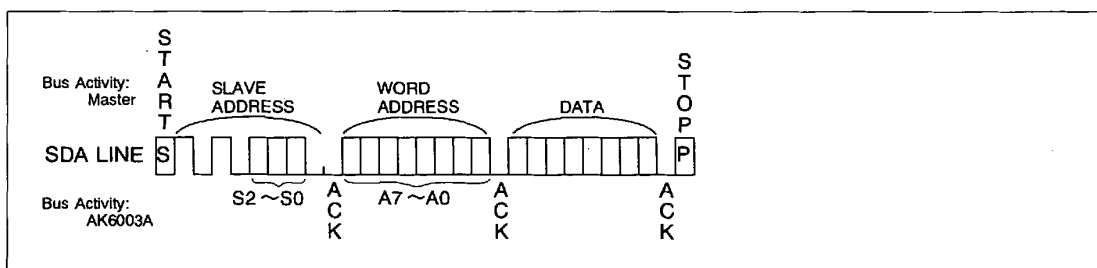
Functional Descriptions

■ **WRITE Operations**

**BYTE WRITE**

A write operation requires a word address following the slave address word ( $R/\overline{W}=0$ ) and acknowledge. The word address is comprised of eight bits and provides access to any one of the 256 words. Upon receipt of the word address the AK6003A responds with an acknowledge, and awaits the next eight bits of data, again, responding with an acknowledge.

The master then terminates the transfer by generating a stop condition, at which time the AK6003A begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the AK6003A inputs are disable, and the device will not respond to any requests from the master.



BYTE WRITE

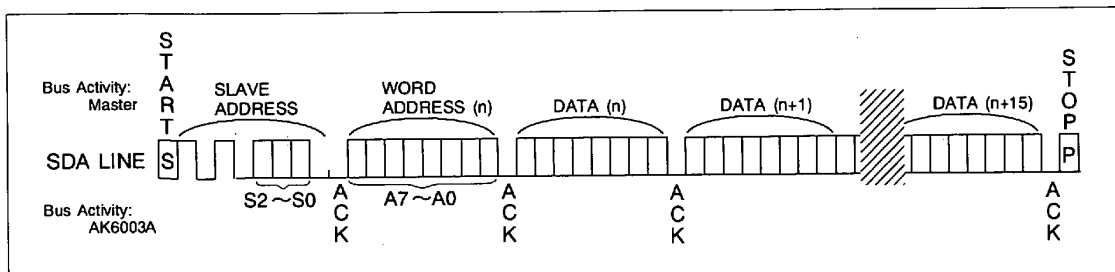
**PAGE WRITE**

The AK6003A is capable of a sixteen byte page write operation.

It is initiated in the same manner as the byte write operation. But instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the AK6003A will respond with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the AK6003A begins the internal write cycle to the nonvolatile memory.

After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. When the highest address is reached (XXXX 1111), the address counter rolls over to address "XXXX 0000" allowing the read cycle to be continued indefinitely.

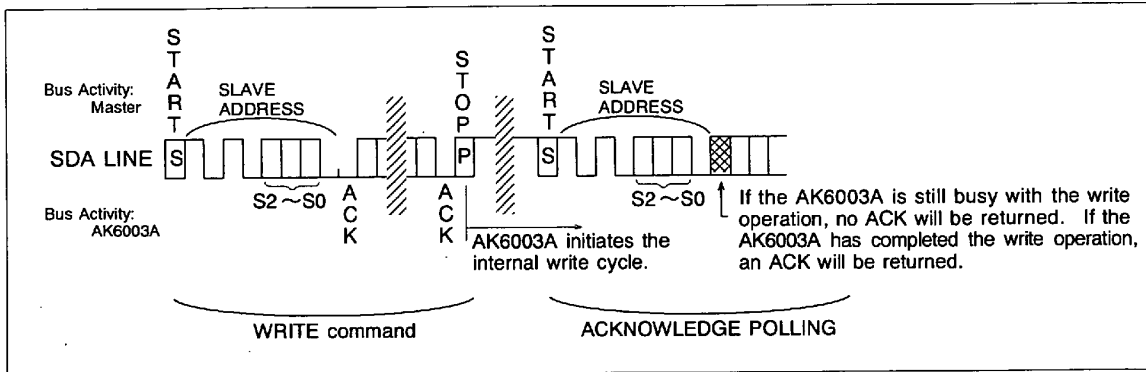
If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. When the master transmit eighteen words prior to the stop condition, seventeenth word will be overwritten to first word, and eighteenth word will be overwritten to second word.



PAGE WRITE

**ACKNOWLEDGE POLLING**

Since the device will not acknowledge during the internal write cycle, this can be used to determine when the cycle is complete. This feature (ACK polling) can be used to maximize bus throughput. Once the stop condition is issued to indicate the end of the host's write operation the AK6003A initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the AK6003A is still busy with the write operation no ACK will be returned. If the AK6003A has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation. When the write operation is executed after the ACK polling, the host can issue the byte address consecutively after the ACK is returned. When the read operation is executed after the ACK polling, the host should issue the stop condition once.



**ACKNOWLEDGE POLLING**



■ **Software Write Protect Operation**

The AK6003A has a software write protect feature. The software write protect register is programmed by sending the software write protect command and the write protection is enabled. If the software write protection is enabled, Write operations onto the lower half of the array(\$00~\$7F) will not be executed permanently.

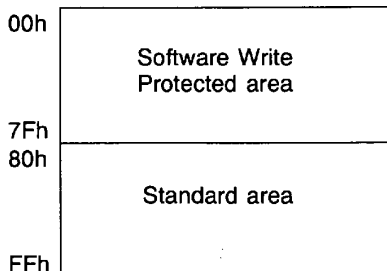
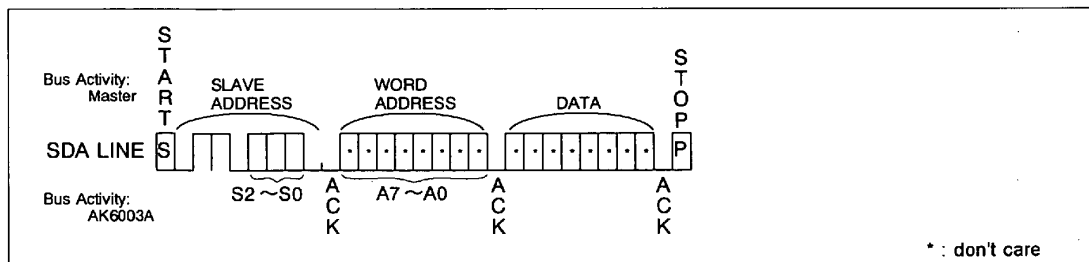


Figure5. EEPROM composition

The software write protect operation requires the word address following the slave address word ( $R/\bar{W}=0$ ) and acknowledge. The most significant four bits of the slave address are "0110". Upon receipt of the word address the AK6003A responds with an acknowledge and awaits for the next eight bits of data, again, responding with an acknowledge. The word address bits and the next eight bits of data are don't cares. After the receipt of the slave address set to "0110" and  $R/\bar{W}=1$ , the AK6003A will not respond with an acknowledge.

The master then terminates the transfer by generating a stop condition, at which time the AK6003A begins to program the software write protect register. While the programming is in progress the AK6003A inputs are disable, and the device will not respond to any requests from the master. Once the software write protect register has been programmed, the write protection can not be reversed. The software write protection can not be reversed even if the AK6003A is powered down. Once the software write protect register has been programmed, the software write protect command is ignored.



SOFTWARE WRITE PROTECT

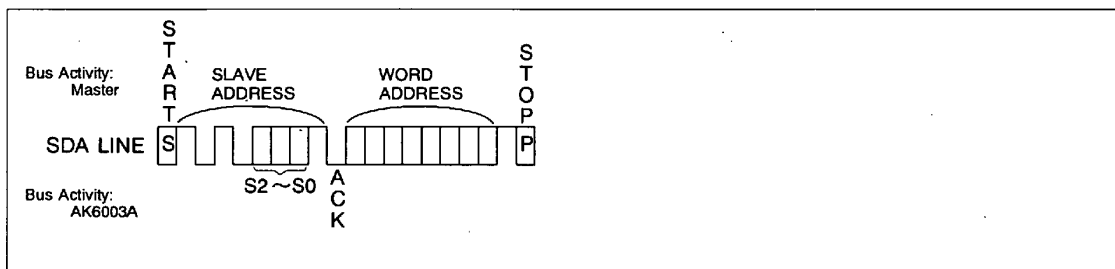
**■ READ Operations**

There are three basic read operations: current address read, random read, and sequential read. Read operations are initiated in the same manner as write operations, with the exception that the  $\overline{R/W}$  bit of the slave address is set to a one.

It is noted that the ninth clock cycle of the read operation is not a "don't care". To terminate a read operation, the master must hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

**CURRENT ADDRESS READ**

Internally the AK6003A contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n+1$ . Upon receipt of the slave address with  $\overline{R/W}$  set to one, the AK6003A issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but generate a stop condition, and therefore the AK6003A discontinues transmission.

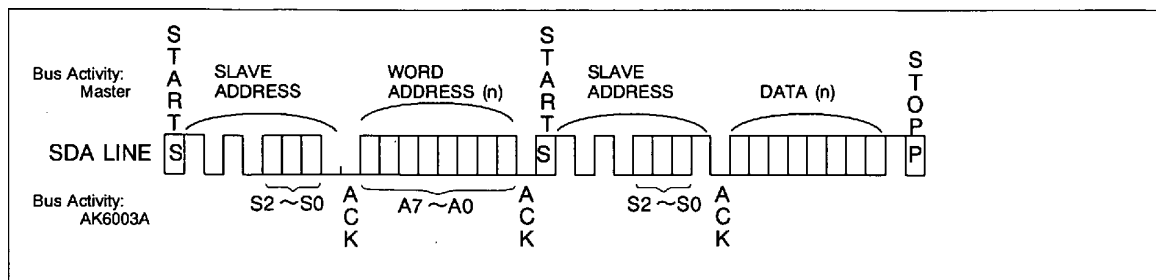


CURRENT ADDRESS READ

**RANDOM READ**

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the  $\overline{R/W}$  bit set to one, the master must first perform a "dummy" write operation.

The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the  $\overline{R/W}$  bit set to one. This will be followed by an acknowledge from the AK6003A and then by the eight bit word. The master will not acknowledge the transfer but generate the stop condition, and therefore the AK6003A discontinues transmission.

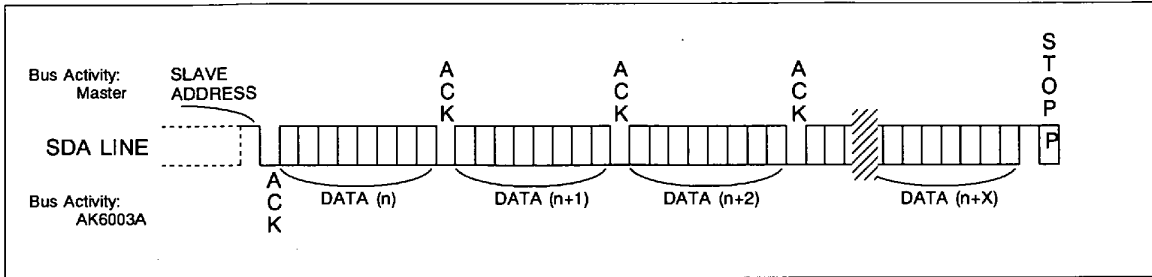


RANDOM READ

**SEQUENTIAL READ**

Sequential read can be initiated as either a current address read or random read. The first word is transmitted in the same manner as the other read modes. However the master responds with an acknowledge, indicating it requires additional data. The AK6003A continues to output data for each acknowledge received. The data output is sequential, with the data from address n followed by the data from n+1. The master will not acknowledge the transfer but generate the stop condition, and therefore the AK6003A discontinues transmission.

When the highest address is reached (\$FF), the address counter rolls over to address \$00 allowing the read cycle to be continued indefinitely.



SEQUENTIAL READ

<b>Absolute Maximum Ratings</b>
---------------------------------

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+7.0	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

<b>Recommended Operating Condition</b>
--

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	1.8	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

**Electrical Characteristics**

(1)DC Electrical Characteristics

(-40°C ≤ Ta ≤ 85°C, 1.8V ≤ VCC ≤ 5.5V unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V,fSCL=400KHz		3.0	mA
	ICC2	VCC=2.5V,fSCL=100KHz		2.4	mA
	ICC3	VCC=1.8V,fSCL=100KHz		1.5	mA
Current Dissipation (READ)	ICC4	VCC=5.5V,fSCL=400KHz		500	uA
	ICC5	VCC=2.5V,fSCL=100KHz		200	uA
	ICC6	VCC=1.8V,fSCL=100KHz		100	uA
Current Dissipation (Standby)	ICCS	VCC=5.5V, *1		0.8	uA
Input High Voltage	VIH1	2.5V ≤ VCC ≤ 5.5V	0.7×VCC	VCC+0.5	V
	VIH2	1.8V ≤ VCC < 2.5V	0.8×VCC	VCC+0.5	V
Input Low Voltage	VIL1	2.5V ≤ VCC ≤ 5.5V	-0.3	0.3×VCC	V
	VIL2	1.8V ≤ VCC < 2.5V	-0.3	0.2×VCC	V
Output Low Voltage	VOL1	2.5V ≤ VCC ≤ 5.5V IOL=4.5mA		0.4	V
	VOL2	1.8V ≤ VCC < 2.5V IOL=3.0mA		0.4	V
Hysteresis of Schmitt trigger inputs (SCL, SDA) *2	VHYS		0.05×VCC		V
Input Leakage Current *3	ILI	VCC=5.5V,VIN=VCC/GND		±1.0	uA
Output Leakage Current	ILO	VCC=5.5V, VOUT=VCC/GND		±1.0	uA

\*1:VIN=VCC / GND, WC=GND

\*2:The parameter is periodically sampled and not 100% tested.

\*3:SCL,SDA,S0,S1,S2

(2)Capacitance

(Ta=25°C,f=1MHz,VCC=5.0V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input/Output Capacitance (SDA)	CI/O	VI/O=0V		8.0	pF
Input Capacitance (SCL)	CIN	VIN=0V		6.0	pF

(note) The parameter is periodically sampled and not 100% tested.

## (3)AC Electrical Characteristics-1

(-40°C ≤ Ta ≤ 85°C, 1.8V ≤ VCC ≤ 5.5V unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
SCL Clock Frequency	fSCL			100	KHz
Noise Suppression Time Constant at SCL, SDA *5	tl			100	ns
SCL Low to SDA Data Out Valid : SDA	tAA1	4.5V ≤ VCC ≤ 5.5V	0.2	3.5	us
	tAA2	2.5V ≤ VCC < 4.5V	0.3	3.5	us
	tAA3	1.8V ≤ VCC < 2.5V	0.3	4.5	us
Time the Bus Must be Free before a New Transmission can start	tBUF		4.7		us
Start Condition Hold Time	tHD:STA		4.0		us
Clock Low Period	tLOW		4.7		us
Clock High Period	tHIGH		4.0		us
Start Condition Setup Time	tSU:STA		4.7		us
Data in Hold Time	tHD:DAT		0		us
Data in Setup Time	tSU:DAT		250		ns
SDA and SCL Rise Time *5	tR			1.0	us
SDA and SCL Fall Time *5	tF			0.3	us
Stop Condition Setup Time	tSU:STO		4.0		us
Data Out Hold Time	tDH		100		ns
Write Cycle Time *4	tWR			10	ms

\*4: The write cycle time (tWR) is the time from a valid stop condition of a write sequence to the end of the internal program cycle.

Since the device will not acknowledge during the internal program cycle, this can be used to determine when the cycle is complete. This feature (ACK polling) can be used to maximize bus throughput.

\*5: The parameter is periodically sampled and not 100% tested.

(4)AC Electrical Characteristics-2

(-40°C ≤ Ta ≤ 85°C, 4.5V ≤ VCC ≤ 5.5V unless otherwise specified)

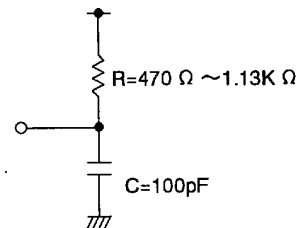
Parameter	Symbol	Condition	Min.	Max.	Unit
SCL Clock Frequency	fSCL			400	KHz
Noise Suppression Time Constant at SCL, SDA *7	tl			50	ns
SCL Low to SDA Data Out Valid : SDA	tAA		0.2	0.9	us
Time the Bus Must be Free before a New Transmission can start	tBUF		1.3		us
Start Condition Hold Time	tHD:STA		0.6		us
Clock Low Period	tLOW		1.3		us
Clock High Period	tHIG		0.6		us
Start Condition Setup Time	tSU:STA		0.6		us
Data in Hold Time	tHD:DAT		0		us
Data in Setup Time	tSU:DAT		100		ns
SDA and SCL Rise Time *7	tR			0.3	us
SDA and SCL Fall Time *7	tF			0.3	us
Stop Condition Setup Time	tSU:STO		0.6		us
Data Out Hold Time	tDH		50		ns
Write Cycle Time *6	tWR			10	ms

\*6: The write cycle time (tWR) is the time from a valid stop condition of a write sequence to the end of the internal program cycle.  
 Since the device will not acknowledge during the internal program cycle, this can be used to determine when the cycle is complete. This feature (ACK polling) can be used to maximize bus throughput.

\*7: The parameter is periodically sampled and not 100% tested.

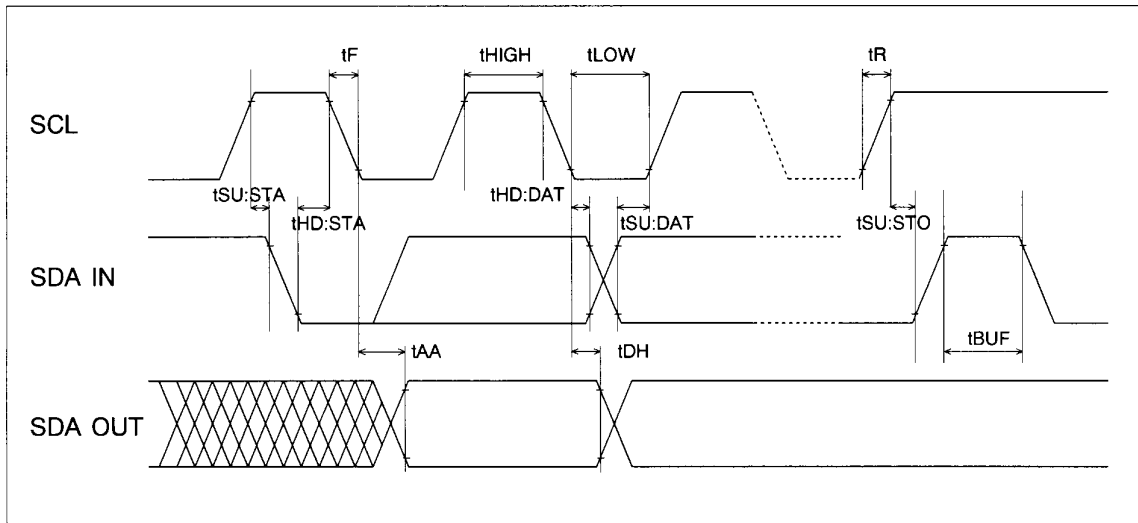
■ AC Conditions of Test

Input Pulse Levels	0.1×VCC~0.9×VCC
Input Rise and Fall Times	10ns
Output Timing Level	0.5×VCC

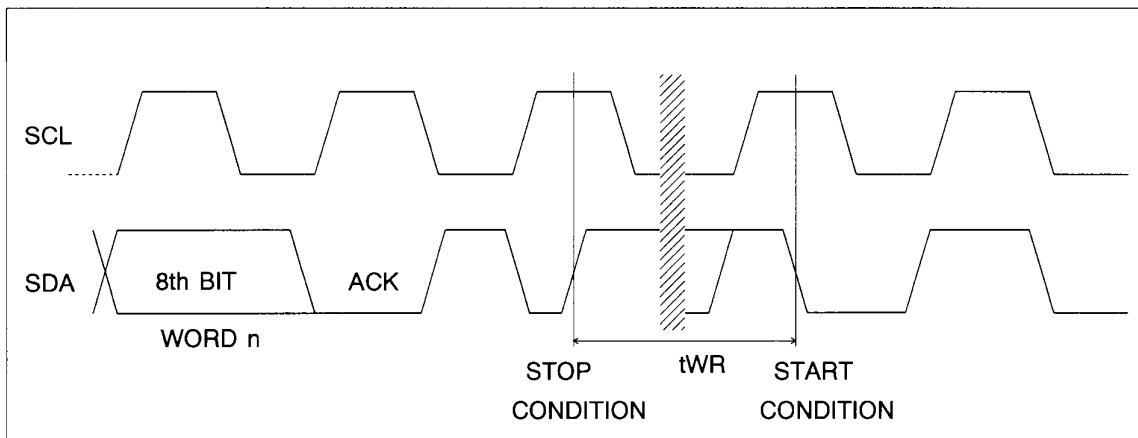


Equivalent AC Load Circuit

**Synchronous Data Timing**



BUS TIMING



WRITE CYCLE TIMING



## IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  - (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  - (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.