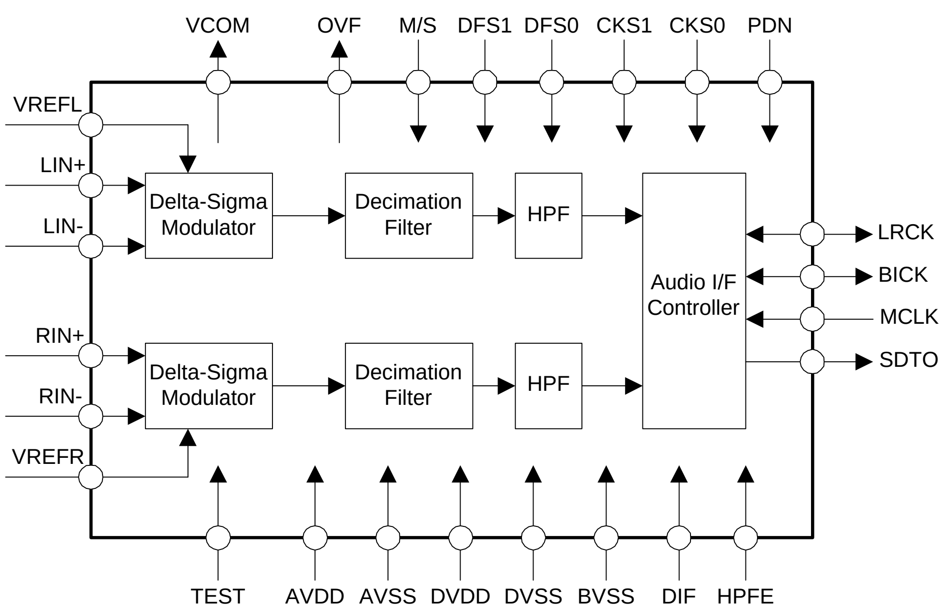
AK5385A
24Bit 192kHz ΔΣ ADC

GENERAL DESCRIPTION

The AK5385A is a 24bit, 192kHz sampling 2ch A/D converter for high-end audio system. The modulator in the AK5385A uses the Enhanced Dual Bit architecture and the AK5385A realizes high accuracy and low cost. The AK5385A performs 114dB dynamic range, so the device is suitable for AV-amp, AV recorder and musical instruments. The AK5385A is available in 28pin VSOP and SOP package, utilizing less board space.

FEATURES

- **Sampling Rate: 8kHz ~ 216kHz**
- **Full Differential Inputs**
- **S/(N+D): 103dB**
- **DR: 114dB**
- **S/N: 114dB**
- **High Performance Linear Phase Digital Anti-Alias filter**
  - **Passband: 0~21.768kHz (@fs=48kHz)**
  - **Ripple: 0.005dB**
  - **Stopband: 100dB**
- **Digital HPF**
- **Power Supply: 5V ± 5%(Analog), 3.0 ~ 5.25V(Digital)**
- **Power Dissipation: 183mW (@fs=48kHz)**
- **Package: 28pin SOP / 28pin VSOP**
- **AK5383/AK5393/AK5394A Semi-Pin compatible**

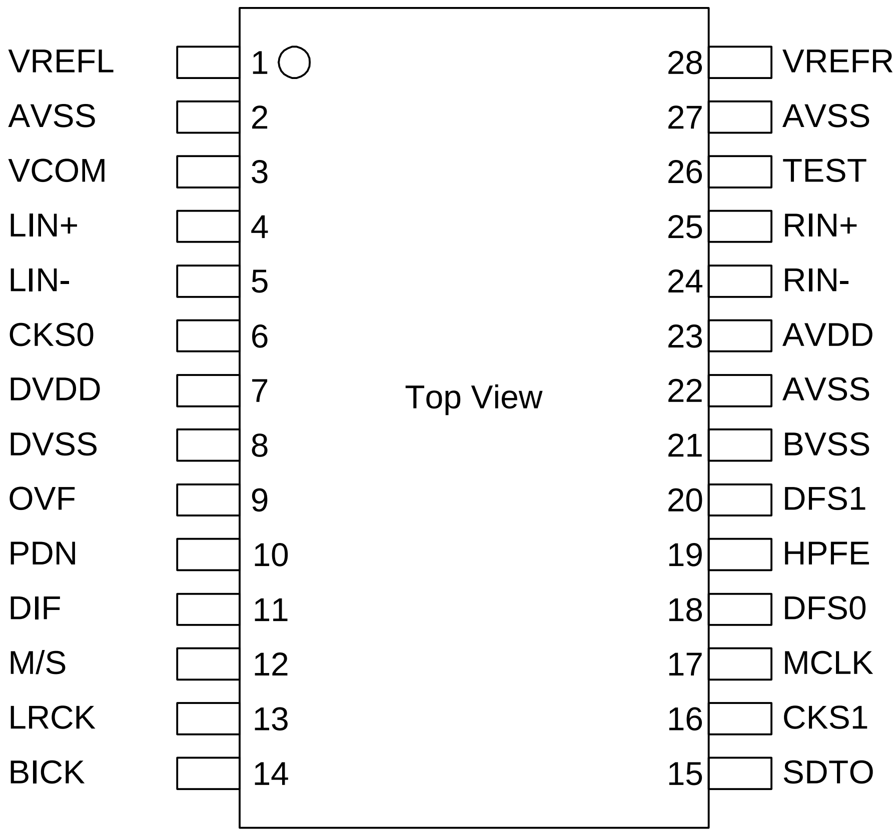


Block diagram

■ Ordering Guide

AK5385AVS	–10 ~ +70°C	28pin SOP (1.27mm pitch)
AK5385AVF	–40 ~ +85°C	28pin VSOP (0.65mm pitch)
AKD5385A	Evaluation Board for AK5385A	

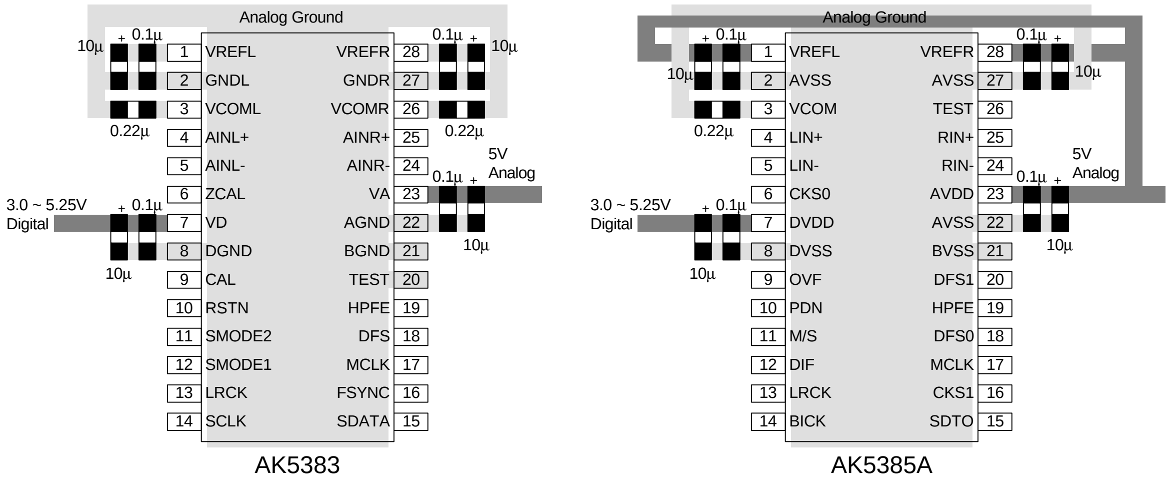
■ Pin Layout



■ Compatibility with AK5383/AK5394A

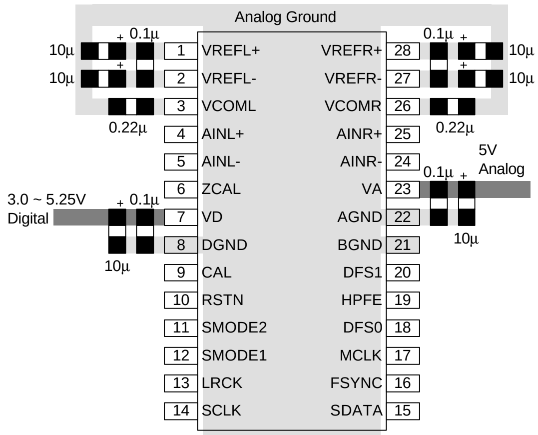
	AK5385A	AK5383	AK5394A
Pin 1	VREFL	VREFL	VREFL+
Pin 2	AVSS	GNDL	VREFL–
Pin 3	VCOM	VCOML	VCOML
Pin 6	CKS0	ZCAL	ZCAL
Pin 9	OVF	CAL	CAL
Pin 11	DIF	SMODE2	SMODE2
Pin 12	M/S	SMODE1	SMODE1
Pin 16	CKS1	FSYNC	FSYNC
Pin 18	DFS0	DFS	DFS0
Pin 20	DFS1	TEST	DFS1
Pin 26	TEST	VCOMR	VCOMR
Pin 27	AVSS	GNDR	VREFR–
Pin 28	VREFR	VREFR	VREFR+
fs	8kHz ~ 216kHz	1kHz ~ 108kHz	1kHz ~ 216kHz
MCLK at 48kHz	256/384/512fs	256fs	256fs
MCLK at 96kHz	256fs	128fs	128fs
MCLK at 192kHz	128fs	Not Available	64fs
DR, S/N	114dB	110dB	123dB
Input Voltage	±2.9Vpp	±2.45Vpp	±2.4Vpp
Offset Calibration	Not Available	Available	Available

■ Compare PCB layout example between AK5385A and AK5383

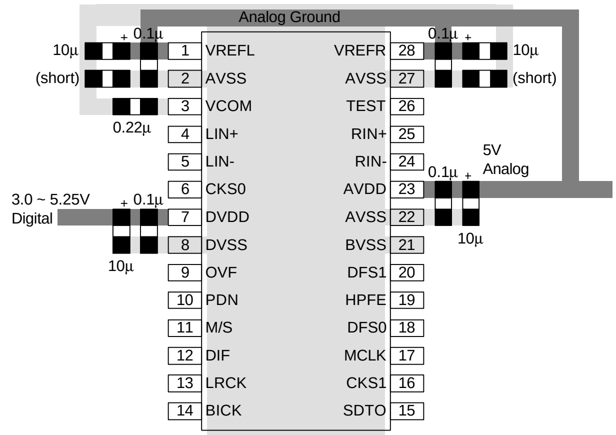


Pin #	AK5383	AK5385A
1	VREFL	VREFL
	Lch Voltage Reference **Output** Pin, 3.75V Normally, connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.	Lch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
6	ZCAL	CKS0
	Zero Calibration Control Pin This pin controls the calibration reference signal.	Master Clock Select 0 Pin (Internal Pull-down Pin, typ. 100kΩ)
9	CAL	OVF
	Calibration Active Signal Pin	Analog Input Overflow Detect Pin
11	SMODE2	DIF
	Serial Interface Mode Select Pin	Audio Interface Format Pin
12	SMODE1	M/S
	Serial Interface Mode Select Pin	Master / Slave Mode Pin
16	FSYNC	CKS1
	Frame Synchronization Signal Pin	Master Clock Select 1 Pin (Internal Pull-down Pin, typ.100kΩ)
18	DFS	DFS0
	Double Speed Sampling Mode Pin	Sampling Speed Select 0 Pin
20	TEST	DFS1
	Test Pin (Internal Pull-down Pin)	Sampling Speed Select 1 Pin
26	VCOMR	TEST
	Rch Common Voltage Pin, 2.75V	Test Pin (Internal Pull-down Pin, typ. 100kΩ)
28	VREFR	VREFR
	Rch Voltage Reference **Output** Pin, 3.75V Normally, connected to GNDL with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.	Rch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.

■ Compare PCB layout example between AK5385A and AK5394A



AK5394A



AK5385A

Pin #	AK5394A	AK5385A
1	VREFL+	VREFL
	Lch Positive Voltage Reference **Output** Pin, 3.75V Normally connected to AGND with a large electrolytic capacitor and connected to VREFL– with a 0.22µF ceramic capacitor.	Lch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.
2	VREFL–	AVSS
	Lch Negative Voltage Reference **Output** Pin, 1.25V Normally connected to AGND with a large electrolytic capacitor and connected to VREFL+ with a 0.22µF ceramic capacitor.	Analog Ground Pin
6	ZCAL	CKS0
	Zero Calibration Control Pin This pin controls the calibration reference signal.	Master Clock Select 0 Pin (Internal Pull-down Pin, typ. 100kΩ)
9	CAL	OVF
	Calibration Active Signal Pin	Analog Input Overflow Detect Pin
11	SMODE2	DIF
	Serial Interface Mode Select Pin	Audio Interface Format Pin
12	SMODE1	M/S
	Serial Interface Mode Select Pin	Master / Slave Mode Pin
16	FSYNC	CKS1
	Frame Synchronization Signal Pin	Master Clock Select 1 Pin (Internal Pull-down Pin, typ. 100kΩ)
27	VREFR–	AVSS
	Rch Negative Voltage Reference **Output** Pin, 1.25V Normally connected to AGND with a large electrolytic capacitor and connected to VREFR+ with a 0.22µF ceramic capacitor.	Analog Ground Pin
26	VCOMR	TEST
	Rch Common Voltage Pin, 2.75V	Test Pin (Internal Pull-down Pin, typ. 100kΩ)
28	VREFR+	VREFR
	Rch Positive Reference **Output** Voltage, 3.75V Normally connected to AGND with a large electrolytic capacitor and connected to VREFR– with a 0.22µF ceramic capacitor.	Rch Voltage Reference **Input** Pin, AVDD Normally, connected to AVSS with a 10µF electrolytic capacitor and a 0.1µF ceramic capacitor.

PIN / FUNCTION

No.	Pin Name	I/O	Function
1	VREFL	I	Lch Voltage Reference Input Pin, AVDD Normally, connected to AVSS with a 10μF electrolytic capacitor and a 0.1μF ceramic capacitor.
2	AVSS	-	Analog Ground Pin
3	VCOM	O	Common Voltage Output Pin, AVDD/2
4	LIN+	I	Lch Analog Positive Input Pin
5	LIN–	I	Lch Analog Negative Input Pin
6	CKS0	I	Master Clock Select 0 Pin (Internal Pull-down Pin, typ. 100kΩ)
7	DVDD	-	Digital Power Supply Pin, 3.0 ~ 5.25V
8	DVSS	-	Digital Ground Pin
9	OVF	O	Analog Input Overflow Detect Pin This pin goes to “H” if analog input overflows.
10	PDN	I	Power Down Mode Pin “H”: Power up, “L”: Power down
11	DIF	I	Audio Interface Format Pin “H” : 24bit I^2S Compatible, “L” : 24bit MSB justified
12	M/S	I	Master / Slave Mode Pin “H” : Master Mode, “L” : Slave Mode
13	LRCK	I/O	Output Channel Clock Pin “L” Output in Master Mode at Power-down mode.
14	BICK	I/O	Audio Serial Data Clock Pin “L” Output in Master Mode at Power-down mode.
15	SDTO	O	Audio Serial Data Output Pin “L” Output at Power-down mode.
16	CKS1	I	Master Clock Select 1 Pin (Internal Pull-down Pin, typ. 100kΩ)
17	MCLK	I	Master Clock Input Pin
18	DFS0	I	Sampling Speed Select 0 Pin
19	HPFE	I	High Pass Filter Enable Pin “H” : Enable, “L” : Disable
20	DFS1	I	Sampling Speed Select 1 Pin
21	BVSS	-	Substrate Ground Pin
22	AVSS	-	Analog Ground Pin
23	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
24	RIN–	I	Rch Analog Negative Input Pin
25	RIN+	I	Rch Analog Positive Input Pin
26	TEST	I	Test Pin (Internal Pull-down Pin, typ. 100kΩ)
27	AVSS	-	Analog Ground Pin
28	VREFR	I	Rch Voltage Reference Input Pin, AVDD Normally, connected to AVSS with a 10μF electrolytic capacitor and a 0.1μF ceramic capacitor.

Note: All digital input pins except pull-down pins should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN+, LIN–	These pins should be connected to AVSS.
	RIN+, RIN–	These pins should be connected to AVSS.
	VREFL, VREFR	These pins should be connected to AVDD.
Digital	OVF	This pin should be open.
	TEST	This pin should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, BVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	|BVSS – DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (LIN+/–, RIN+/–, VREFL/R pins)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (All digital input pins)		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (Power applied)	28SOP Package	Ta	–10	70	°C
	28VSOP Package	Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS BVSS, and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, BVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Digital	DVDD	3.0	3.3	AVDD	V
Voltage Reference (VREFL/R pins)		VREF	3.0	-	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=5.0V, DVDD=3.3V; AVSS=BVSS=DVSS=0V; VREFL=VREFR=AVDD; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz, 40Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Analog Input Characteristics:						
Resolution					24	Bits
Input Voltage (Note 4)			±2.7	±2.9	±3.1	Vpp
S/(N+D)	fs=48kHz BW=20kHz	−1dBFS (Note 5)	-	103		dB
		−1dBFS	92	100		dB
		−20dBFS	-	91		dB
		−60dBFS	-	51		dB
	fs=96kHz BW=40kHz	−1dBFS	90	98		dB
		−20dBFS	-	86		dB
		−60dBFS	-	46		dB
	fs=192kHz BW=40kHz	−1dBFS	-	98		dB
		−20dBFS	-	86		dB
		−60dBFS	-	46		dB
Dynamic Range (−60dBFS with A-weighted)			107	114		dB
S/N (A-weighted)			107	114		dB
Input Resistance			9	13		kΩ
Interchannel Isolation			100	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Power Supply Rejection (Note 6)				50	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
AVDD				30	45	mA
DVDD (fs=48kHz)				10	15	mA
DVDD (fs=96kHz)				17	25	mA
DVDD (fs=192kHz)				20	30	mA
Power down mode (PDN pin = "L") (Note 7)						
AVDD+DVDD				10	100	μA

Note 4. This value is (LIN+)−(LIN−) and (RIN+)−(RIN−). Input voltage is proportional to VREF voltage.
Vin = 0.58 x VREF (Vpp).

Note 5. 100μF capacitors are connected between the VREFL/R pins and AVSS.

Note 6. PSR is applied to AVDD and DVDD with 1kHz, 20mVpp. The VREFL and VREFR pins held a constant voltage.

Note 7. All digital input pins are held DVDD or DVSS.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; DFS1 = “L”, DFS0 = “L”)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	–0.005dB	PB	0		21.5	kHz
	–0.02dB		-	22.038	-	kHz
	–0.06dB		-	22.2	-	kHz
	–6.0dB		-	24.0	-	kHz
Stopband		SB	26.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 9)		GD		43.2		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR		1.0		Hz
	–0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; DFS1 = “L”, DFS0 = “H”)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	–0.005dB	PB	0		43.0	kHz
	–0.02dB		-	44.081	-	kHz
	–0.06dB		-	44.5	-	kHz
	–6.0dB		-	48.0	-	kHz
Stopband		SB	53.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 9)		GD		43.1		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR		2.0		Hz
	–0.1dB			13.0		Hz

Note 8. The passband and stopband frequencies scale with fs. The reference frequency of these responses is 1kHz.
Note 9. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; DFS1 = "H", DFS0 = "L")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	–0.005dB	PB	0		86.0	kHz
	–0.02dB		-	88.183	-	kHz
	–0.06dB		-	89.0	-	kHz
	–6.0dB		-	96.0	-	kHz
Stopband		SB	106.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 9)		GD		38.2		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR		4.0		Hz
	–0.1dB			26.0		Hz

Note 8. The passband and stopband frequencies scale with fs. The reference frequency of these responses is 1kHz.
Note 9. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=–400μA)	VOH	DVDD–0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current (Note 10)	Iin	-	-	±10	μA

Note 10. CKS1, CKS0 and TEST pins are internally connected to a pull-down resistor. (typ. 100kΩ)

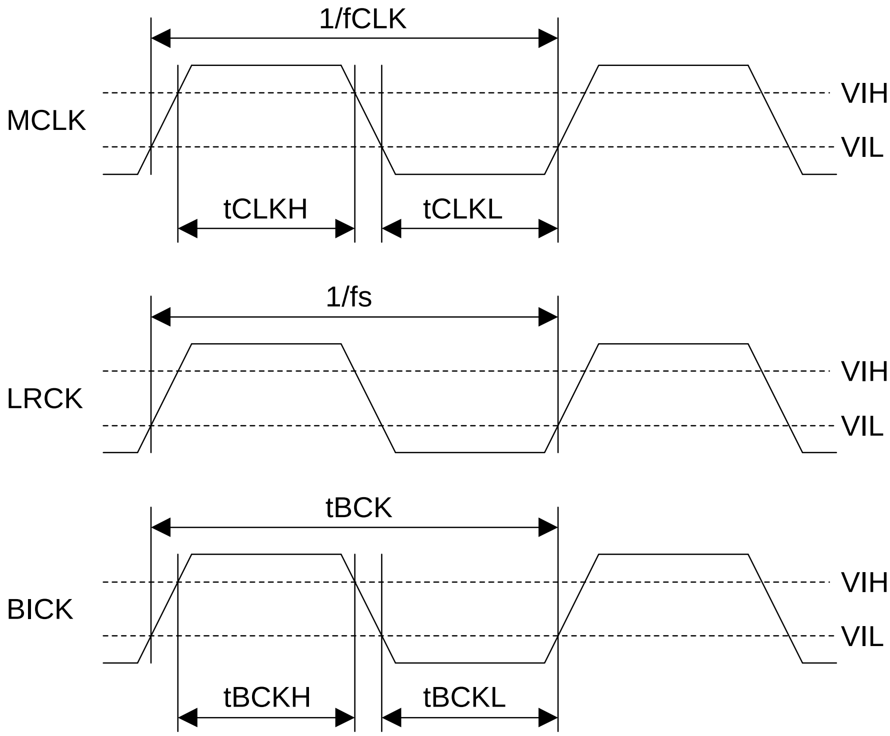
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=4.75 ~ 5.25V; DVDD=3.0 ~ 5.25V; C_L=20pF)

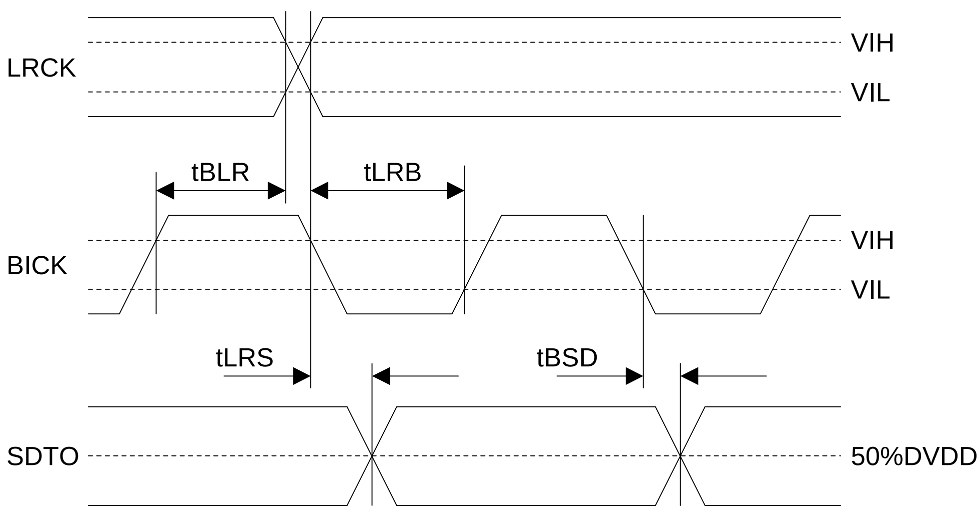
Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	2.048		27.648	MHz
Pulse Width Low		tCLKL	14.5			ns
Pulse Width High		tCLKH	14.5			ns
LRCK Frequency						
Normal Speed Mode		fsn	8		54	kHz
Double Speed Mode		fsd	54		108	kHz
Quad Speed Mode		fsq	108		216	kHz
Duty Cycle	Slave mode		45		55	%
	Master mode			50		%
Audio Interface Timing						
Slave mode						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			ns
Double Speed Mode		tBCK	1/64fsd			ns
Quad Speed Mode		tBCK	1/64fsq			ns
BICK Pulse Width Low		tBCKL	33			ns
Pulse Width High		tBCKH	33			ns
LRCK Edge to BICK "↑"	(Note 11)	tLRB	20			ns
BICK "↑" to LRCK Edge	(Note 11)	tBLR	20			ns
LRCK to SDTO (MSB)	(Except I^2S mode)	tLRS			20	ns
BICK "↓" to SDTO		tBSD			20	ns
Master mode						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	−20		20	ns
BICK "↓" to SDTO		tBSD	−20		20	ns
Reset Timing						
PDN Pulse Width	(Note 12)	tPD	150			ns
PDN "↑" to SDTO valid	(Note 13)	tPDV		516		1/fs

Note 11. BICK rising edge must not occur at the same time as LRCK edge.
Note 12. The AK5385A can be reset by bringing the PDN pin = "L".
Note 13. This cycle is the number of LRCK rising edges from the PDN pin = "H". This value is in master mode
This value is longer 1/fs in slave mode than master mode.

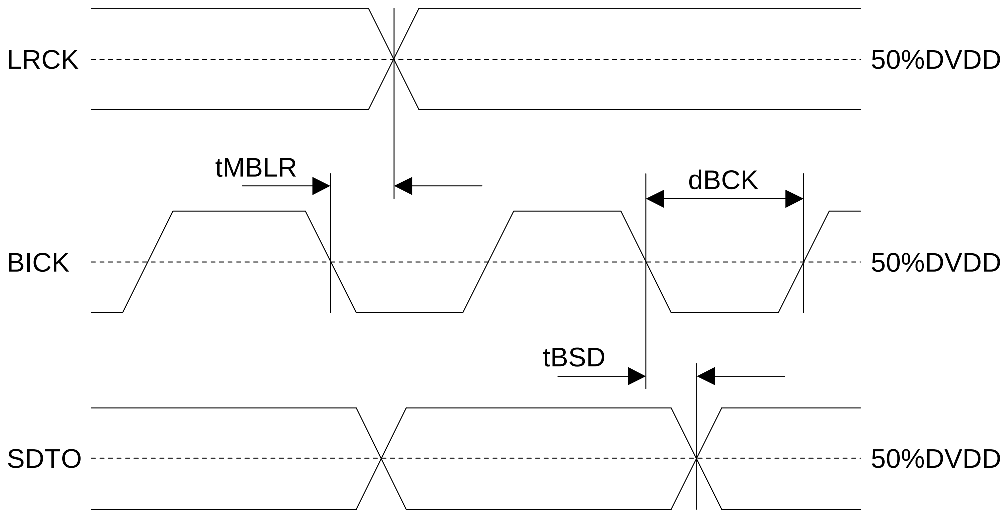
■ Timing Diagram



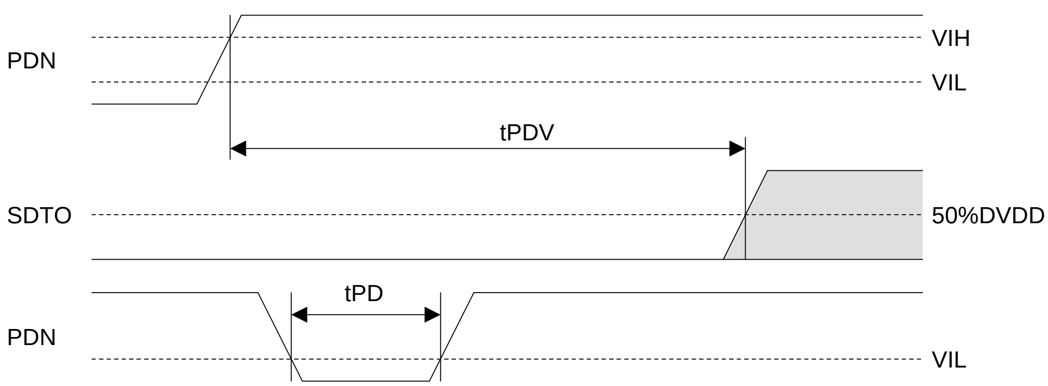
Clock Timing



Audio Interface Timing (Slave mode)



Audio Interface Timing (Master mode)



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

MCLK (256fs/384fs/512fs), BICK (48fs~) and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. MCLK frequency is selected by CKS1-0 pins as shown in Table 2 and LRCK frequency is selected by DFS1-0 pins as shown in Table 3.

As the AK5385A includes the phase detect circuit for LRCK, the AK5385A is reset automatically when the synchronization is out of phase by changing the clock frequencies.

All external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = “L”. If these clocks are not provided, the AK5385A may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5385A in power-down mode (PDN pin = “L”). In master mode, the master clock (MCLK) must be provided unless PDN pin = “L”.

fs	MCLK			
	128fs	256fs	384fs	512fs
32kHz	N/A	8.192MHz	12.288MHz	16.384MHz
44.1kHz	N/A	11.2896MHz	16.9344MHz	22.5792MHz
48kHz	N/A	12.288MHz	18.432MHz	24.576MHz
96kHz	N/A	24.576MHz	N/A	N/A
192kHz	24.576MHz	N/A	N/A	N/A

Table 1. System Clock Example

CKS1 pin	CKS0 pin	MCLK Frequency
L	L	256fs
L	H	128fs
H	L	512fs
H	H	384fs

Table 2. MCLK Frequency

DFS1 pin	DFS0 pin	LRCK Frequency
L	L	8kHz ≤ fs ≤ 54kHz
L	H	54kHz < fs ≤ 108kHz
H	L	108kHz < fs ≤ 216kHz
H	H	N/A

Table 3. Sampling Speed

When changing MCLK frequency in master/slave mode, the AK5385A should reset by PDN pin = “L”. (ex. 12.288MHz(@fs=48kHz) to 24.576MHz(@fs=96kHz) at CKS1 pin = CKS0 pin = “L”.

If the CKS1-0 and DFS1-0 pins are changed with same MCLK frequency in master/slave mode (ex. MCLK is fixed to 24.576MHz and fs is changed from 48kHz (CKS1 pin = “L”, CKS0 pin = “L”) to 96kHz (CKS1 pin = “L”, CKS0 pin = “H”)), no reset by PDN pin = “L” is required.

■ Audio Interface Format

Two kinds of data formats can be chosen with the DIF pin (Table 4). In both modes, the serial data is in MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK. The audio interface supports both master and slave modes. In master mode, BICK and LRCK are output with the BICK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

Mode	DIF pin	SDTO	LRCK	BICK	Figure
0	L	24bit, MSB justified	H/L	≥ 48fs	Figure 1
1	H	24bit, I^2S Compatible	L/H	≥ 48fs	Figure 2

Table 4. Audio Interface Format

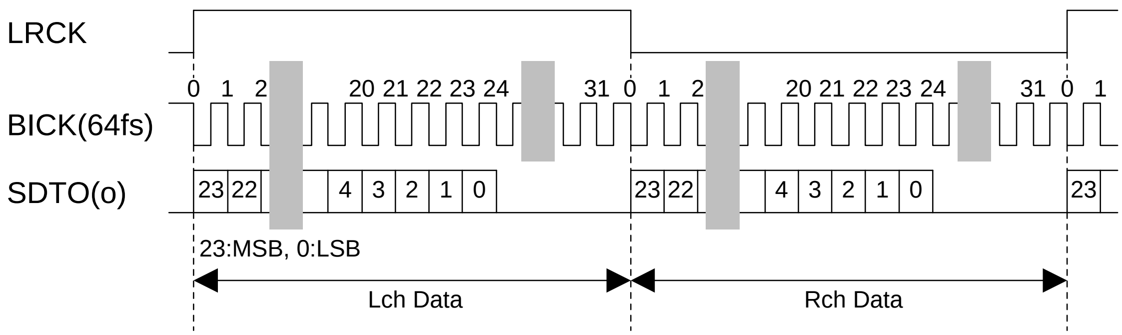


Figure 1. Mode 0 Timing

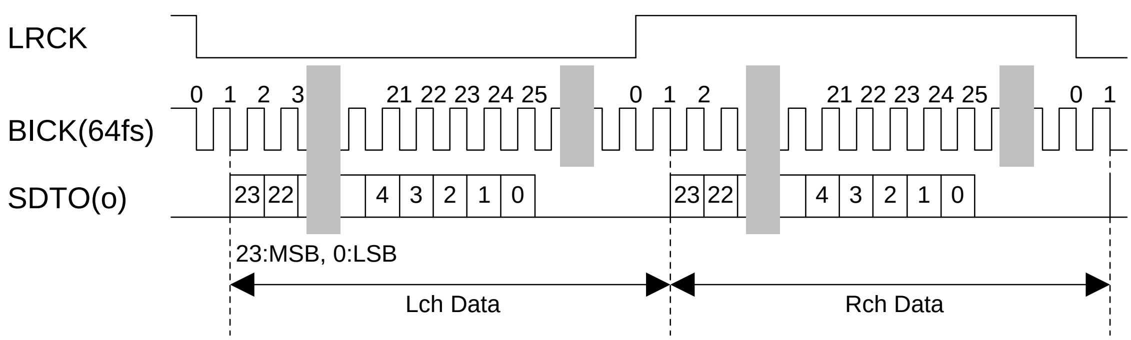


Figure 2. Mode 1 Timing

■ Master Mode and Slave Mode

The M/S pin selects either master or slave modes. M/S pin = "H" selects master mode and "L" selects slave mode. The AK5385A outputs BICK and LRCK in master mode. In slave mode, provide MCLK, BICK and LRCK.

M/S pin	Mode	BICK, LRCK
L	Slave Mode	BICK = Input LRCK = Input
H	Master Mode	BICK = Output LRCK = Output

Table 5. Master mode/Slave mode

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

HPF is controlled by HPFE pin. If HPF setting (ON/OFF) is changed at operating, click noise occurs by changing DC offset. It is recommended that HPF setting is changed at PDN pin = "L".

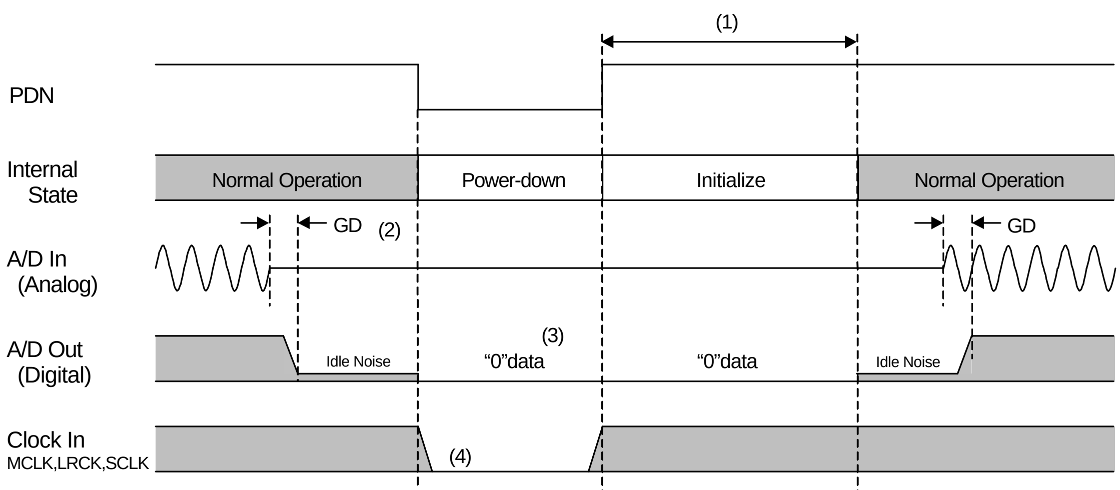
■ Overflow Detection

The AK5385A has overflow detect function for analog input. OVF pin goes to "H" if Lch or Rch overflows (more than −0.3dBFS). OVF output for overflowed analog input has the same group delay as ADC (GD=43.2/fs=0.9ms@fs=48kHz). OVF is "L" for 516/fs (=10.75ms@fs=48kHz) after PDN pin = "↑", and then overflow detection is enabled.

■ Power Down and Reset

The AK5385A is placed in the power-down mode by bringing PDN pin "L" and the digital filter is also reset at the same time. This reset should always be done after power-up. In the power-down mode, the VCOM is AGND level. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 516 cycles of LRCK clock in master mode (517 cycles in slave mode). During initialization, the ADC digital data outputs of both channels are forced to "0". The ADC outputs settle in the data corresponding to the input signals after the end of initialization (Settling approximately takes the group delay time).

The AK5385A should be reset once by bringing PDN pin "L" after power-up. The internal timing starts clocking by the rising edge (falling edge at Mode 1) of LRCK after exiting from reset and power down state by MCLK.



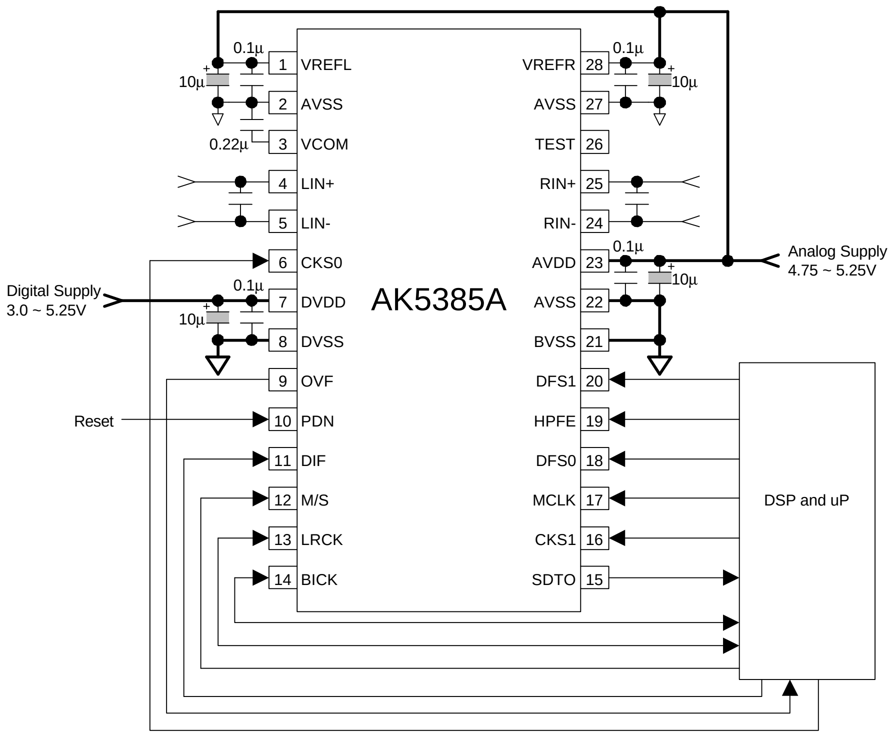
Notes:

(1) 517/fs in slave mode and 516/fs in master mode.
(2) Digital output corresponding to analog input has the group delay (GD).
(3) A/D output is "0" data at the power-down state.
(4) When the external clocks (MCLK, SCLK, LRCK) are stopped, the AK5385A should be in the power-down state.

Figure 3. Power-down/up sequence example

SYSTEM DESIGN

Figure 4 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:
- AVSS, BVSS and DVSS of the AK5385A should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All input pins except pull-down (CKS0, CKS1 and TEST pin) pin should not be left floating.

Figure 4. Typical Connection Diagram

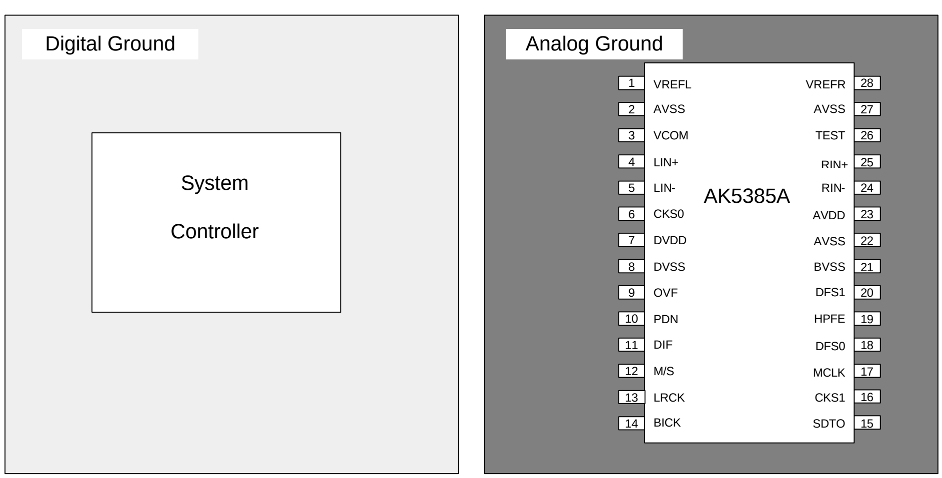


Figure 5. Ground Layout

Note:
- AVSS BVSS, and DVSS must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK5385A requires careful attention to power supply and grounding arrangements. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS, BVSS and DVSS of the AK5385A must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5385A as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The reference voltage for A/D converter is supplied from VREFL/R pins at AVSS reference. AVSS pin is connected to analog ground and an electrolytic capacitor over 10µF parallel with a 0.1µF ceramic capacitor between the VREFL/R pins and the AVSS pin eliminate the effects of high frequency noise. Especially, a ceramic capacitor should be as near to the pins as possible. And all digital signals, especially clocks, should be kept away from the VREFL/R pins in order to avoid unwanted coupling into the AK5385A. No load current may be taken from the VREFL/R pins.

VCOM is a signal ground of this chip. An electrolytic capacitor 0.22µF attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5385A.

3. Analog Inputs

Analog signal is differentially input into the modulator via the LIN+ (RIN+) and the LIN− (RIN−) pins. The input voltage is the difference between the LIN+ (RIN+) and LIN− (RIN−) pins. The full scale of each pin is nominally ±2.9Vpp(typ). The AK5385A can accept input voltages from AVSS to AVDD. The ADC output data format is 2’s compliment. The internal HPF removes the DC offset.

The AK5385A samples the analog inputs at 128fs (6.144MHz@fs=48kHz, Normal Speed Mode). The digital filter rejects noise above the stop band except for multiples of 128fs. The AK5385A includes an anti-aliasing filter (RC filter) to attenuate a noise around 128fs.

The AK5385A accepts +5V supply voltage. Any voltage which exceeds the upper limit of AVDD+0.3V and lower limit of AVSS−0.3V and any current beyond 10mA for the analog input pins (LIN+/−, RIN+/−) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

4. External Analog Circuit Examples

Figure 6 shows an input buffer circuit example 1. This is a full-differential input buffer circuit with an inverted-amp (gain: −10dB). The capacitor of 10nF between LIN+/– (RIN+/–) decreases the clock feed through noise of modulator, and composes a 1st order LPF (fc=360kHz) with 22Ω resistor before the capacitor. This circuit also has a 1st order LPF (fc=370kHz) composed of op-amp. The evaluation board should be referred about the detail.

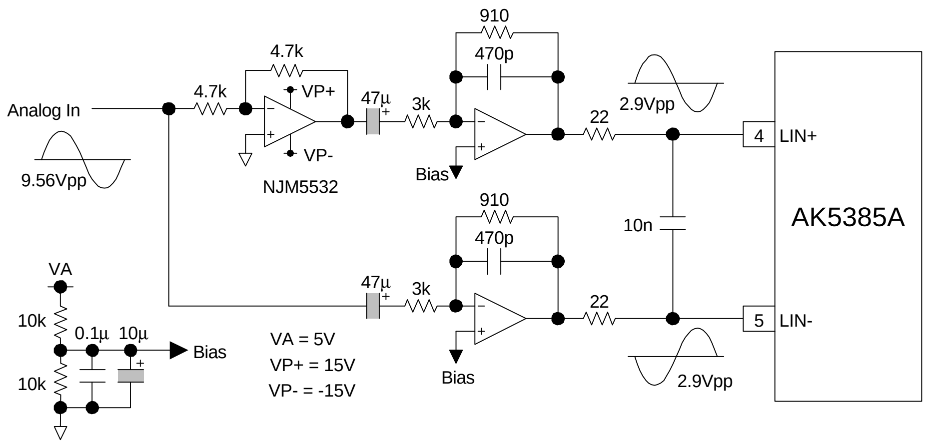


Figure 6.Input Buffer example

Figure 7 shows an input buffer circuit example 2. (1st order HPF: fc=0.66Hz, Table 6; 1st order LPF: fc=590kHz, gain=−14dB, Table 7). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is +/–14.7Vpp.

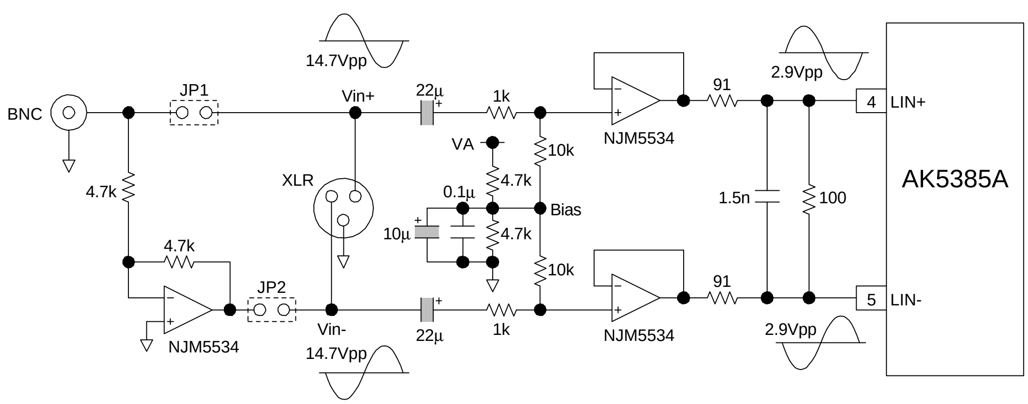


Figure 7.Input Buffer example

fin	1Hz	10Hz
Frequency Response	–1.56dB	–0.02dB

Table 6. Frequency Response of HPF

fin	20kHz	40kHz	6.144MHz
Frequency Response	–0.005dB	–0.02dB	–15.6dB

Table 7. Frequency Response of LPF

5. Measurement Example

Figure 8 shows the S/(N+D) vs. VREF capacitor that is connected between VREFL/R pins and AVSS pin with the 0.1μF capacitor in parallel. X-AXIS is the capacity for VREF; Y-AXIS is S/(N+D).

[Measurement Condition]

- AVDD = 5.0V, DVDD = 3.3V; AVSS = BVSS = DVSS = 0V
- fs = 48kHz
- Measurement Bandwidth = 10Hz ~ 20kHz
- Ta = 25°C
- Using Audio Precision System Two Cascade

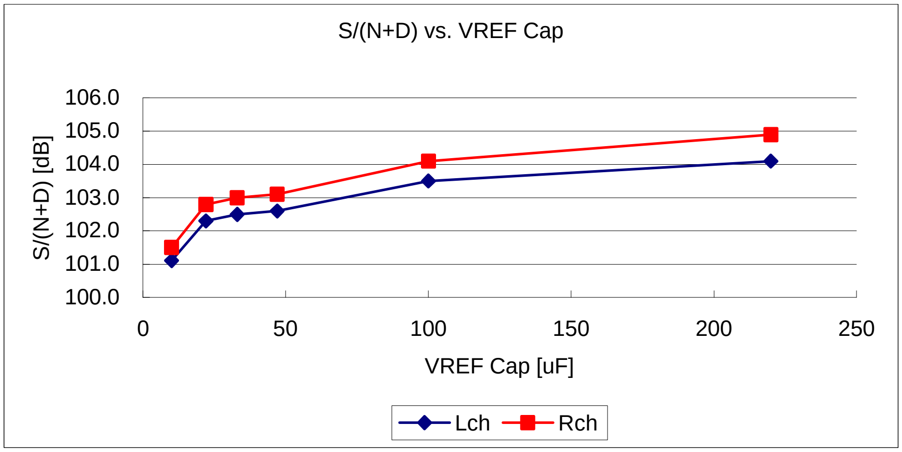


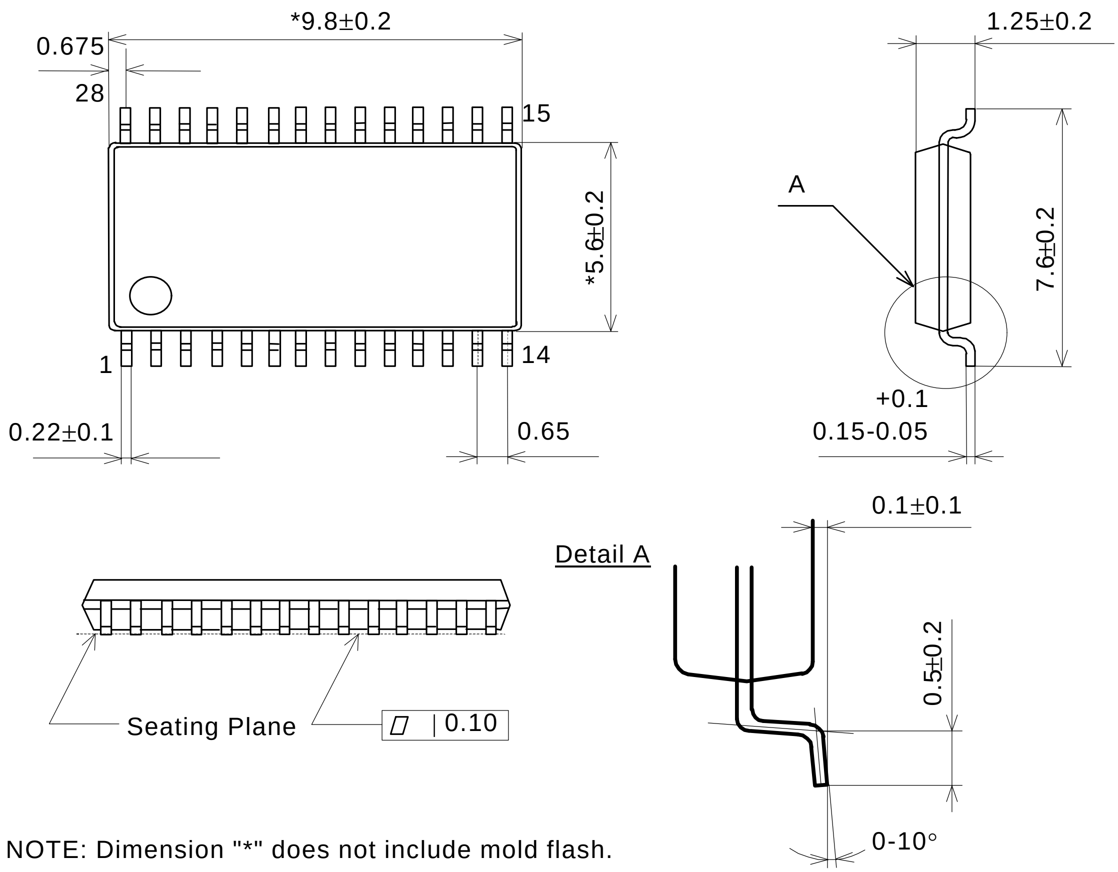
Figure 8. S/(N+D) vs. VREF Cap

6. Synchronization of Multiple Devices

In system where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the AK5385As in the system. The all AK5385As should be reset at the same timing with preventing the reset signal for AK5385A from overlapping on the edge of MCLK, so that all AK5385As begin sampling on the same clock edge.

PACKAGE (AK5385AVF)

28pin VSOP (Unit: mm)



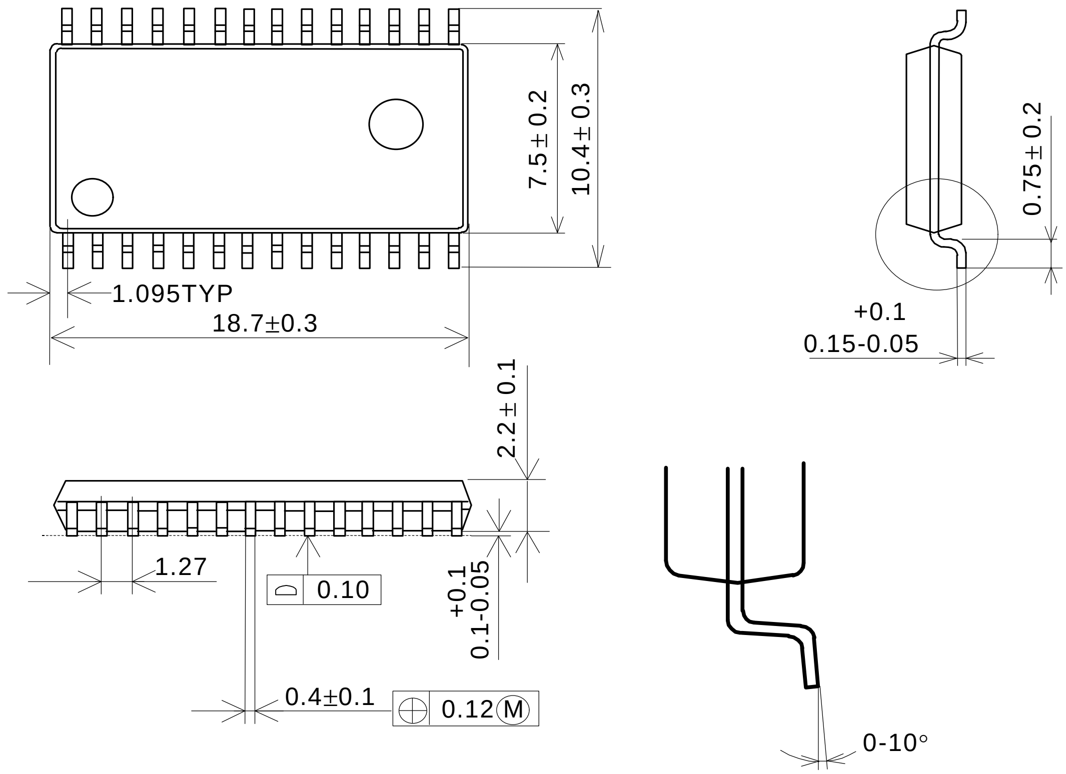
NOTE: Dimension "*" does not include mold flash.

■ **Material & Lead finish**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

PACKAGE (AK5385AVS)

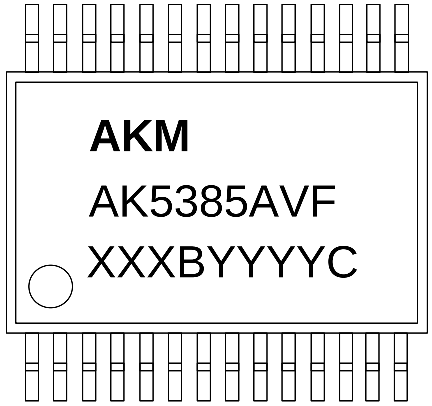
28pin SOP (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

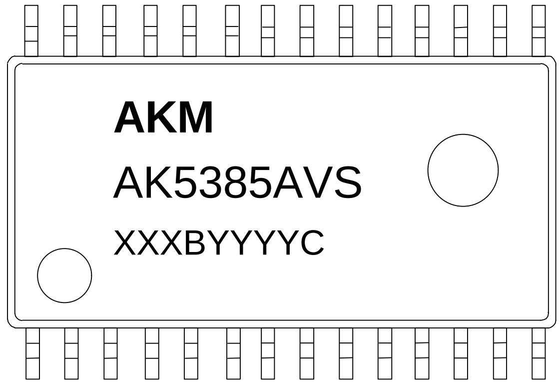
MARKING (AK5385AVF)



XXXBYYYYC Date code identifier

XXXB :Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)

MARKING (AK5385AVS)



XXXBYYYYC Date code identifier

XXXB :Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)