ZiLOG

Z89331
OTP DIGITAL
TELEVISION CONTROLLER

FEATURES

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Part Number	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z89331	24	640	12

*General-Purpose

■ 42-Pin SDIP Package

■ 4.75- to 5.25-Volt Operating Range

■ 0°C to +70°C Temperature Range

■ One-Time Programmable

■ Serial Interfacing I²C Port

■ Fully Customized Character Set

■ Character-Control and Closed-Caption Modes

■ Keypad User Control

■ TV Tuner Serial Interface

■ Direct Video Signals

■ Low-EMI Option

GENERAL DESCRIPTION

The Z89331 One-Time Programmable (OTP) Digital Television Controller is designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The Z89331 features a Z89C00 RISC processor core that controls on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed-caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry-standard I²C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.
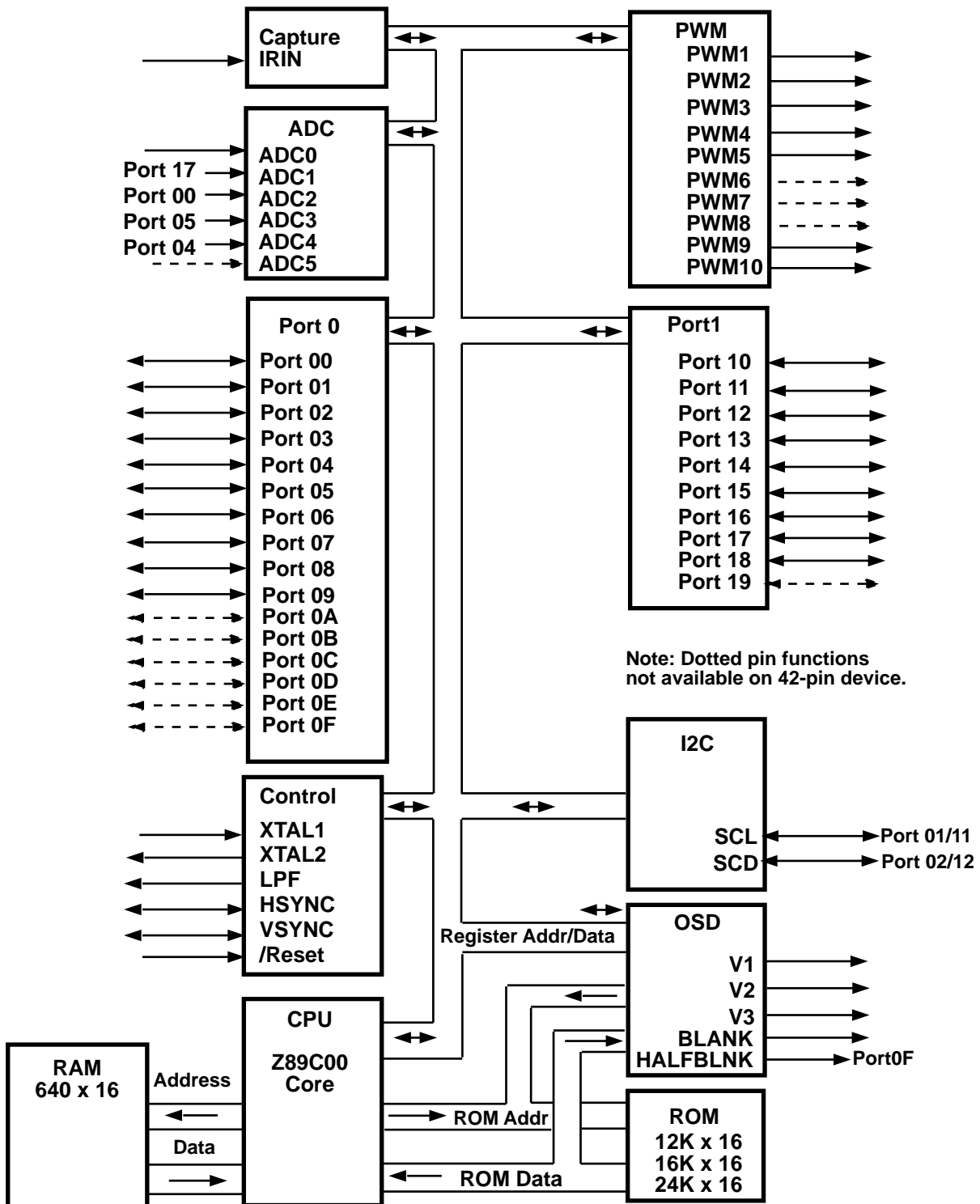
Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

| Capture IRIN | | PWM PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8 PWM9 PWM10 |

ADC
ADC0
Port 17 → ADC1
Port 00 → ADC2
Port 05 → ADC3
Port 04 → ADC4
- - - → ADC5

Port 0
Port 00
Port 01
Port 02
Port 03
Port 04
Port 05
Port 06
Port 07
Port 08
Port 09
Port 0A
Port 0B
Port 0C
Port 0D
Port 0E
Port 0F

Port1
Port 10
Port 11
Port 12
Port 13
Port 14
Port 15
Port 16
Port 17
Port 18
Port 19

Note: Dotted pin functions not available on 42-pin device.

Control
XTAL1
XTAL2
LPF
HSYNC
VSYNC
/Reset

I2C
SCL → Port 01/11
SCD → Port 02/12

Register Addr/Data

OSD
V1
V2
V3
BLANK
HALFBLNK → Port0F

CPU Z89C00 Core

RAM 640 x 16
Address
Data

ROM Addr
ROM Data

ROM 12K x 16 16K x 16 24K x 16

Functional Block Diagram