Xilinx Launches Design Reuse Initiative

New tools allow you to capture and share your own IP over the Internet.

by Jim Burnham, CORE Generator Product Manager, Xilinx, jim.burnham@xilinx.com

Xilinx recently announced a design reuse initiative aimed at helping you implement designs for reuse and share your intellectual property (IP) internally. The first offerings include:

- **The IP Internet Capture™ tool** - allows you to easily capture and package intellectual property (IP) you have already created for Xilinx FPGAs and share it inside your organization with other design teams, over the Internet.
- **The IP Remote Interface™ tool** - provides you (and third-party developers) with a method to integrate your own parameter-driven IP with the Xilinx CORE Generator system. These cores can be distributed or sold over the Web in a secure environment.

As part of the initiative, Xilinx also created a manual named "Xilinx Design Reuse Methodology for ASIC and FPGA Designers," a supplement to the "Reuse Methodology Manual" from Synopsys and Mentor Graphics. The Xilinx Reuse manual provides guidelines for designers who want a common strategy for reusing intellectual property, regardless of whether it was developed for ASICs or for FPGAs.

"Xilinx customers have been using million-gate FPGAs for more than a year, and they have benefited from leadership products such as the Xilinx 64-bit, 66-MHz PCI core for those devices" said Xilinx CEO Wim Roelandts."While cores are important to large designs, we also want to help customers leverage the tremendous value of the intellectual property they have developed internally for FPGAs. This initiative goes hand-in-hand with our recent announcement of the new Virtex-E multi-million-gate FPGAs, and it will help customers address challenges of reuse, modular design techniques, and team-based design."

IP Internet Capture Tool

The new IP Internet Capture tool, the first of a planned series of programmable logic design reuse software products from Xilinx, provides you with an automated method to identify, capture, and document a module of synthesizable VHDL or Verilog code, or a fixed-function netlist. The IP Internet Capture tool prompts you for key reuse information such as module naming and cataloging information,

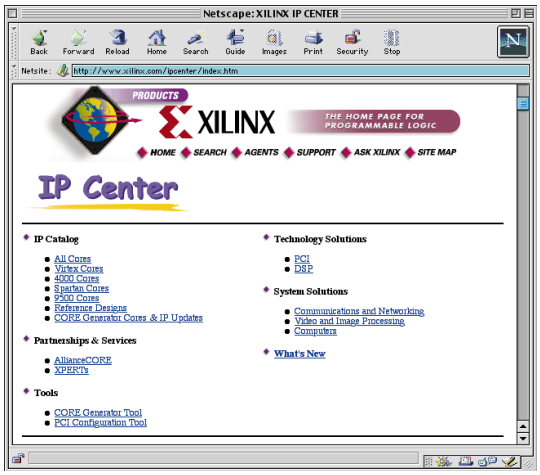

Figure 1 - Design Reuse Tools Available from the Xilinx IP Center

module description, and details about technical support and module source files. It supports both PDF files and HTML-based Web pages to document cores, and it allows you to create a directory for copying and creating files and creating Web files.

By creating a Web page with links to download the module, the IP Internet Capture tool allows distribution of your intellectual property over your network, as well as over internal or external web sites. Once the new module has been captured and posted, other engineers can use standard Internet browsers to download the IP and install it in their copy of the Xilinx CORE Generator system.

The IP Internet Capture tool supports all Xilinx FPGA families.

IP Remote Interface Tool

The new IP Remote Interface tool is a new feature of the Xilinx CORE Generator system, providing the ability to access IP over the Web. Third-party Xilinx AllianceCORE partners or customer teams can use the IP Remote Interface tool to create parameter-driven cores. It allows IP designers to create their own graphical user interface and software executables. These applications with customer-specified parameters can then select from a set of fixed net lists, modify generic values in VHDL or Verilog source code, or drive algorithmic software code implemented in programming languages such as Perl, C++, or Java.

This tool provides a high level of security, and it controls access to IP source code, which can be encrypted or compiled. Xilinx AllianceCORE partners can develop parameter-driven cores that access encrypted source code and then write an encrypted or clear-text netlist. Partners can also control access to their cores by requiring authentication or a password. IP developers can also catalog their cores in the Xilinx CORE Generator, and then, through a Web address, provide secure access to their application. This feature provides for both authenticated access and source code security.

"Xilinx has been successfully offering customers access to IP, such as our PCI core, BaseBlox, DSP cores, and reference designs through the IP Center™ on the Xilinx website," said Rich Sevcik, senior vice president of software, cores and support at Xilinx. "Providing our AllianceCORE partners and customers with this capability extends our commitment, made a year ago in the Silicon Xpresso initiative, to step up use of the Internet to increase the productivity of designers."

Xilinx Design Reuse Methodology Manual

The new "Xilinx Design Reuse Methodology for ASIC and FPGA Designers" manual is intended for designers who need to target both ASIC and FPGA architectures with the same RTL code. This Xilinx supplement to the Synopsys and Mentor Graphics manual provides an overview of FPGA system-level features and contains general RTL synthesis coding guidelines that have the most impact on improving system performance.

Conclusion

The IP Internet Capture and IP Remote Interface tools, as well as "Xilinx Design Reuse Methodology for ASIC and FPGA Designers" manual are available from the IP Center on the Xilinx website (www.xilinx.com). The Xilinx IP Center has long been a resource offering access to complete IP solutions. Design reuse is the latest addition to the Xilinx list of IP solutions. Σ