- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range . . . 0 V to 4.25 V (Min)at 5-V Single Supply**
- **Low Noise . . . 16 nV/√Hz Typ at f = 1 kHz**
- **Low Input Offset Voltage 950 µV Max at T_A = 25°C (TLV2442A)**
- **Low Input Bias Current . . . 1 pA Typ**
- **600-Ω Output Drive**
- **High-Gain Bandwidth . . . 1.8 MHz Typ**
- **Low Supply Current . . . 750 µA Per Channel Typ**
- **Macromodel Included**

description

The TLV2442 and TLV2442A are dual rail-to-rail output operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. In addition, the common-mode input voltage range has been extended over typical standard CMOS amplifiers making this device available for a wider range of applications.

The TLV2442 and TLV2442A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices for inputs to analog-to-digital converters (ADCs). The TLV2442 and TLV2442A also has the ability to drive 600-Ω loads for telecom applications. This feature, combined with its temperature performance, makes the TLV2442 family ideal for ISA and PCMCIA modems, digital cameras, pressure sensors, line cards, active voltage regulator (VR) sensors, accelerometers, portable medical applications, hand-held metering, and many other applications.

The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. Also, this technology makes possible input impedance levels that meet or exceed levels offered by topgate JFET and expensive dielectric-isolated devices. The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2. However, exercise care in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

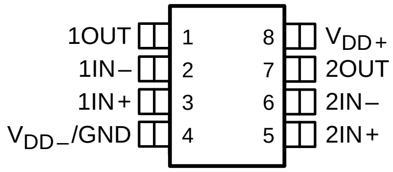
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)	
0°C to 70°C	2.5 mV	TLV2442CD	—	—	TLV2442CPWLE	—	TLV2442Y
−40°C to 85°C	950 µV 2.5 mV	TLV2442AID TLV2442ID	— —	— —	TLV2442AIPWLE —	— —	
−55°C to 125°C	950 µV 2.5 mV	— —	TLV2442AMFK TLV2442MFK	TLV2442AMJG TLV2442MJG	— —	TLV2442AMU TLV2442MU	—

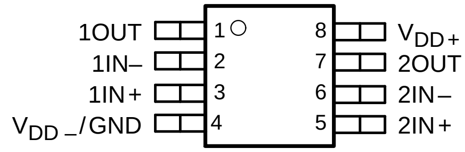
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2442CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

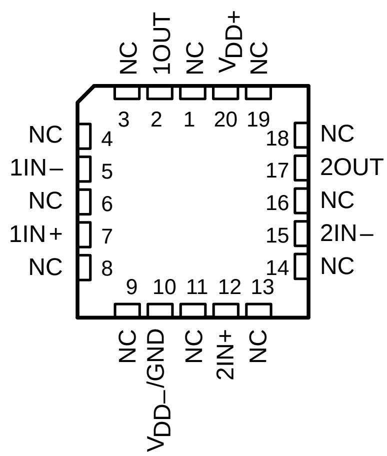
D OR JG PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

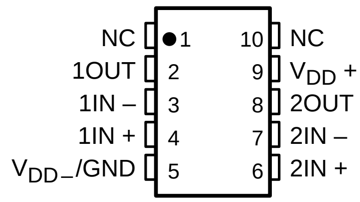


FK PACKAGE
(TOP VIEW)



NC – No internal connection

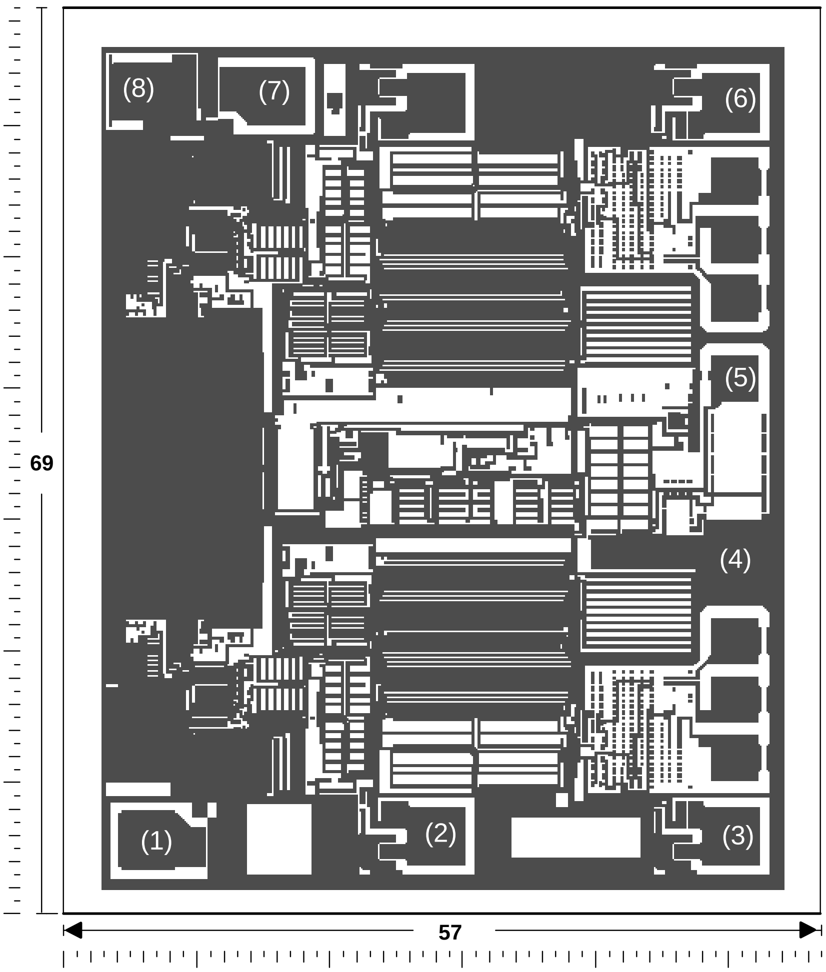
U PACKAGE
(TOP VIEW)

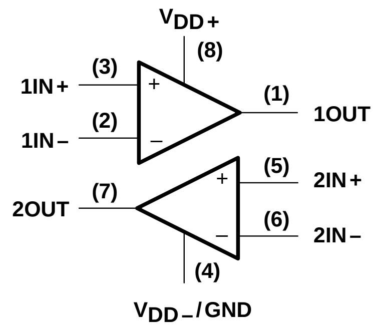


TLV2442Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2442C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

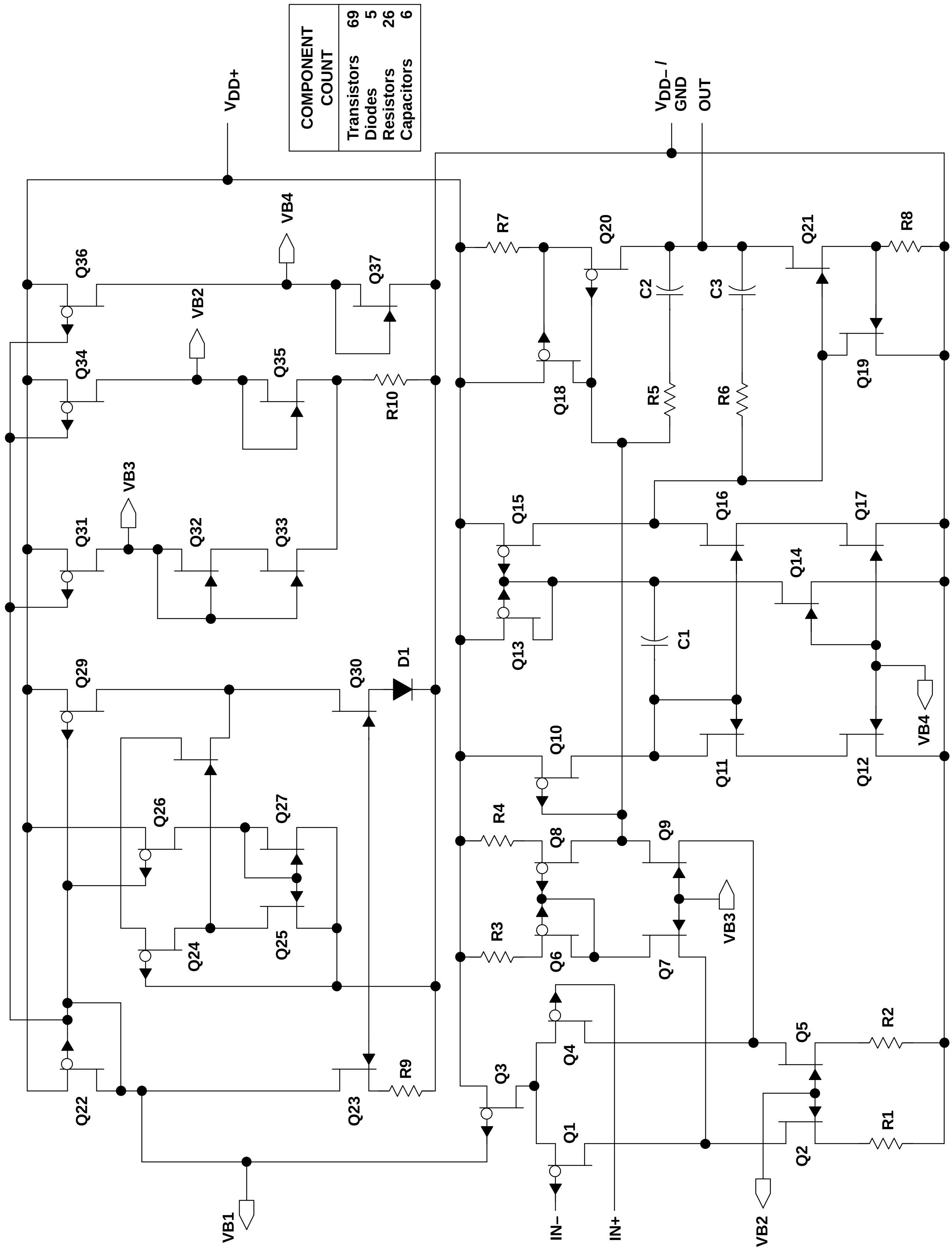
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . $\pm V_{DD}$
Input voltage, V_I (any input, see Note 1) . . . –0.3 V to V_{DD}
Input current, I_I (any input) . . . ±5 mA
Output current, I_O . . . ±50 mA
Total current into V_{DD+} . . . ±50 mA
Total current out of V_{DD-} . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . unlimited
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . 0°C to 70°C
I suffix . . . –40°C to 85°C
M suffix . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.3	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.3	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.3	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C MIN	TLV2442C TYP	TLV2442C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		300	2000	µV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV,	R_S = 50 Ω	25°C	0 to 2.25	–0.25 to 2.5		V
				Full range	0 to 2			
V_{OH}	High-level output voltage	I_O = – 100 µA		25°C		2.98		V
		I_O = – 3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_O = 100 µA	25°C		0.02		V
		V_{IC} = 0,	I_O = 3 mA	25°C		0.63		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 600 Ω	25°C	0.7	1		V/mV
				Full range	0.4			
			R_L = 1 mΩ	25°C		750		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.25 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	65	75		dB
				Full range	55			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, No load	$V_{IC} = V_{DD}/2$,	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		1.5	2.2	mA
				Full range			2.2	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442I			TLV2442AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		300	2000		300	950	µV
				Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.25	–0.25 to 2.5		0 to 2.25	–0.25 to 2.5		V
				Full range	0 to 2			0 to 2			
V_{OH}	High-level output voltage	I_O = –100 µA		25°C		2.98			2.98		V
		I_O = –3 mA		25°C		2.5			2.5		
				Full range	2.25			2.25			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_O = 100 µA	25°C		0.02			0.02		V
		V_{IC} = 0,	I_O = 3 mA	25°C		0.63			0.63		
				Full range			1			1	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 600 Ω	25°C	0.7	1		0.7	1		V/mV
				Full range	0.4			0.4			
			R_L = 1 mΩ	25°C		750			750		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.25 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	75		dB
				Full range	55			55			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		1.45	2.2		1.45	2.2	mA
				Full range			2.2			2.2	

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C, TLV2442I TLV2442AI MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 600 Ω, C_L = 100 pF		25°C	0.65	1.3		V/µs
				Full range	0.65			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		170		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.6		µV
		f = 0.1 Hz to 10 Hz		25°C		5.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.08%		
			A_V = 10			0.3%		
			A_V = 100			2%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		1.75		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω, A_V = 1, C_L = 100 pF		25°C		0.9		MHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 600 Ω, C_L = 100 pF	To 0.1%	25°C		1.5		µs
			To 0.01%			3.2		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		65°		
	Gain margin			25°C		9		dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is –40°C to 85°C.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2442M			TLV2442AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2000		300	950	μV
			Full range			2500			1600	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			260			260	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV, R_S = 50 Ω	25°C	0 to 2.25	–0.25 to 2.5		0 to 2.25	–0.25 to 2.5		V
			Full range	0 to 2			0 to 2			
V_{OH}	High-level output voltage	I_O = –100 μA	25°C		2.98			2.98		V
		I_O = –3 mA	25°C		2.5			2.5		
			Full range	2.25			2.25			
V_{OL}	Low-level output voltage	V_{IC} = 0, I_O = 100 μA	25°C		0.02			0.02		V
		V_{IC} = 0, I_O = 3 mA	25°C		0.63			0.63		
			Full range			1			1	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V, R_L = 600 Ω	25°C	0.7	1		0.7	1		V/mV
			Full range	0.4			0.4			
		V_O = 1 V to 2 V, R_L = 1 mΩ	25°C		750			750		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.25 V, V_O = 1.5 V, R_S = 50 Ω	25°C	65	75		65	75		dB
			Full range	50			50			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = $V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		1.45	2.2		1.45	2.2	mA
			Full range			2.2			2.2	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442M TLV2442AM MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 600 Ω, C_L = 100 pF		25°C	0.65	1.3		V/μs
				Full range	0.4			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		170		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.6		μV
		f = 0.1 Hz to 10 Hz		25°C		5.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.08%		
			A_V = 10			0.3%		
			A_V = 100			2%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		1.75		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω, A_V = 1, C_L = 100 pF		25°C		0.9		MHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 600 Ω, C_L = 100 pF	To 0.1%	25°C		1.5		μs
			To 0.01%			3.2		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		65°		
	Gain margin			25°C		9		dB

† Full range is –55°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		300	2000	µV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le 5$ mV,	$R_S = 50\ \Omega$	25°C	0 to 4.25	–0.25 to 4.5		V
				Full range	0 to 4			
V_{OH}	High-level output voltage	$I_{OH} = -100\ \mu A$		25°C		4.97		V
		$I_{OH} = -5$ mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 100\ \mu A$	25°C		0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 5$ mA	25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 600\ \Omega$‡	25°C	0.9	1.3		V/mV
				Full range	0.5			
			$R_L = 1$ mΩ‡	25°C		950		
r_{id}	Differential input resistance			25°C		10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	$A_V = 10$	25°C		140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 4.25 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	75		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		1.5	2.2	mA
				Full range			2.2	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442I MIN	TLV2442I TYP	TLV2442I MAX	TLV2442AI MIN	TLV2442AI TYP	TLV2442AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2000		300	950	µV
				Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV,	R_S = 50 Ω	25°C	0 to 4.25	–0.25 to 4.5		0 to 4.25	–0.25 to 4.5		V
				Full range	0 to 4			0 to 4			
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		4.97			4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		4	4.35		
				Full range	4			4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.8			0.8		
				Full range			1.25			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 600 Ω‡	25°C	0.9	1.3		0.9	1.3		V/mV
				Full range	0.5			0.5			
			R_L = 1 mΩ‡	25°C		950			950		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.25 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		1.5	2.2		1.5	2.2	mA
				Full range			2.2			2.2	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442C, TLV2442I TLV2442AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡		25°C	0.75	1.4		V/μs
				Full range	0.75			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		130		nV/√Hz
		f = 1 kHz		25°C		16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.8		μV
		f = 0.1 Hz to 10 Hz		25°C		3.6		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.17%		
			A_V = 100			1.5%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		1.81		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		0.5		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		μs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡, C_L = 100 pF‡		25°C		68°		
	Gain margin			25°C		8		dB

† Full range for the C suffix is 0°C to 70°C. Full range for the I suffix is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442M MIN	TLV2442M TYP	TLV2442M MAX	TLV2442AM MIN	TLV2442AM TYP	TLV2442AM MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2000		300	950	μV
				Full range			2500			1600	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			260			260	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert$ ≤ 5 mV,	R_S = 50 Ω	25°C	0 to 4.25	–0.25 to 4.5		0 to 4.25	–0.25 to 4.5		V
				Full range	0 to 4			0 to 4			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97			4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		4	4.35		
				Full range	4			4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.8			0.8		
				Full range			1.25			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 600 Ω‡	25°C	0.9	1.3		0.9	1.3		V/mV
				Full range	0.5			0.5			
			R_L = 1 mΩ‡	25°C		950			950		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.25 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		1.5	2.2		1.5	2.2	mA
				Full range			2.2			2.2	

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2442M TLV2442AM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡		25°C	0.75	1.4		V/μs
				Full range	0.5			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		130		nV/√Hz
		f = 1 kHz		25°C		16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.8		μV
		f = 0.1 Hz to 10 Hz		25°C		3.6		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.17%		
			A_V = 100			1.5%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		1.81		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		0.5		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		μs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡, C_L = 100 pF‡		25°C		68°		
	Gain margin			25°C		8		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2442Y MIN	TLV2442Y TYP	TLV2442Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		300		µV
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		2		µV/°C
	Input offset voltage long-term drift (see Note 4)	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		0.5		pA
I_{IB}	Input bias current	V_{IC} = 0, R_S = 50 Ω	V_O = 0,		1		pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		–0.25 to 2.5		V
V_{OH}	High-level output voltage	I_O = –100 µA			2.98		V
		I_O = –3 mA			2.5		
V_{OL}	Low-level output voltage	V_{IC} = 0	I_O = 100 µA		0.02		V
			I_O = 3 mA		0.63		
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 600 Ω		1		V/mV
			R_L = 1 mΩ		750		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loopoutput impedance	f = 1 MHz,	A_V = 10		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.25 V, R_S = 50 Ω	V_O = 1.5 V,		75		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, No load	$V_{IC} = V_{DD}/2$,		95		dB
I_{DD}	Supply current	V_O = 1.5 V,	No load		1.5		mA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2442Y MIN	TLV2442Y TYP	TLV2442Y MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, C_L = 100 pF	R_L = 600 Ω,		1.3		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz			170		nV/√Hz
		f = 1 kHz			18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			2.6		μV
		f = 0.1 Hz to 10 Hz			5.1		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 600 Ω, f = 1 kHz	A_V = 1		0.08%		
			A_V = 10		0.3%		
			A_V = 100		2%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 600 Ω,		1.75		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω,	A_V = 1, C_L = 100 pF		0.9		MHz
t_s	Settling time	A_V = –1, Step = –2.3 V to 2.3 V, R_L = 600 Ω, C_L = 100 pF	To 0.1%		1.5		μs
			To 0.01%		3.2		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF		65°		
	Gain margin				9		dB

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2442Y MIN	TLV2442Y TYP	TLV2442Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω		300		µV
	Input offset voltage long-term drift (see Note 4)				0.002		µV/mo
I_{IO}	Input offset current				0.5		pA
I_{IB}	Input bias current				1		pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 5 mV,	R_S = 50 Ω		–0.25 to 4.5		V
V_{OH}	High-level output voltage	I_{OH} = –100 µA			4.97		V
		I_{OH} = –5 mA			4.35		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 100 µA		0.01		V
			I_{OL} = 5 mA		0.8		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 600 Ω†		1.3		V/mV
			R_L = 1 mΩ†		950		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10		140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.25 V,	V_O = 2.5 V		75		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V,	V_{IC} = V_{DD}/2		95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		1.5		mA

† Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2442Y MIN	TLV2442Y TYP	TLV2442Y MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 600 Ω†, C_L = 100 pF†			1.4		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			130		nV/√Hz
		f = 1 kHz			16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1.8		µV
		f = 0.1 Hz to 10 Hz			3.6		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 600 Ω†	A_V = 1		0.017%		
			A_V = 10		0.17%		
			A_V = 100		1.5%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω,† C_L = 100 pF†			1.81		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 600 Ω†, C_L = 100 pF†			0.5		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 600 Ω†, C_L = 100 pF†	To 0.1%		1.5		µs
			To 0.01%		2.6		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω†, C_L = 100 pF†			68°		
	Gain margin				8		dB

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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† For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2442
INPUT OFFSET VOLTAGE

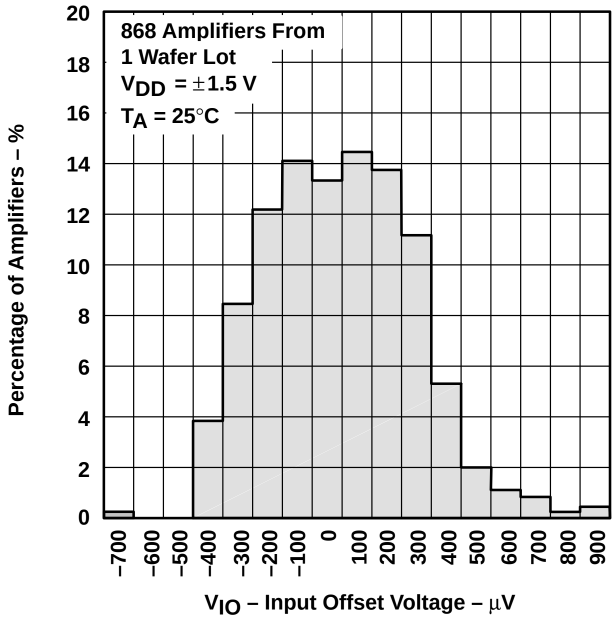


Figure 1

DISTRIBUTION OF TLV2442
INPUT OFFSET VOLTAGE

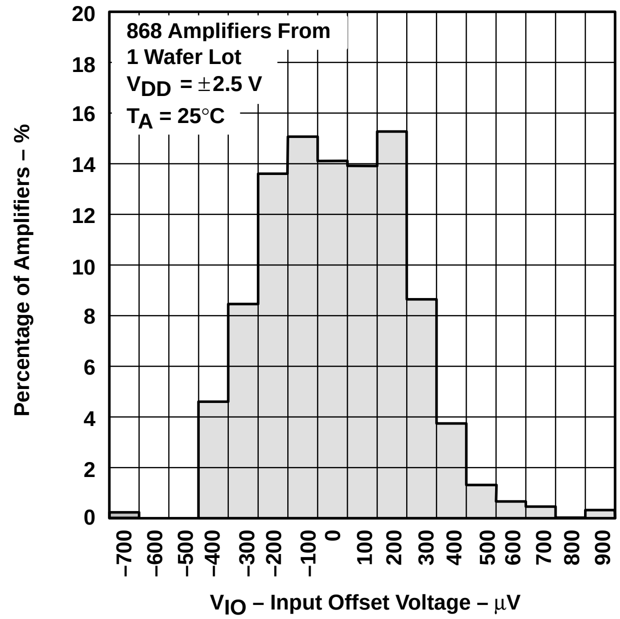


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

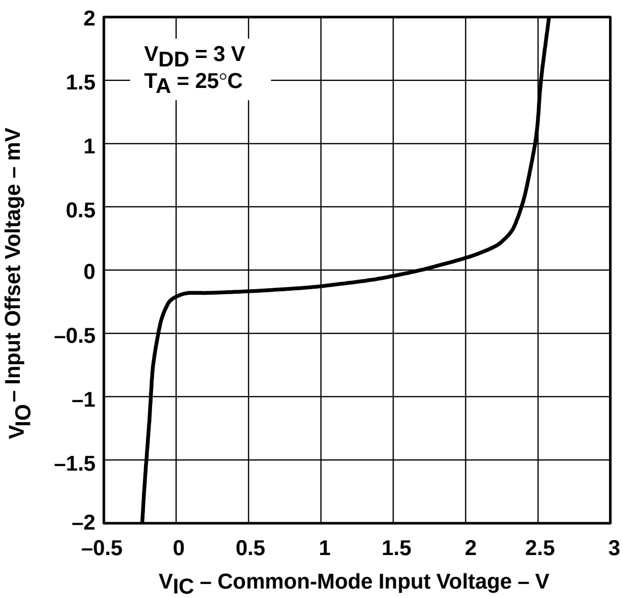


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

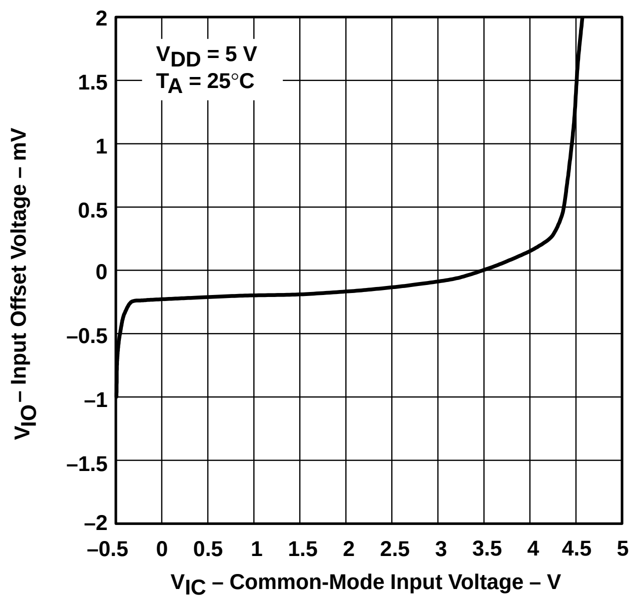


Figure 4

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

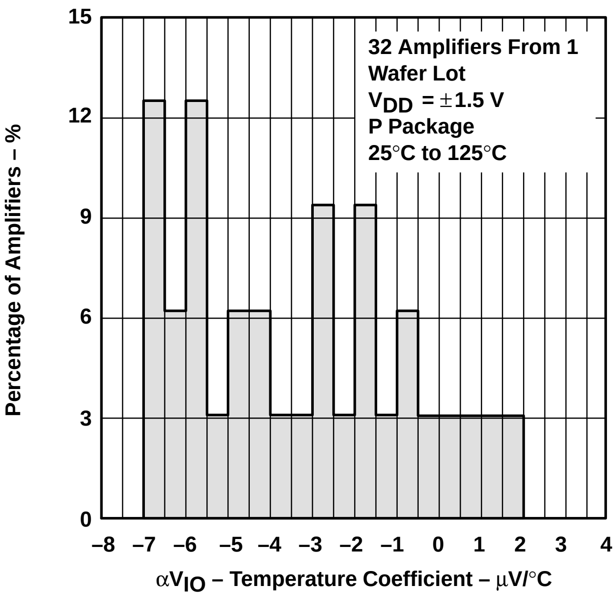


Figure 5

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

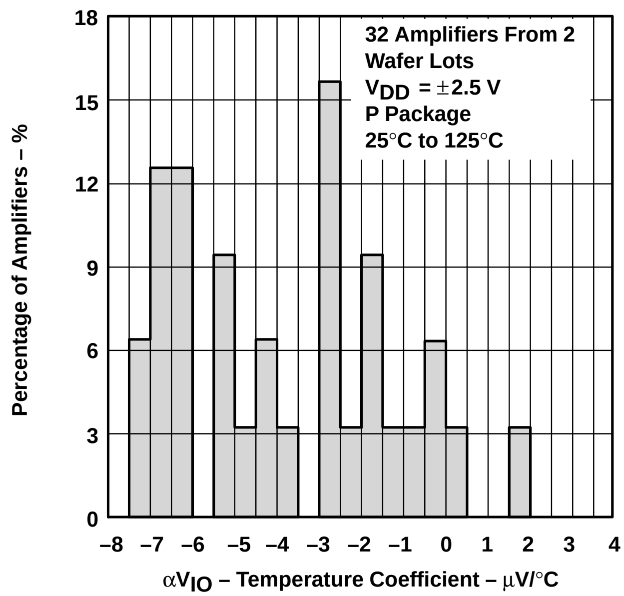


Figure 6

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

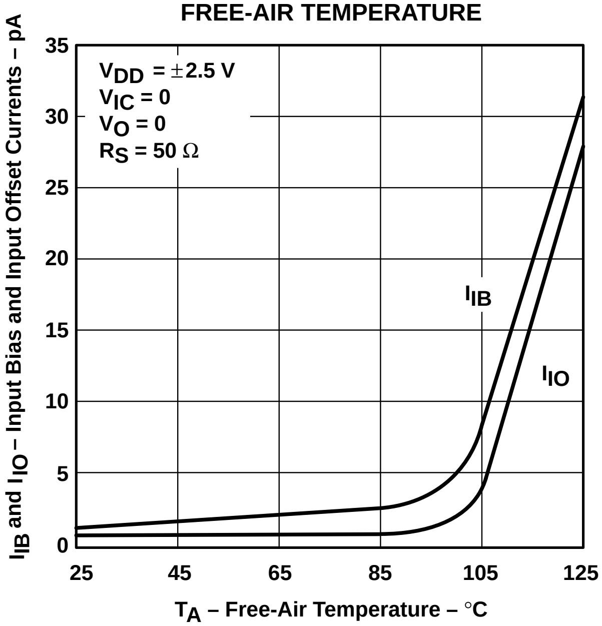


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

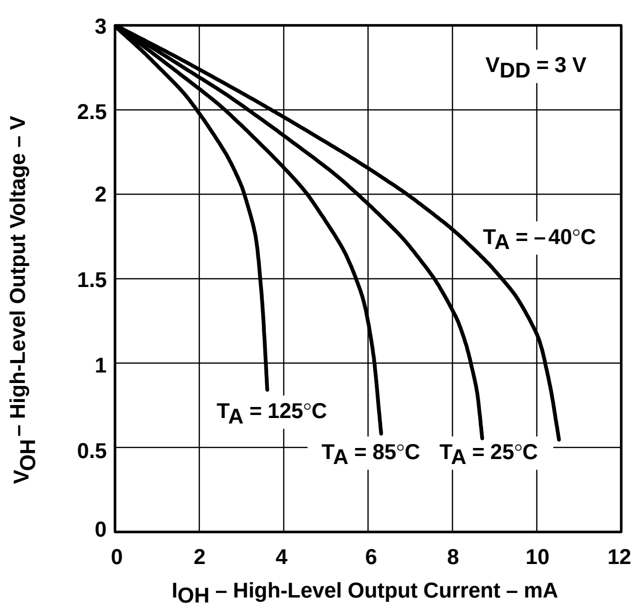


Figure 8

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

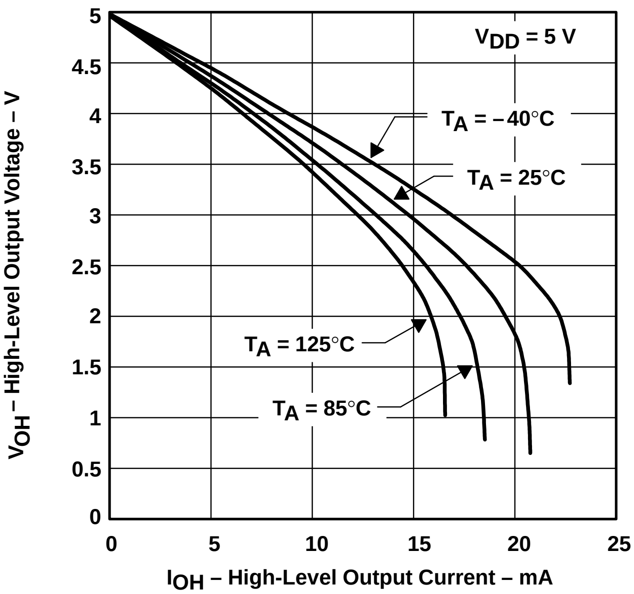


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

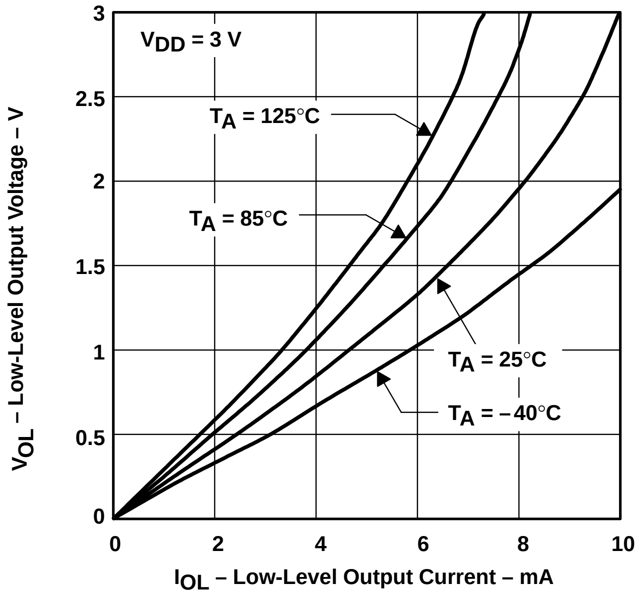


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

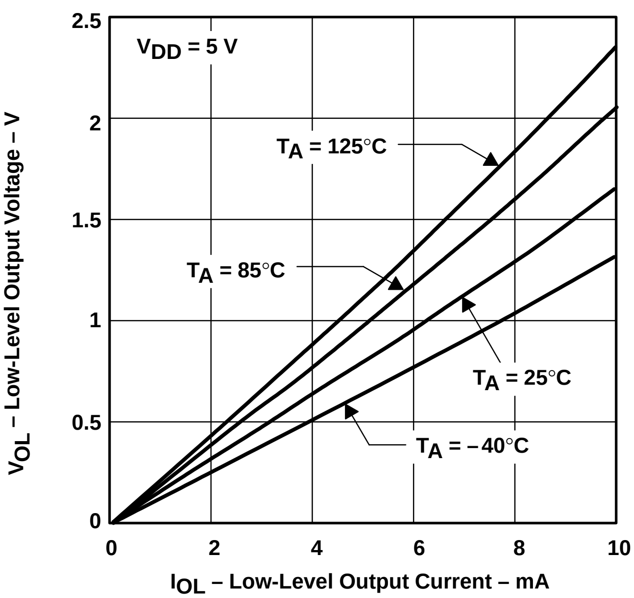


Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

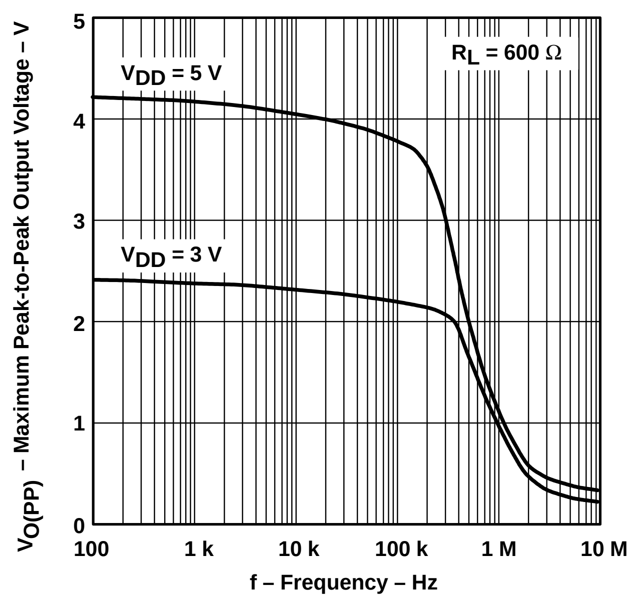


Figure 12

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

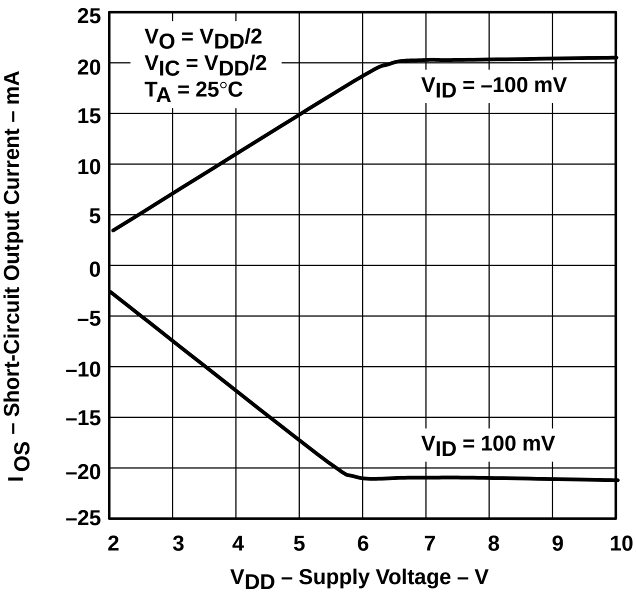


Figure 13

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

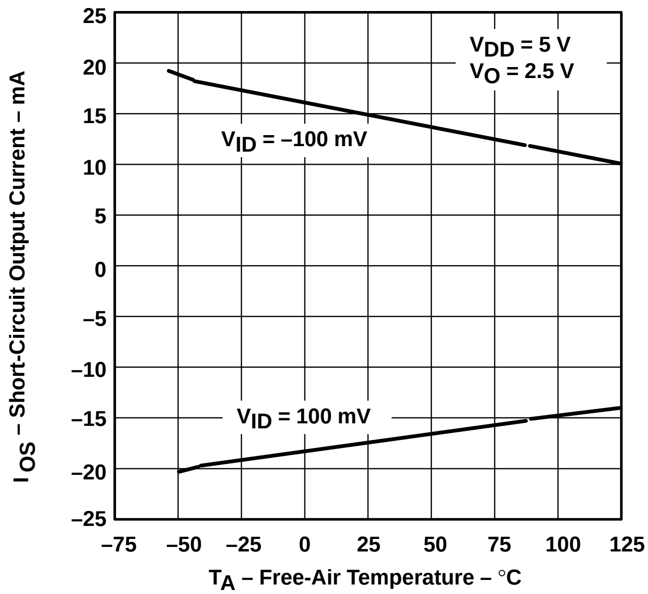


Figure 14

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

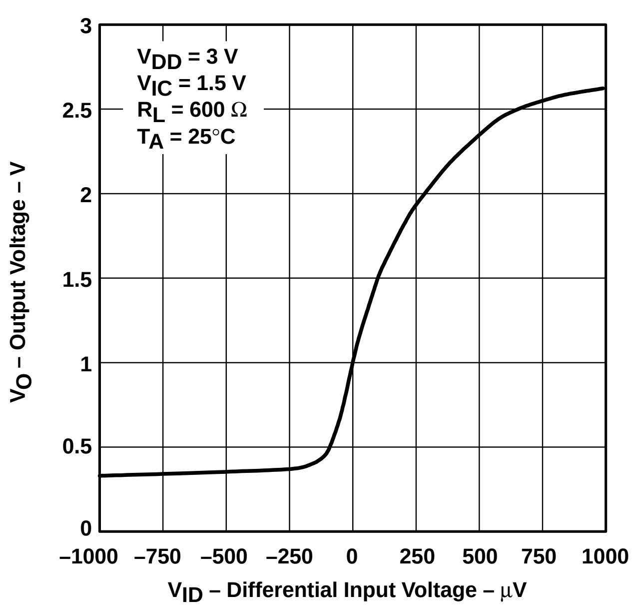


Figure 15

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

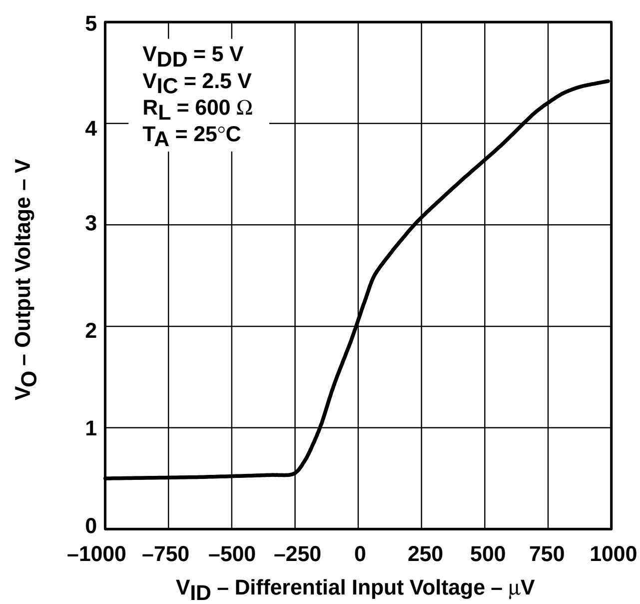


Figure 16

TYPICAL CHARACTERISTICS

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE**

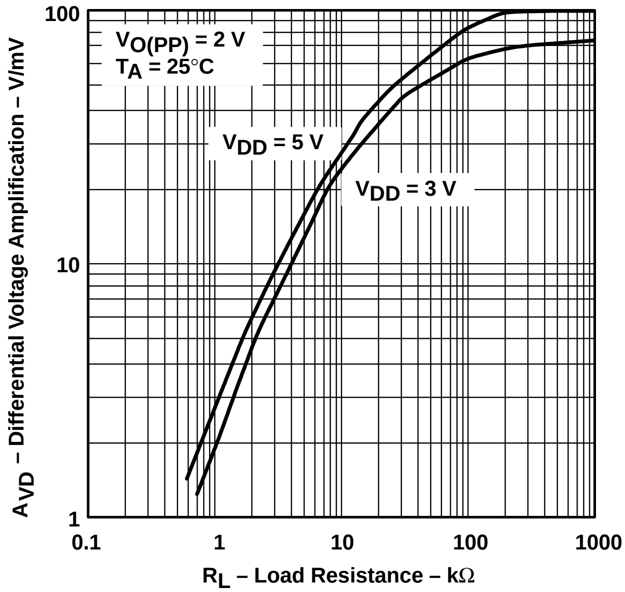


Figure 17

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY**

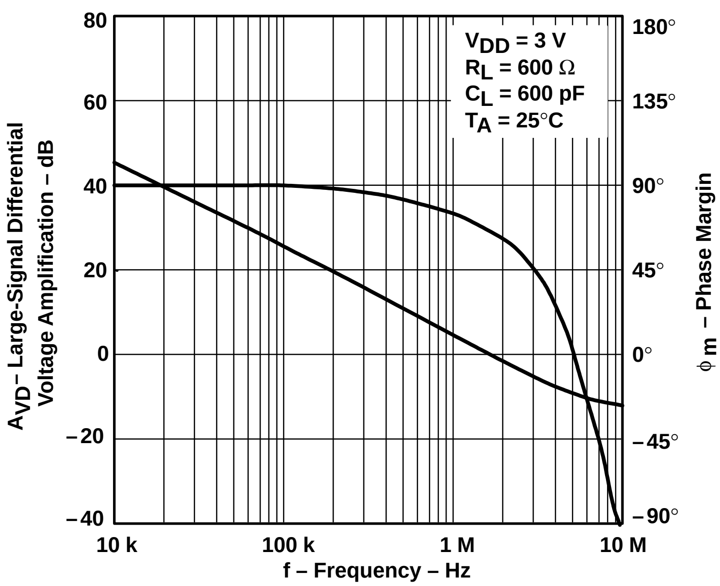


Figure 18

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

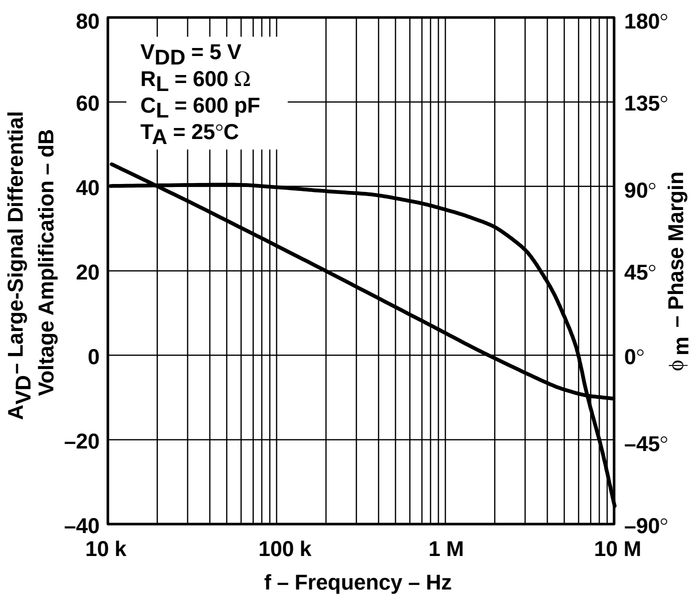


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

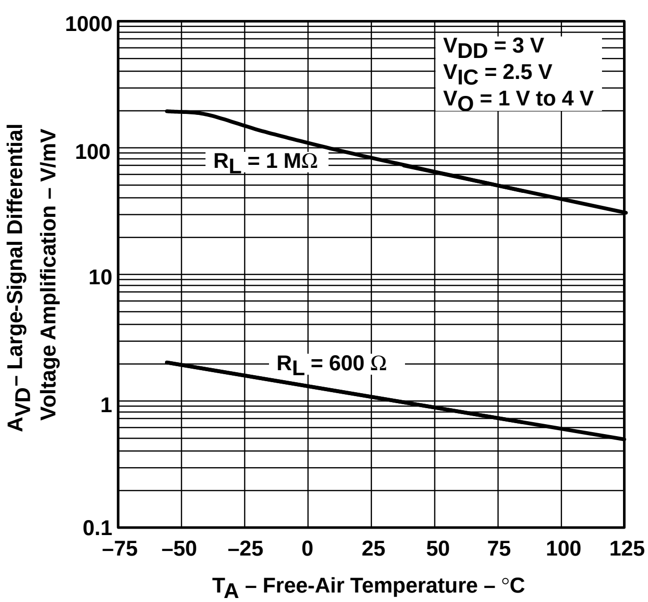


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

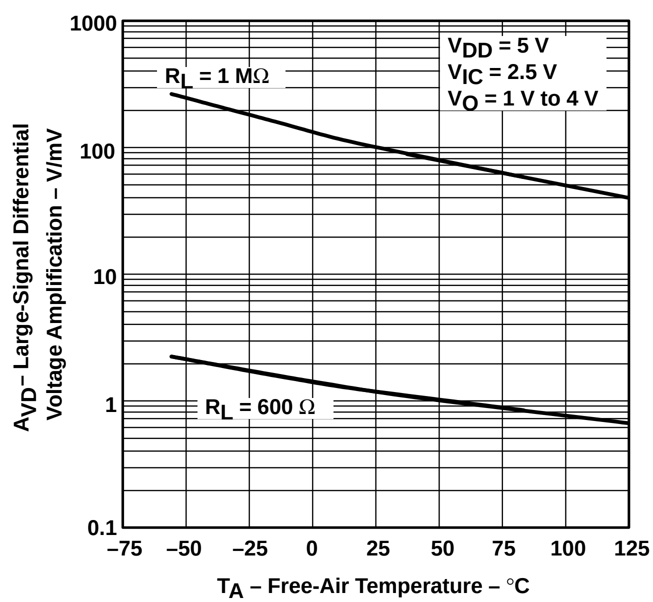


Figure 21

TYPICAL CHARACTERISTICS

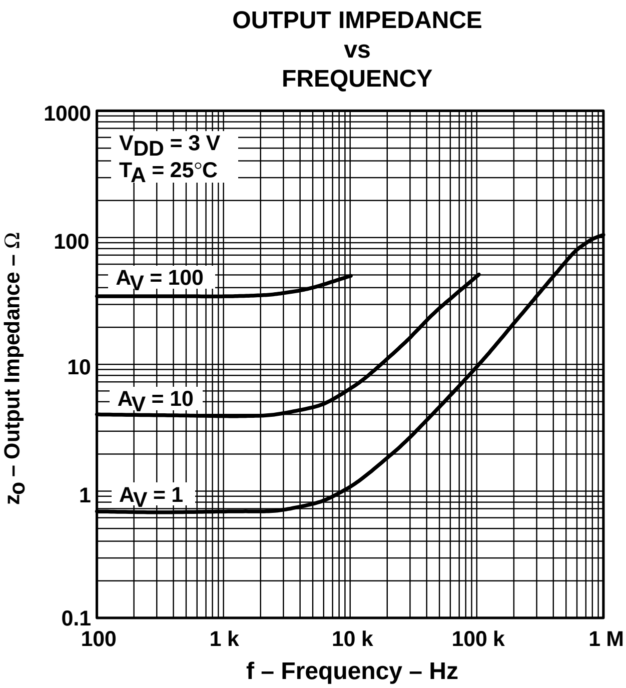


Figure 22

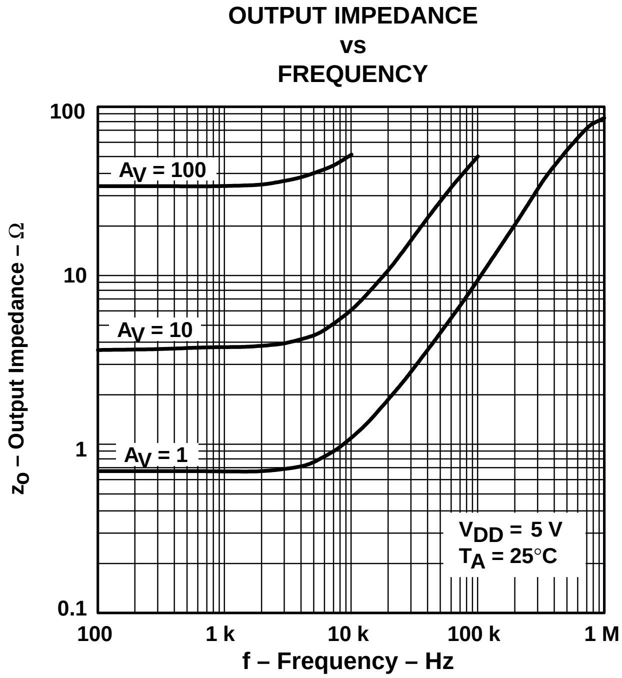


Figure 23

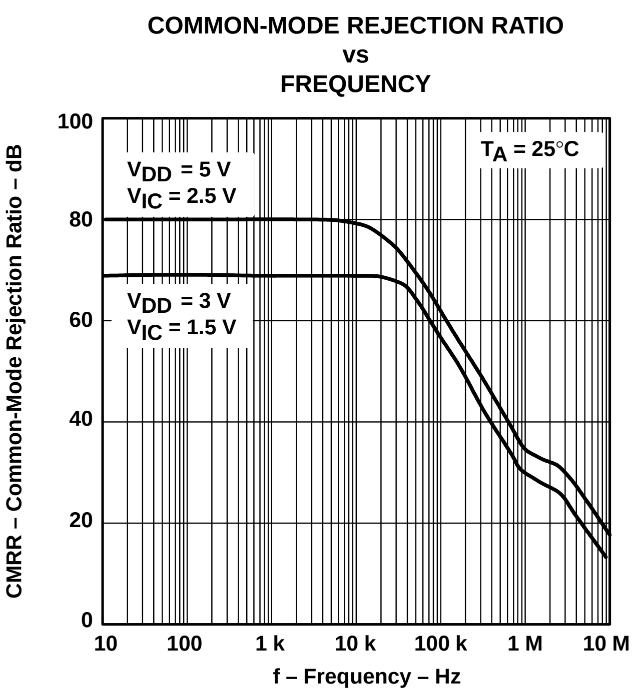


Figure 24

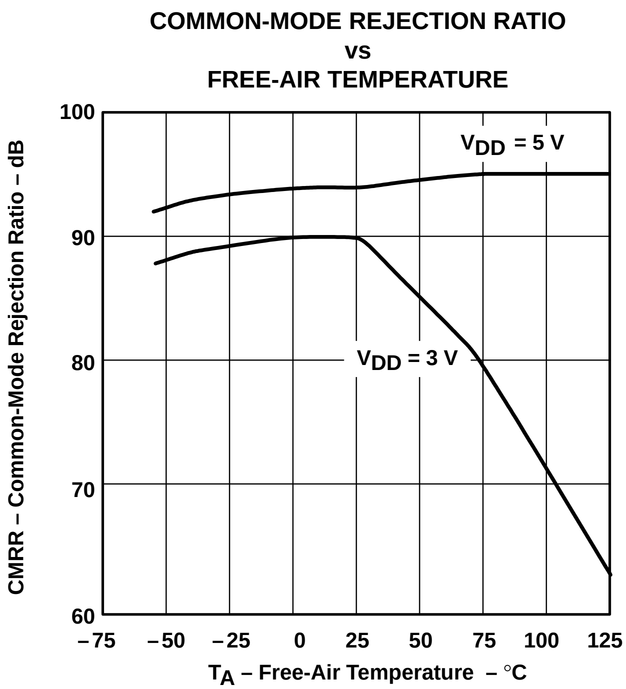


Figure 25

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

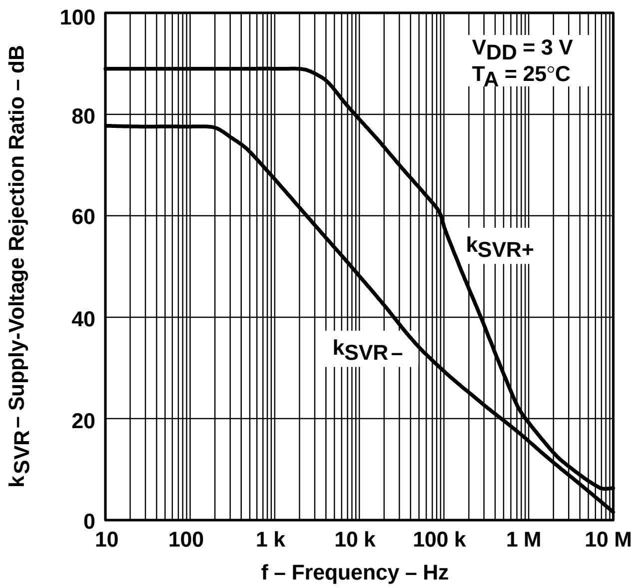


Figure 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

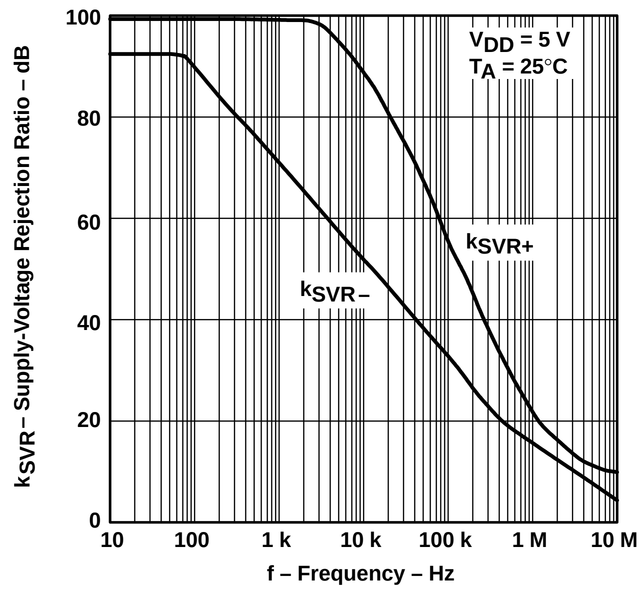


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY-AIR TEMPERATURE

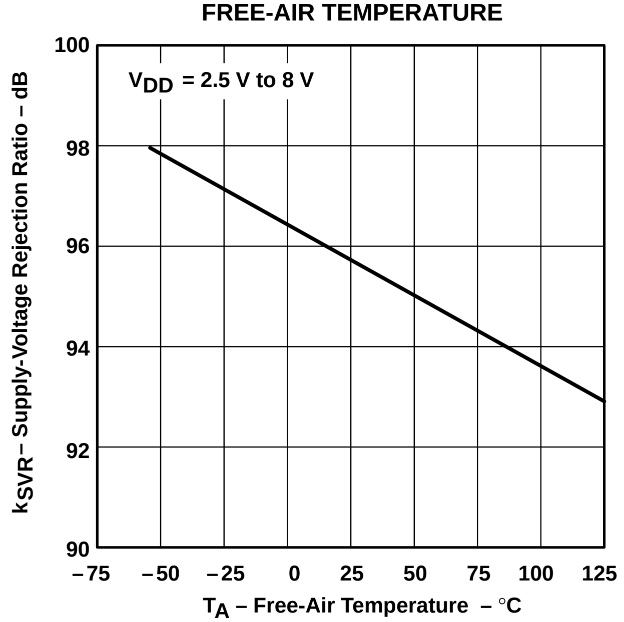


Figure 28

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

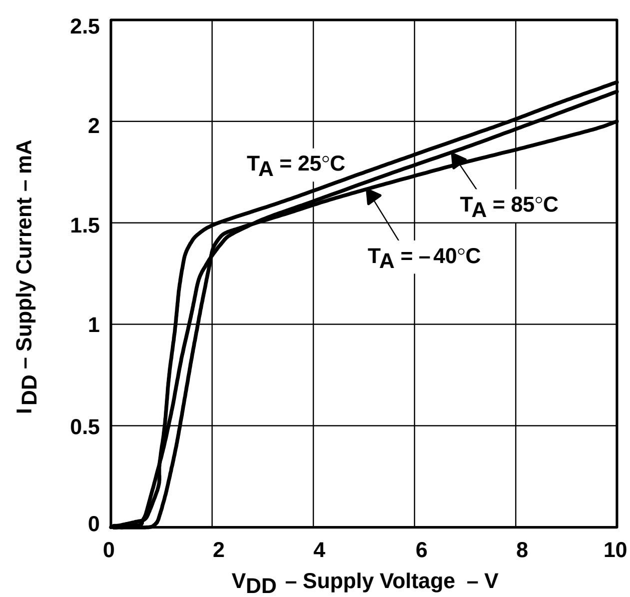


Figure 29

TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD CAPACITANCE

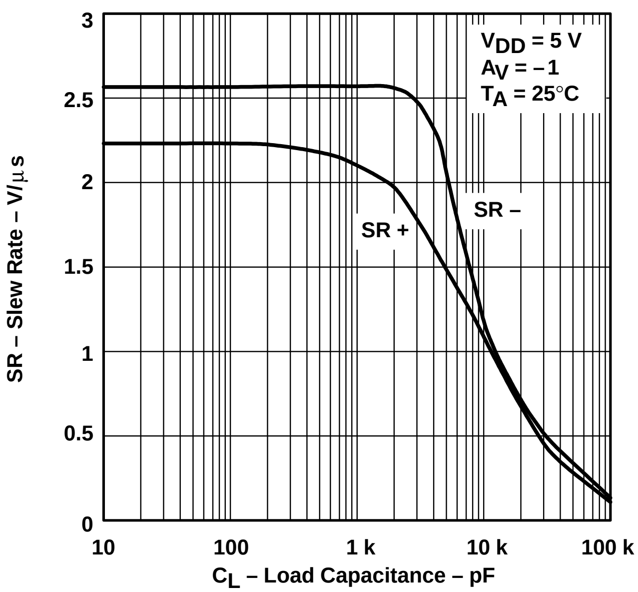


Figure 30

SLEW RATE
vs
FREE-AIR TEMPERATURE

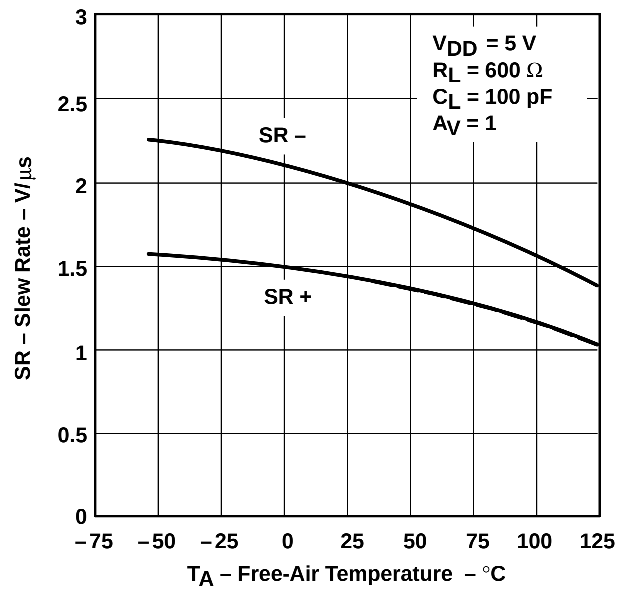


Figure 31

INVERTING LARGE-SIGNAL PULSE RESPONSE

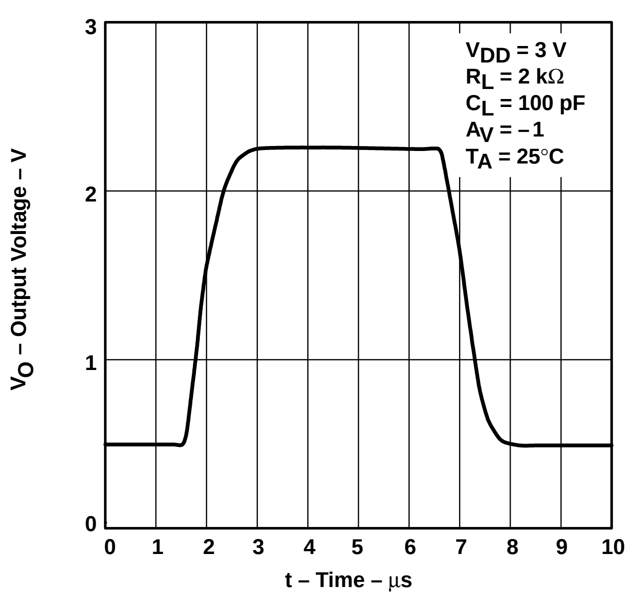


Figure 32

INVERTING LARGE-SIGNAL PULSE RESPONSE

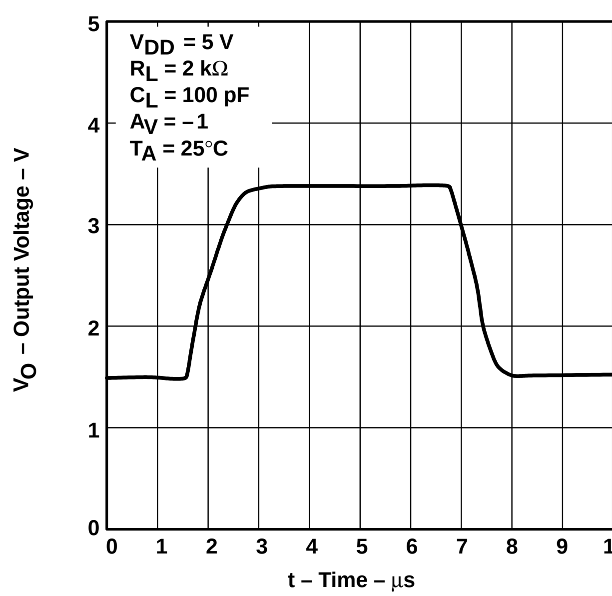


Figure 33

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

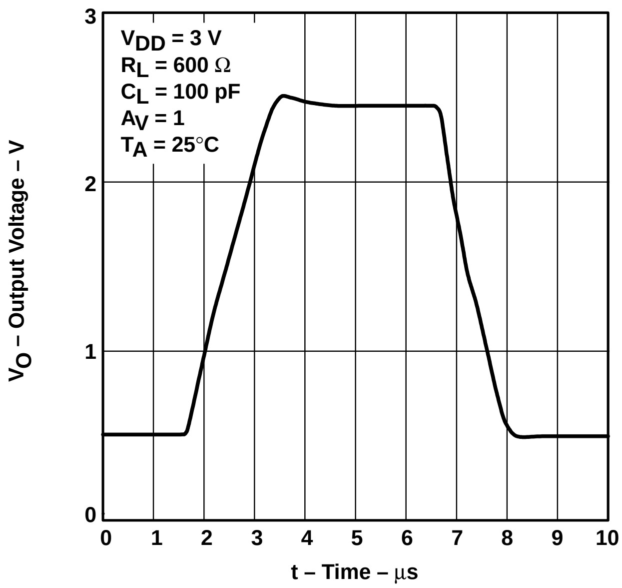


Figure 34

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

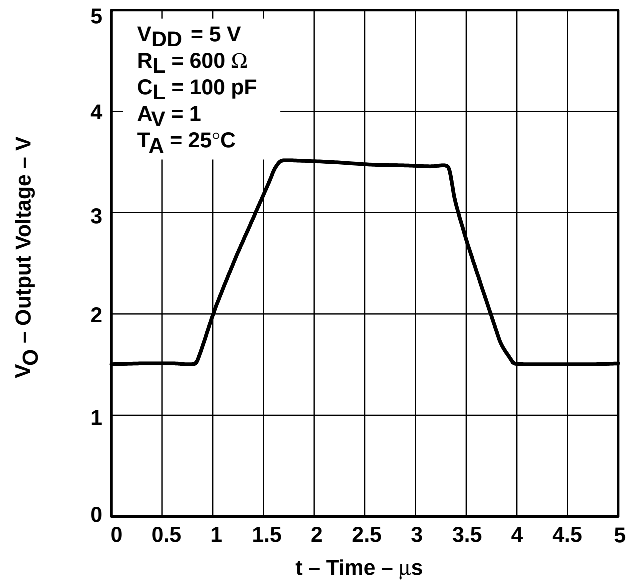


Figure 35

INVERTING SMALL-SIGNAL PULSE RESPONSE

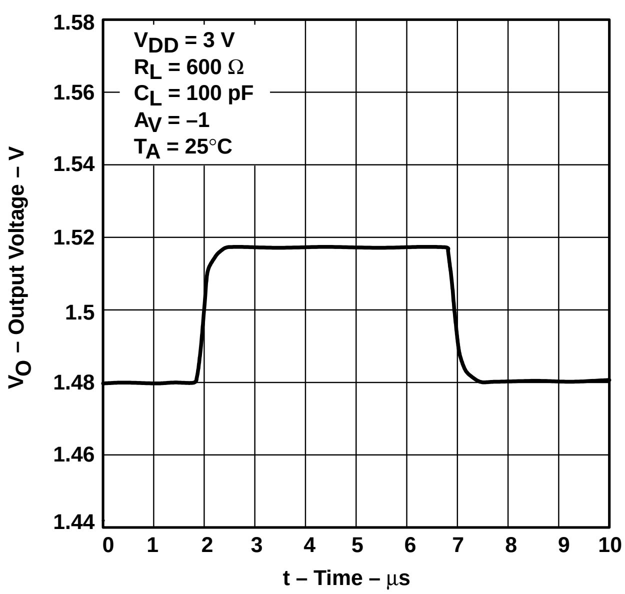


Figure 36

INVERTING SMALL-SIGNAL PULSE RESPONSE

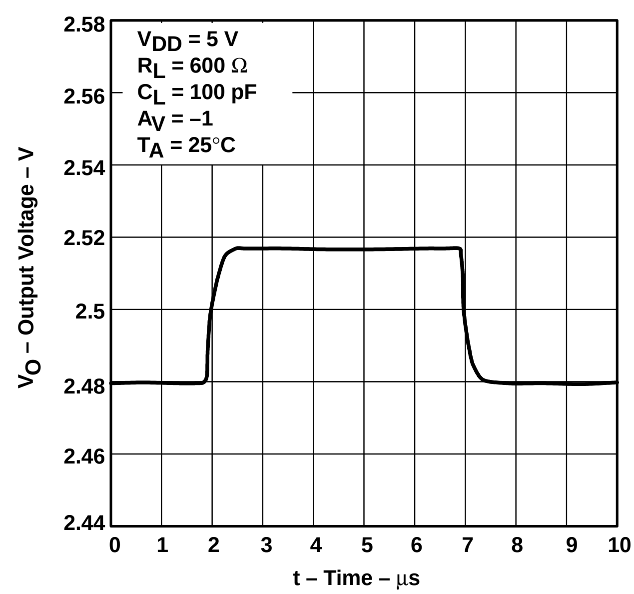


Figure 37

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

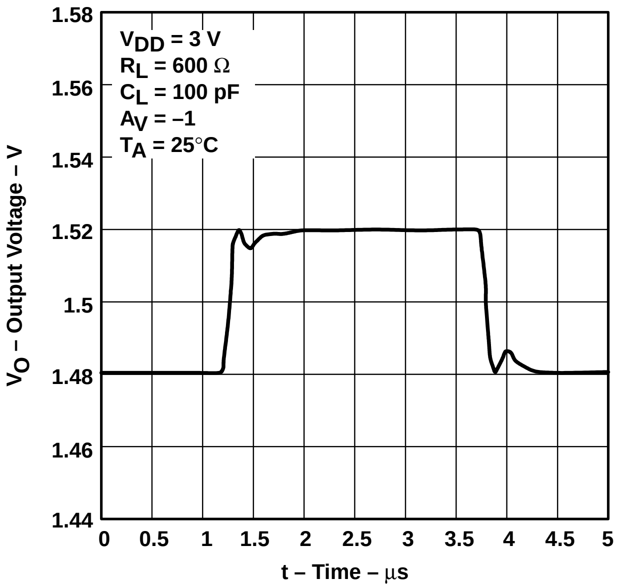


Figure 38

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

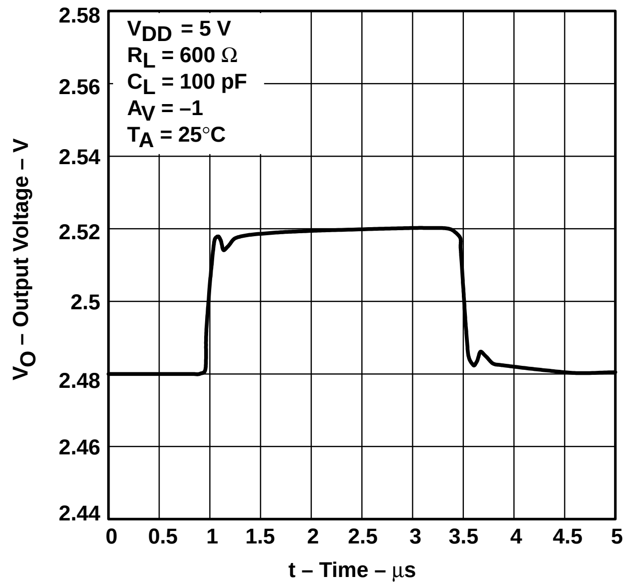


Figure 39

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

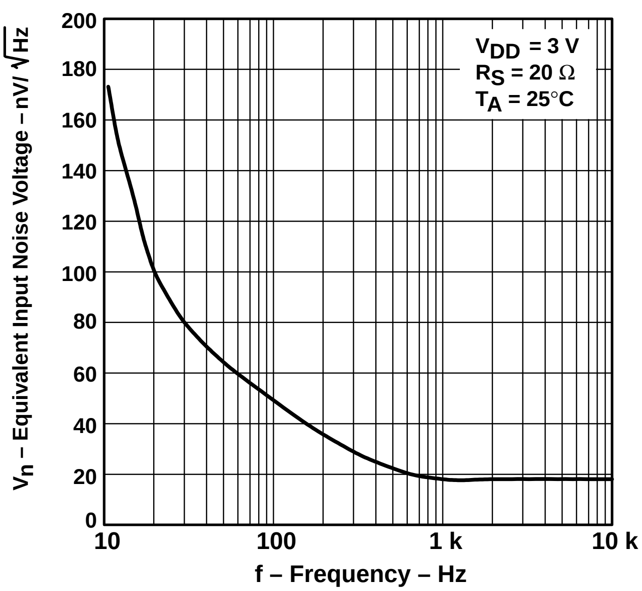


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

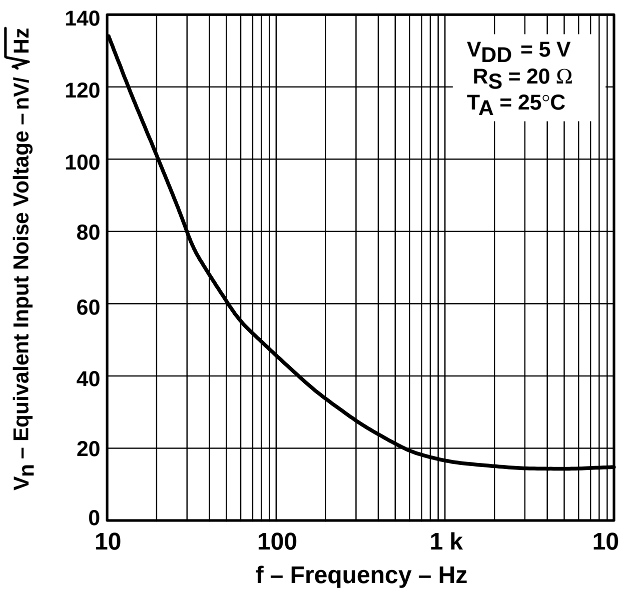


Figure 41

TYPICAL CHARACTERISTICS

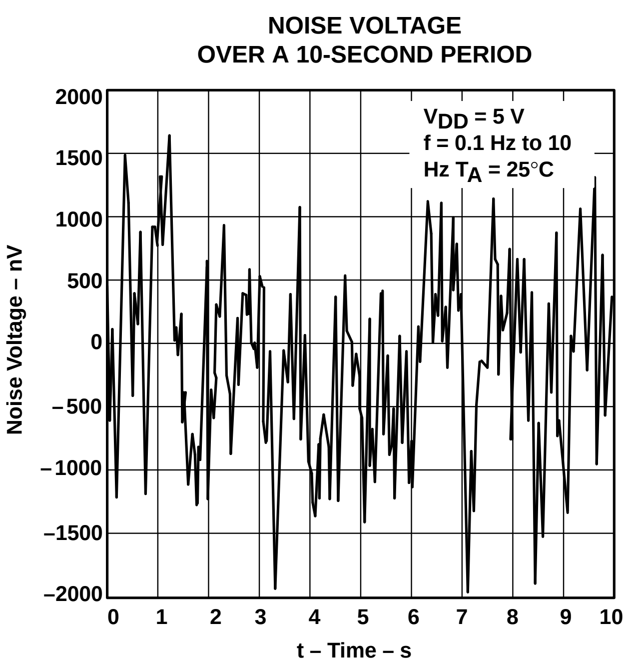


Figure 42

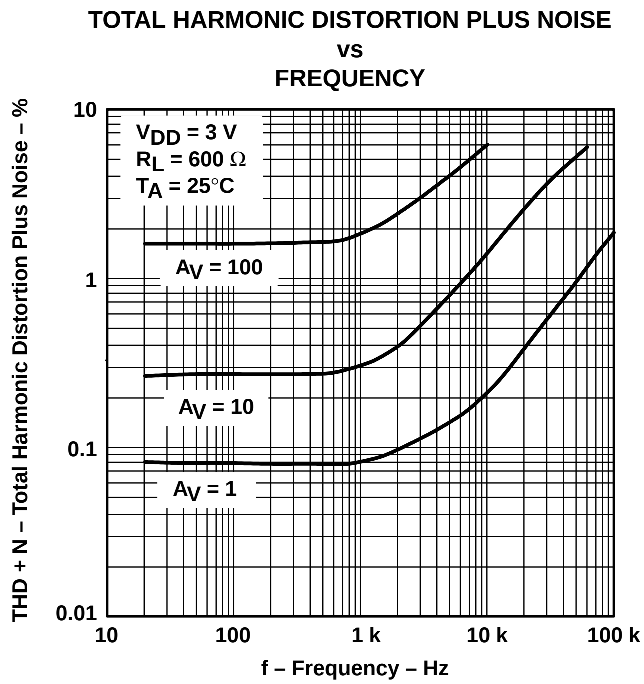


Figure 43

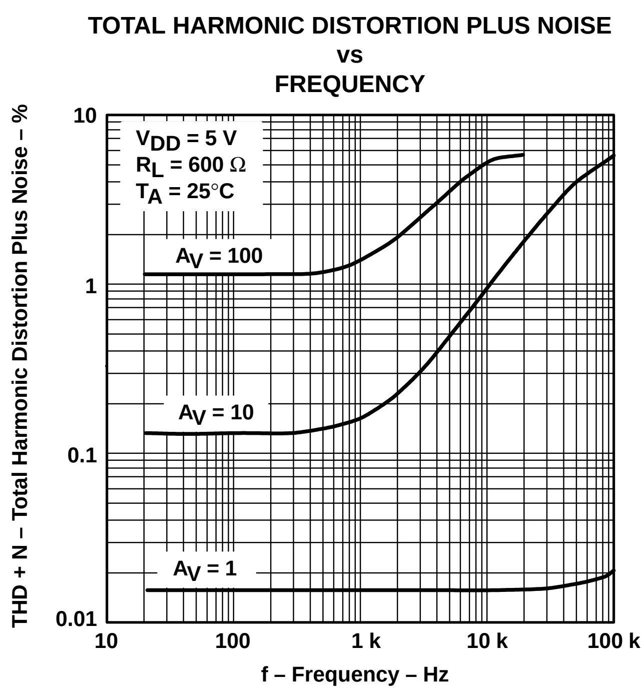


Figure 44

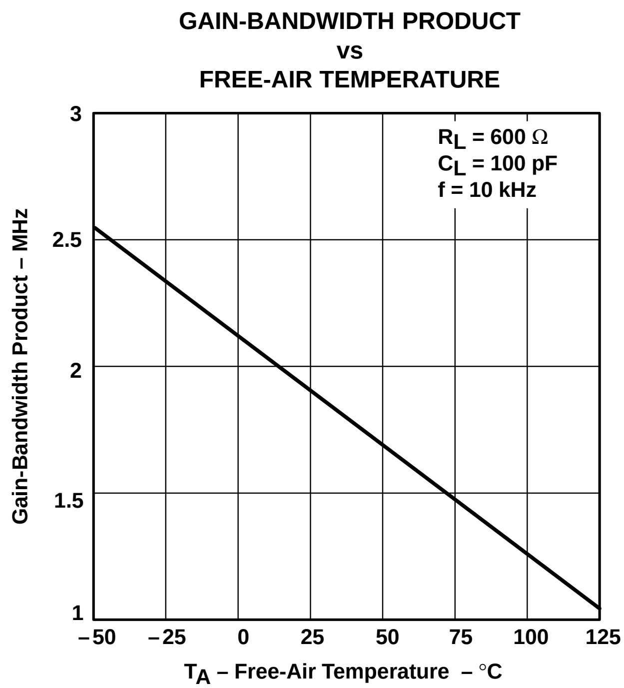


Figure 45

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

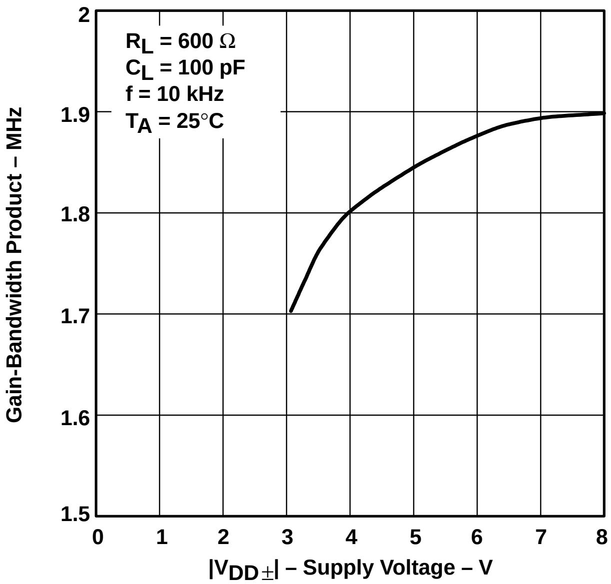


Figure 46

PHASE MARGIN
vs
LOAD CAPACITANCE

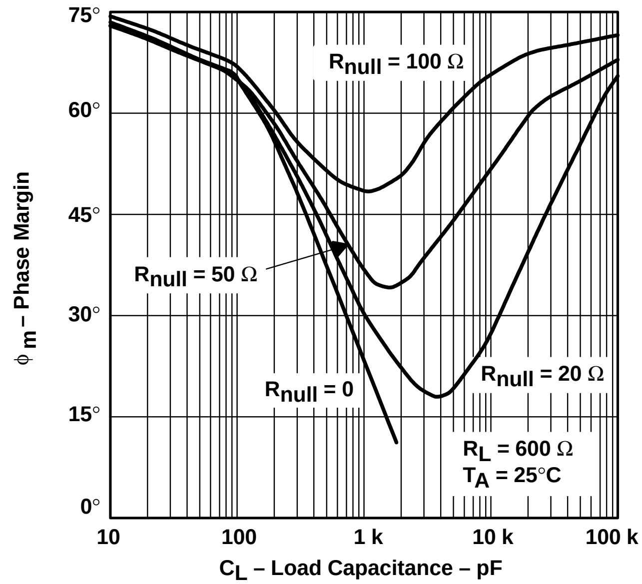


Figure 47

GAIN MARGIN
vs
LOAD CAPACITANCE

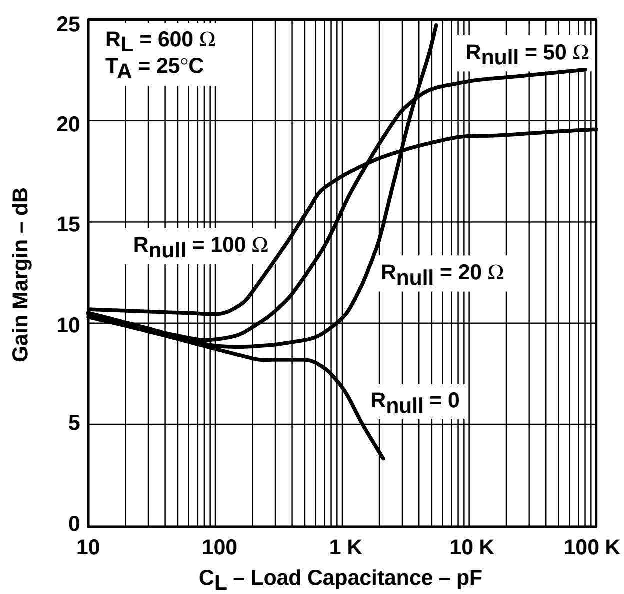


Figure 48

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

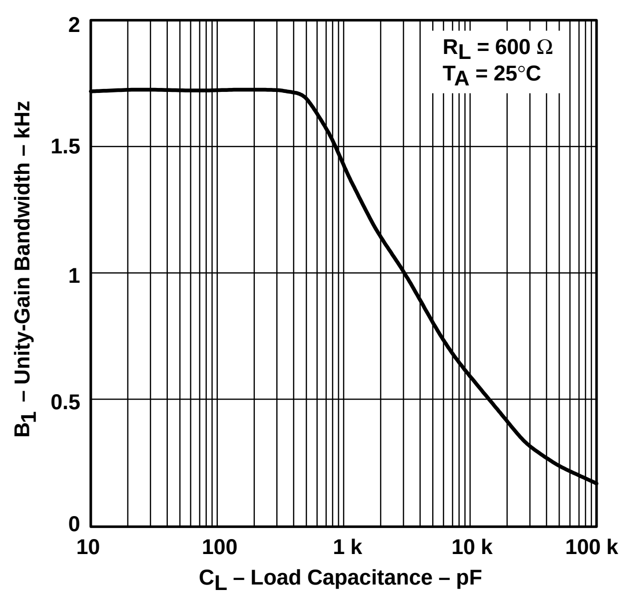


Figure 49

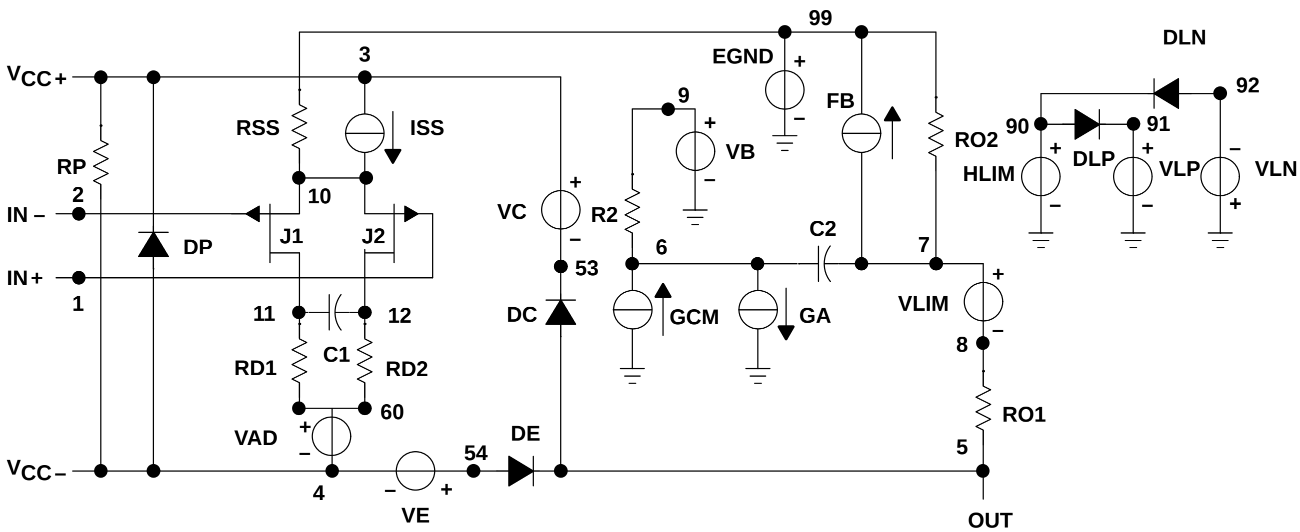
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 53 were generated using the TLV2442 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2442 1 2 3 4 5
C1      11      12      14E–12
C2      6       7       60.00E–12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,) 0 .5 .5
FB      99      0       POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 –1E6 1E6 1E6 –1E6
GA      6       0       11      12 377.0E–6
GCM     0       6       10      99 134E–9
ISS     3       10      DC 216.OE–6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.OE3
RD1     60      11      2.653E3
RD2     60      12      2.653E3
R01     8       5       50
R02     7       99      50
RP      3       4       4.310E3
RSS     10      99      925.9E3
VAD     60      4       –.5
VB      9       0       DC 0
VC      3       53      DC .78
VE      54      4       DC .78
VLIM    7       8       DC 0
VLP     91      0       DC 1.9
VLN     0       92      DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=1.500E–12BETA=1.316E-3
+ VTO=–.270)
.ENDS
```

Figure 50. Boyle Macromodel and Subcircuit

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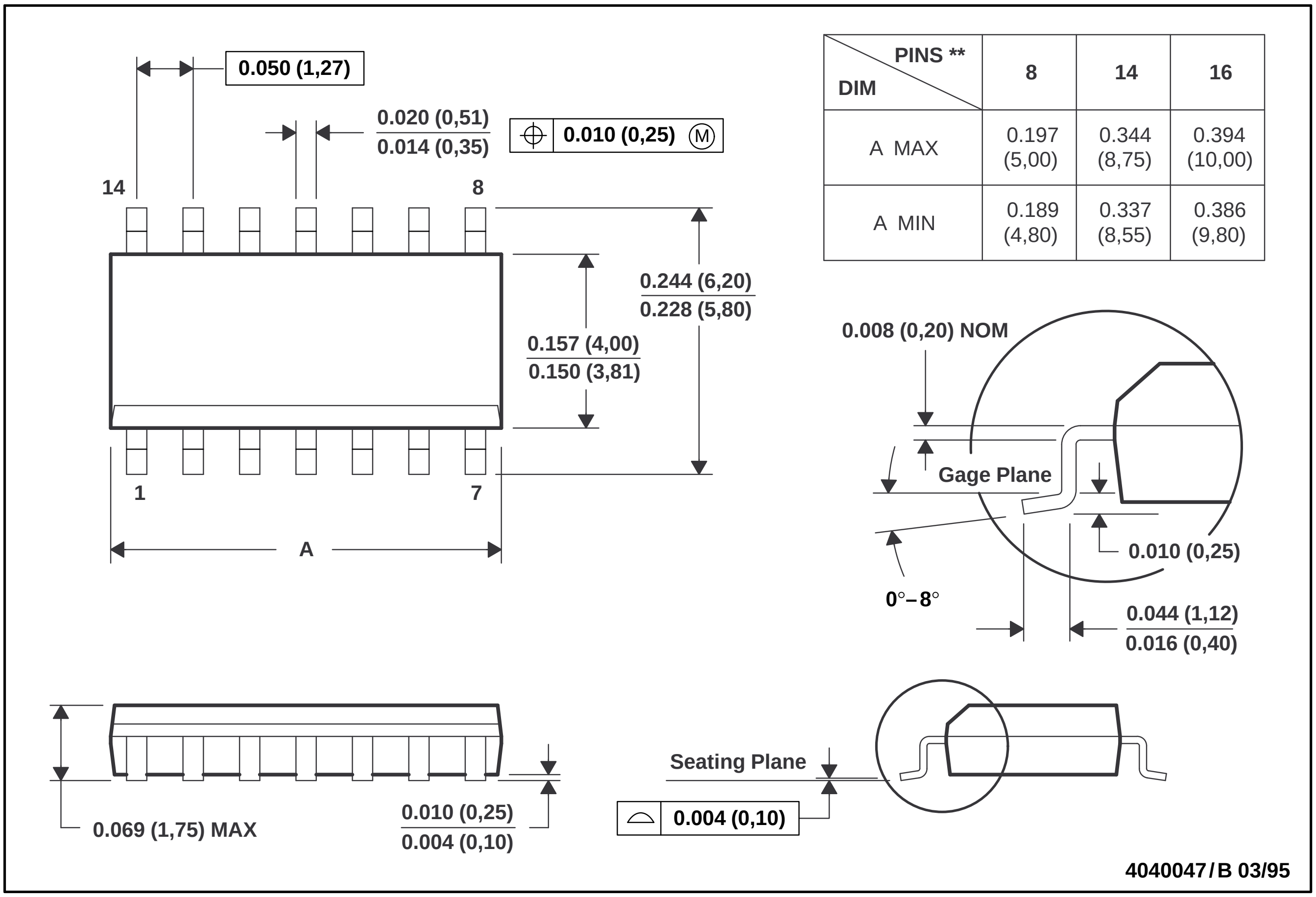
MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



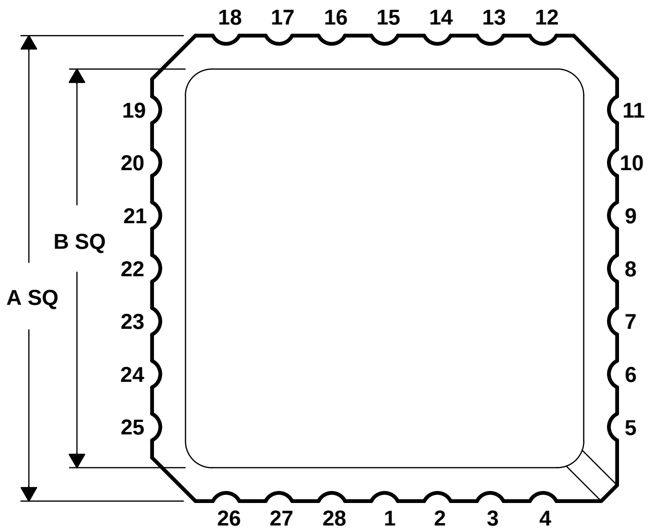
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

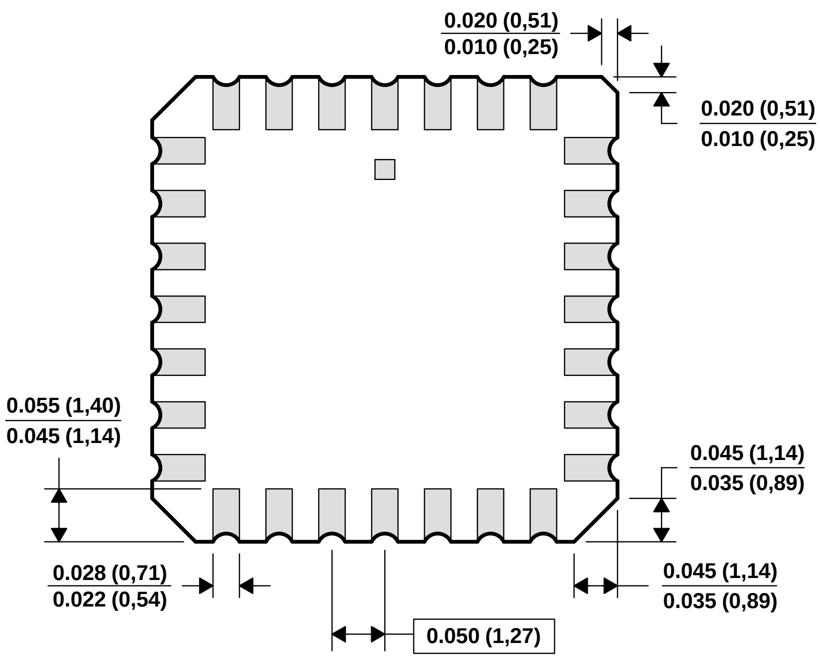
MECHANICAL INFORMATION

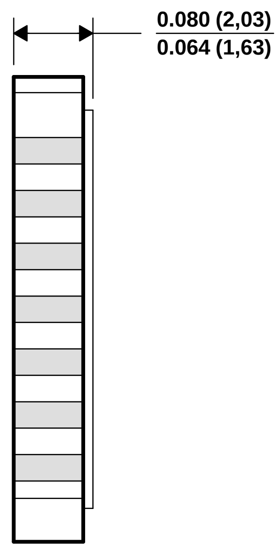
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



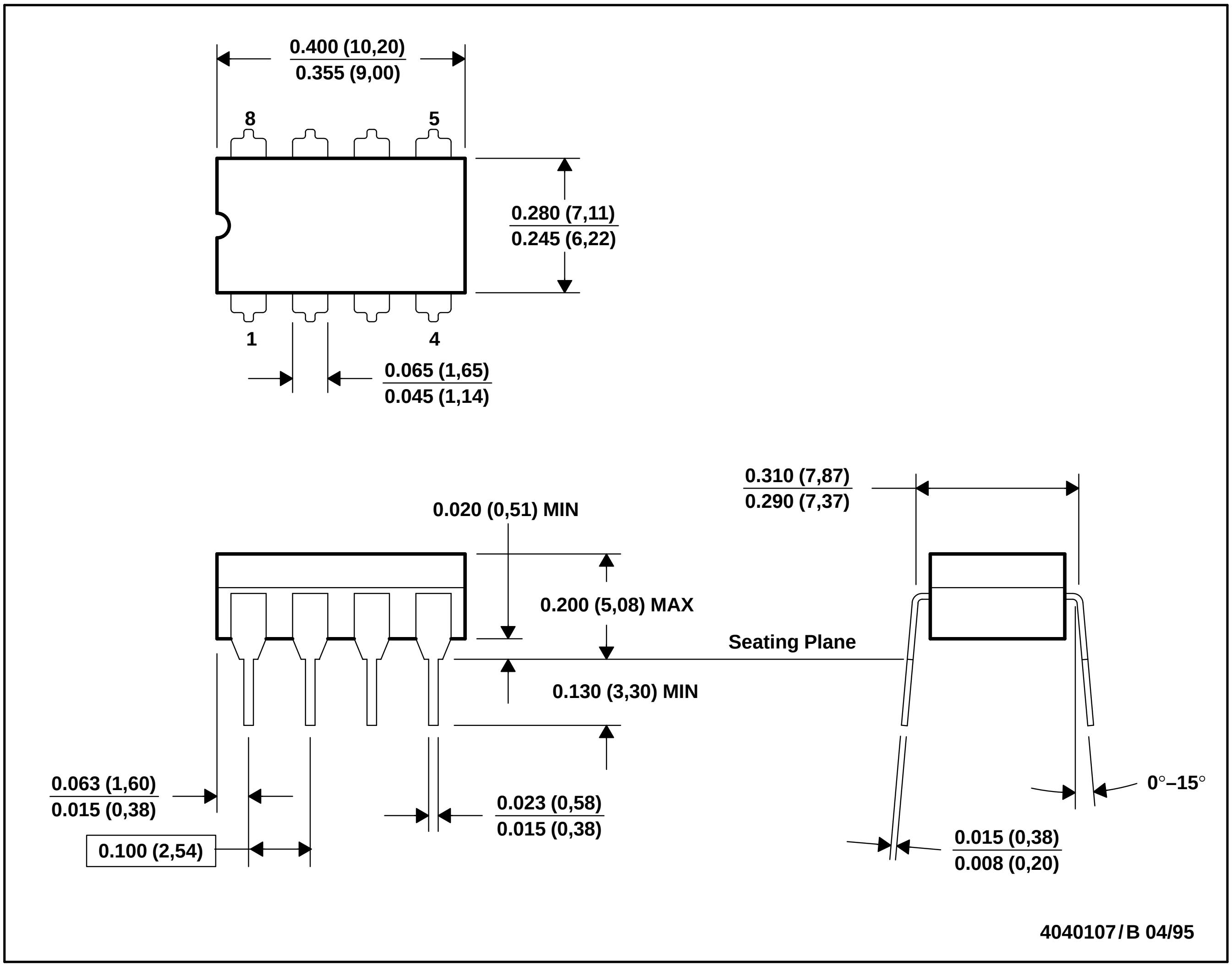


4040140/C 11/95

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**

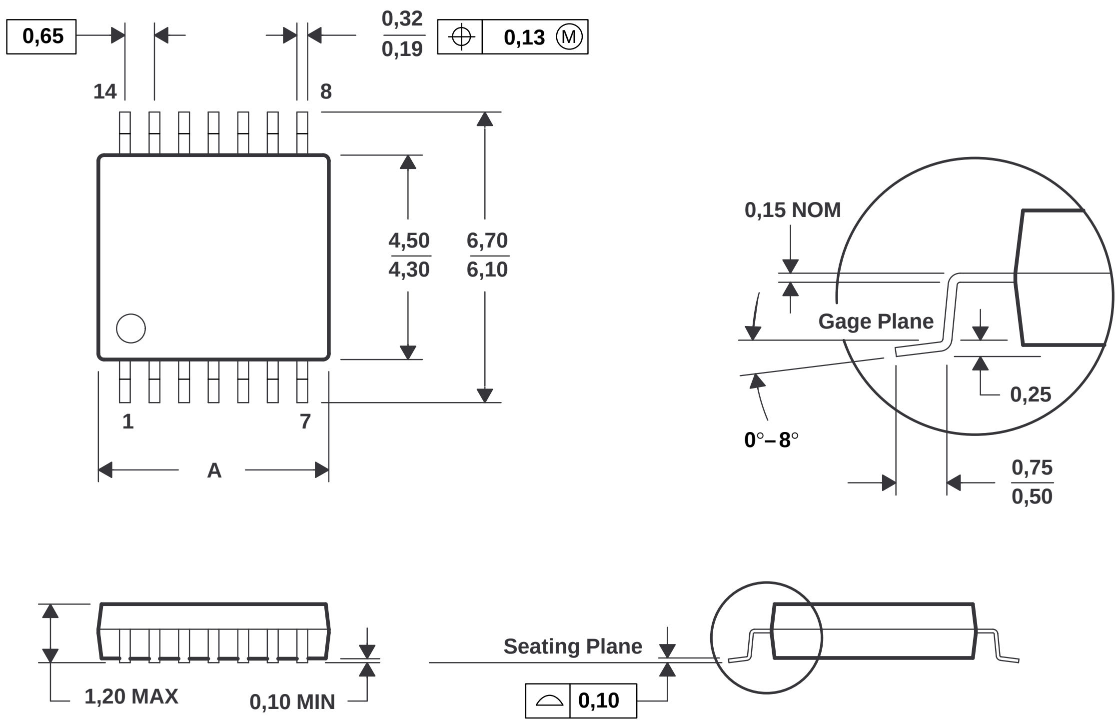


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



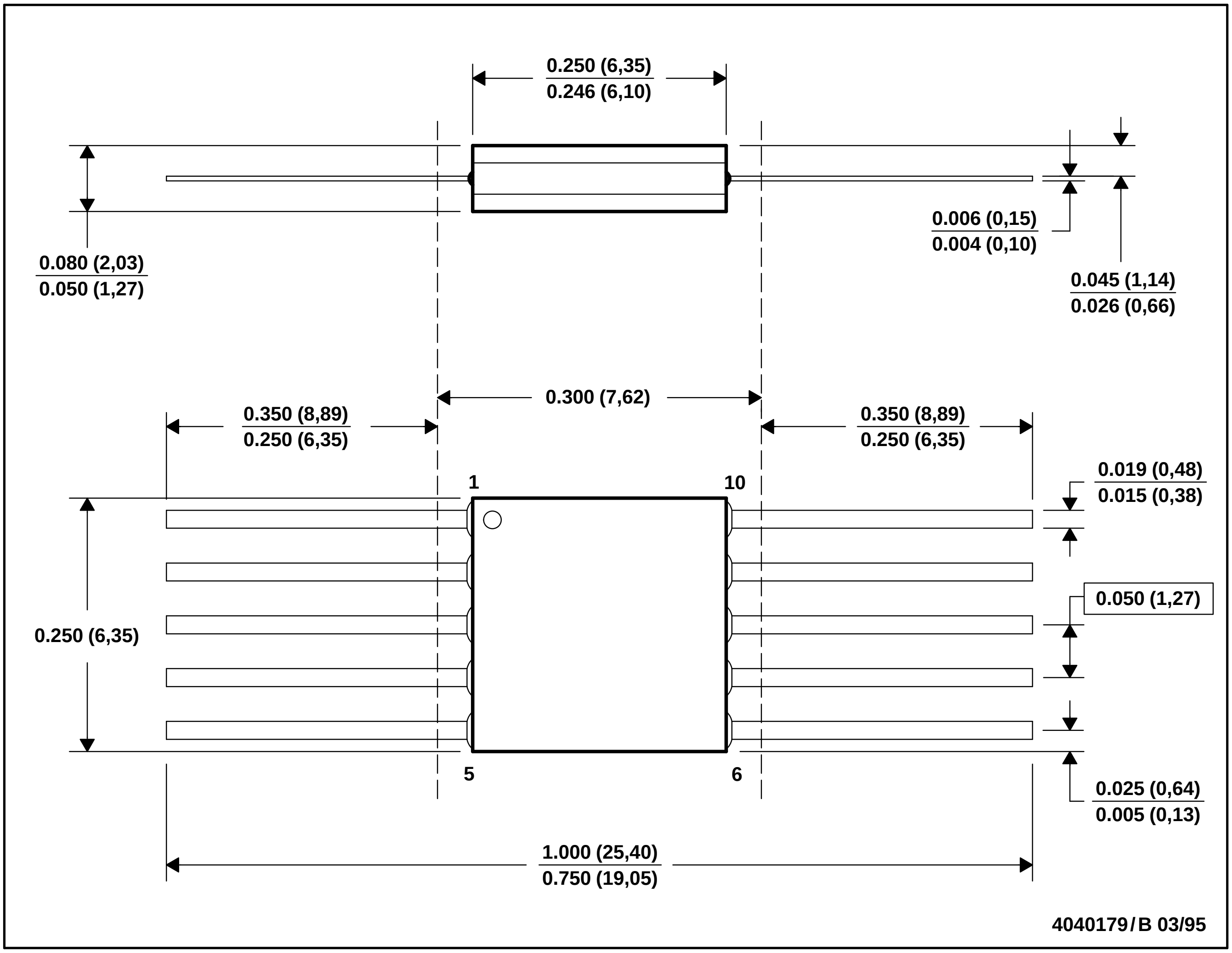
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

MECHANICAL INFORMATION

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA