# Mysteries of the PCM Highway

AMD

***Application Note***

*Most AMD SLAC™ devices transport their digitized voice channels via streams of digital bits called PCM (pulse code modulation) highways. These digital highways carry the encoded voice or modem signals into and out of the linecard part of the system. In this manner, the AMD SLAC devices support systems such as channel banks, digital loop carriers, wireless local loop home side boxes, or central office switch linecards. This application note provides an overview of the PCM highway operation and the various modes in which the PCM highway can operate. Not all AMD SLAC devices support all of the variations discussed in this note. This application note does not include devices utilizing the GCI or IOM-2 protocol and structure.*

## TYPES OF PCM HIGHWAYS

There are two types of PCM highways, differentiated by the direction of data travel, shown in Figure 1.

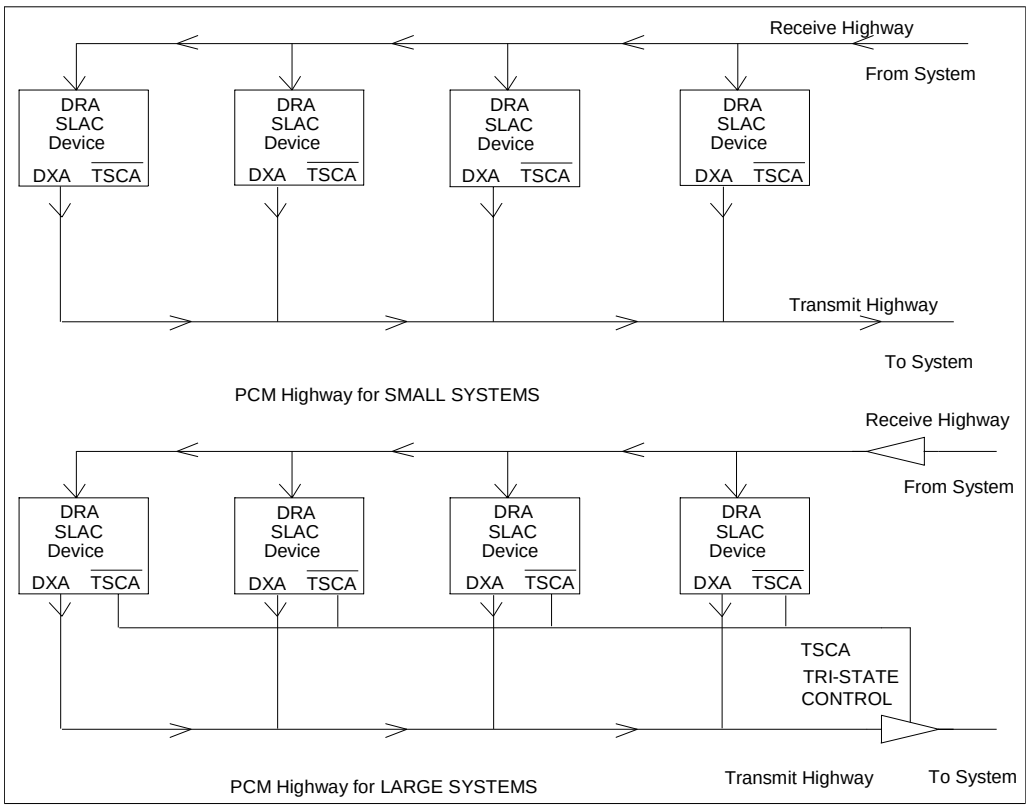


**Figure 1. PCM Highway**

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A Transmit highway from AMD's viewpoint takes data generated by the SLAC devices and transports it to other system devices such as a switch, mux, or radio. The Receive highway carries PCM data to input to SLAC devices from the system. For a very small system, the Transmit highway can directly feed the Receive highway.

Larger systems feed the SLAC device "Transmit" highway output into a transport or switching system block between the Transmit highway and the SLAC device Transmit highway output. In a similar fashion, the transport or switching matrix block feeds the Receive highway SLAC device input. The switching matrix is needed when there are more channels of transmitting devices than there are time slots on one PCM highway. So a switching matrix is created for interconnecting more than one Transmit highway and more than one Receive highway.

## TIME SLOT ZERO

The PCM highways for AMD SLAC devices have their bit rate set by the PCM Clock (PCLK) input to the SLAC devices. A frame sync signal aligns and allows division of data into timeslots of eight bits, shown in Figure 2. AMD SLAC devices can receive data or transmit data in any PCM highway time slot. The number of time slots available depends on the PCM Clock (PCLK) rate used with the SLAC device.

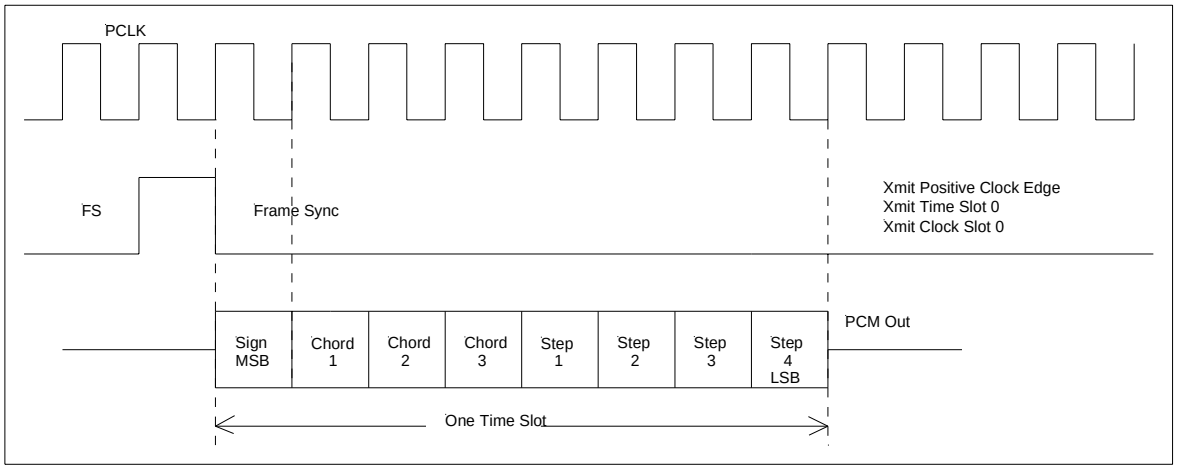


**Figure 2. The First Time Slot (or Time Slot Zero)**

## TIME SLOTS ON A HIGHWAY

For a PCLK (or highway) rate of 2.048 MHz, 32 time slots of eight bits are possible in one frame of data. Each time slot can carry one A-law or μ-law PCM voice channel. A frame of data carries one 8-bit data sample from each channel. The frame of data is defined by the frame synchronization signal occurring every 125 μs. This 8 kHz sample rate and the 2.048 MHz data rate creates the 32 channels or time slots. The microprocessor interface (MPI) in an AMD SLAC device can receive commands to assign any channel of a device to any highway time slot. This software flexibility permits the AMD SLAC device to perform time-division switching. For small switching systems, this capability may be sufficient for the system. Other higher clock rates and lower clock rates can be used, depending on system requirements.

### Broadcasting

In the example shown in Figure 3, any of 32 time slots numbered 0–31 can be used by a SLAC device as a channel for PCM data. This example uses a PCM highway rate of 2.048 MHz. Broadcast of a call progress tone or message occurs when multiple SLAC devices or multiple device channels receive the same time slot data (one source to many listeners). Assigning multiple SLAC device TX channels to the same transmit time slot results in a jumbling of voice data, which generally is not useful because the multiple output drivers in the SLAC devices conflict.

### Dual Highways

Some AMD SLAC devices have dual PCM highways. The dual highway structure allows redundant highways for systems requiring fault tolerance. A channel can be switched to the second highway if a system fault blocks use of the primary highway. The dual highway structure allows small systems to have an element of space switching to accommodate higher traffic loads due to internet modem access. Because SLAC devices with dual highways have access to both highways, the number of timeslots available to them doubles. This allows increased occupancy, caused by the longer connection times occurring with modem access to the internet.

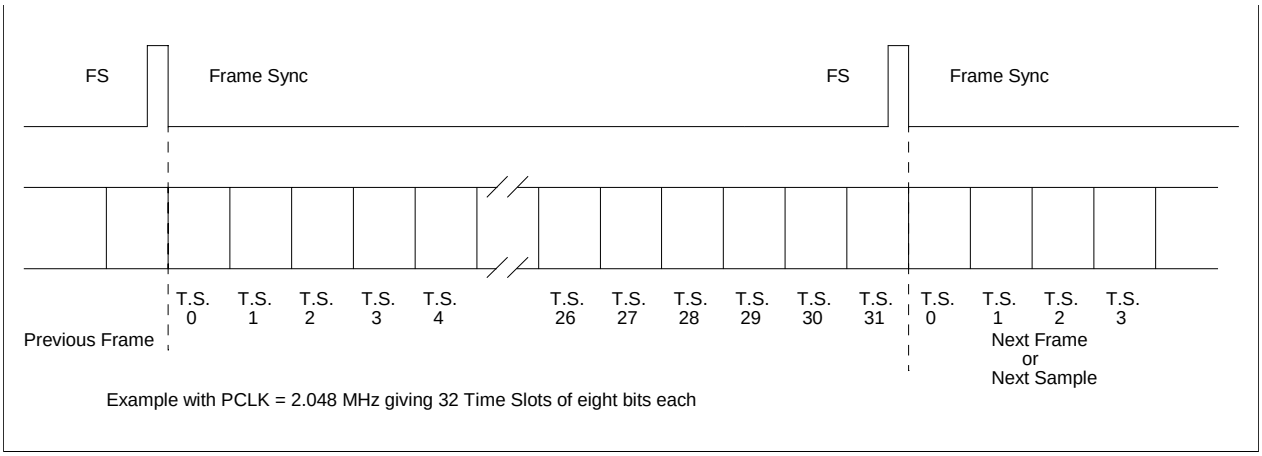


**Figure 3. PCM Highway Time Slots**

## Rate of the PCM Highway

Table 1 lists common PCLK rates and the number of time slots for that PCLK rate. The 128 kHz rate is not available on QSLAC™ devices because that would limit the device to two channels. Some SLAC devices support other rates such as integer multiples of 1.536 MHz. See individual device data sheets for details of a specific device and package.

**Table 1. PCLK Rates vs. Number of Time Slots**

| PCM Clock Rate (MHz) | Number of Time Slots (Channels) |
|---|---|
| 0.128 | 2 |
| 0.256 | 4 |
| 0.512 | 8 |
| 1.024 | 16 |
| 1.544 | 24 |
| 2.048 | 32 |
| 3.088 | 48 |
| 4.096 | 64 |
| 6.176 | 96 |
| 8.192 | 128 |

## Structure of a Time Slot

Each time slot consists of eight bits. These eight bits normally consist of an MSB (most significant bit), which is the sign bit, three chord or range bits, and four steps-within-a-chord bits. (Details of these eight bits are discussed later in this application note.) Figure 4 shows the relative timing of the receive input and transmit output of a typical SLAC device.

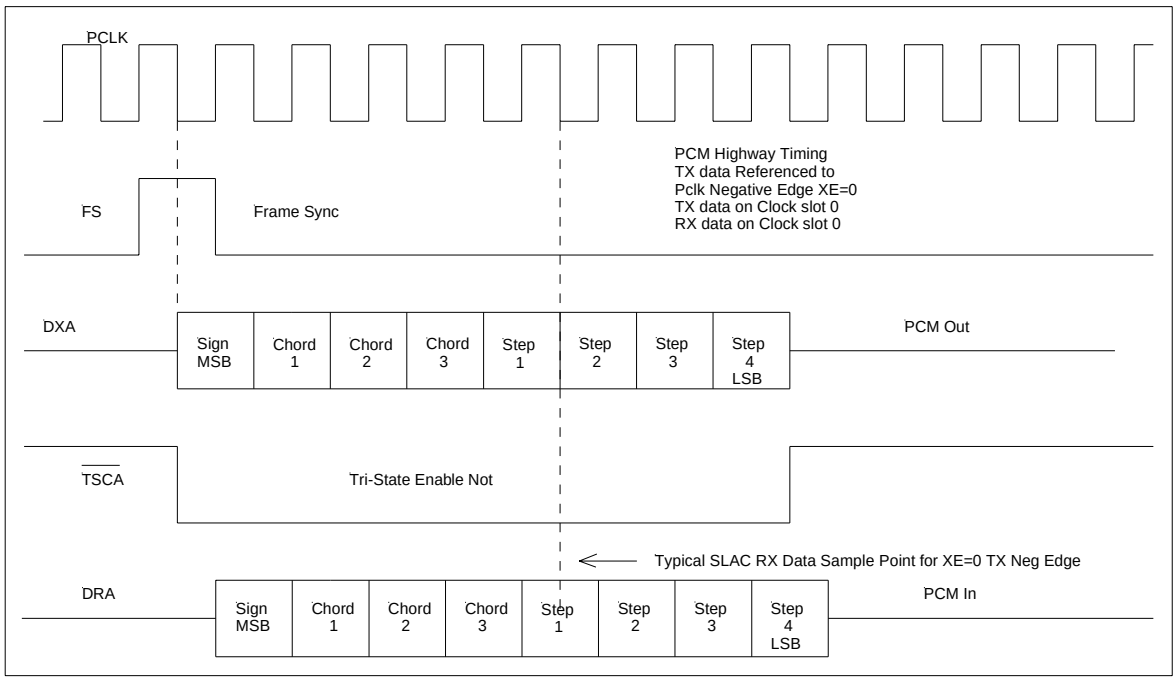


**Figure 4. PCM Highway Timing (Referenced to Negative Edge of PCLK)**

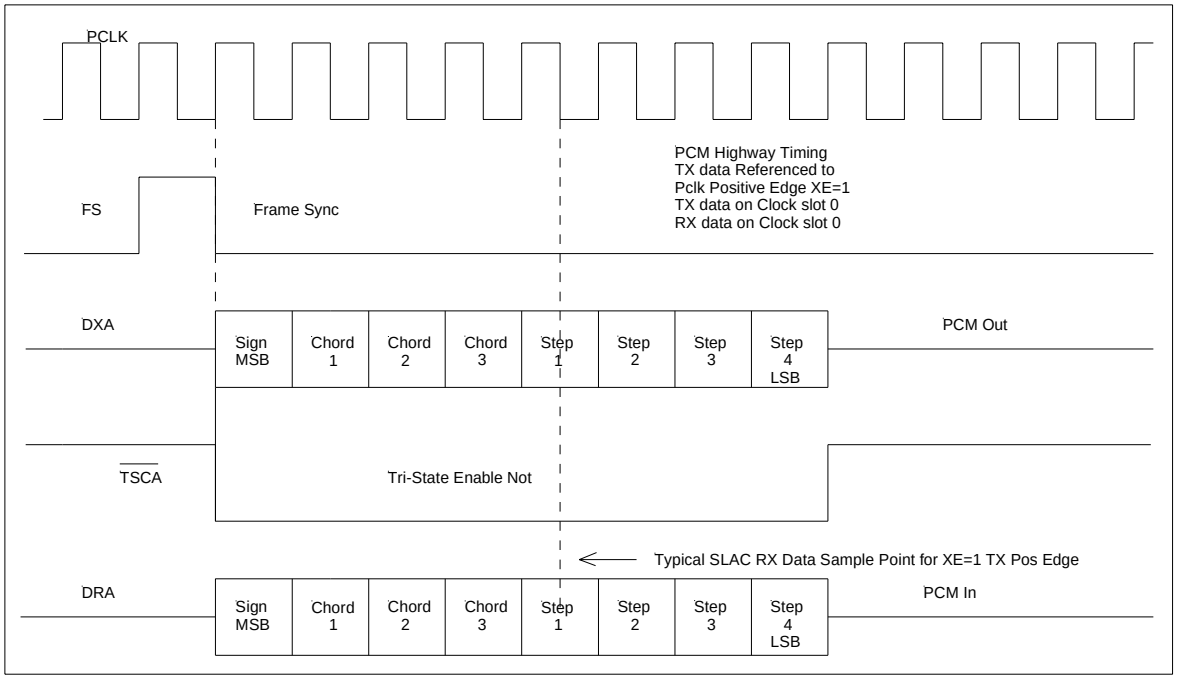


**Figure 5. PCM Highway Timing (Referenced to Positive Edge of PCLK)**

To make clear the effect of the clock edge setting, Figure 4 shows the PCM for XE = 0 or Transmit data referenced to the Negative PCLK edge. Figure 5 shows the PCM for XE = 1 or Transmit data referenced to the Positive PCLK edge. Note that the clock edge setting controls when the PCM transmit data is output, but does not change the receive input sampling time. The examples in Figure 4 and Figure 5 show the SLAC devices assigned to time slot zero or the first time slot after the frame sync signal. A new signal has been introduced. This active low time slot control enable allows a tri-state buffer to activate when the SLAC device outputs data. Typically, this is done in larger systems or in systems with hot-insert of linecards.

## Frame Synchronization Differences

AMD SLAC devices differ from most dumb codec parts in their simpler and more flexible timing. The older non-programmable parts have PCM output synchronized to a Transmit Frame Sync signal. Their PCM input is synchronized to a Receive Frame Sync signal. The applied frame sync signals must often be offset in time to deal with clock skew or bit delays in the system.

The AMD SLAC devices utilize only one frame sync signal to inform the device when time slot zero occurs for both receive and transmit. Software registers for both receive and transmit are separately programmable for each channel's timeslot assignment. This reduces system logic and wiring. Four channels of a non-programmable device must have four transmit frame sync signals and four receive frame sync signals applied. The AMD QSLAC device has only one frame sync signal applied and is programmed to its time slot assignment.

## Timing Skew Problems

Many systems have a master frame signal that differs from the framing signal used by the linecards because of timing skews or logic functional delays. The AMD SLAC devices are programmed to select or use a specific clock edge. This generally saves some inversion gates and their delays in the clock sub-system. AMD SLAC devices have a clock slot feature that allows the input or output to be offset from the zero time slot defined in relation to the framing signal applied. The clock slot permits 0–7 clock cycles of delay from the position defined by the applied frame synchronization signal. Figure 6 shows the application of clock slot assignment for the timing.

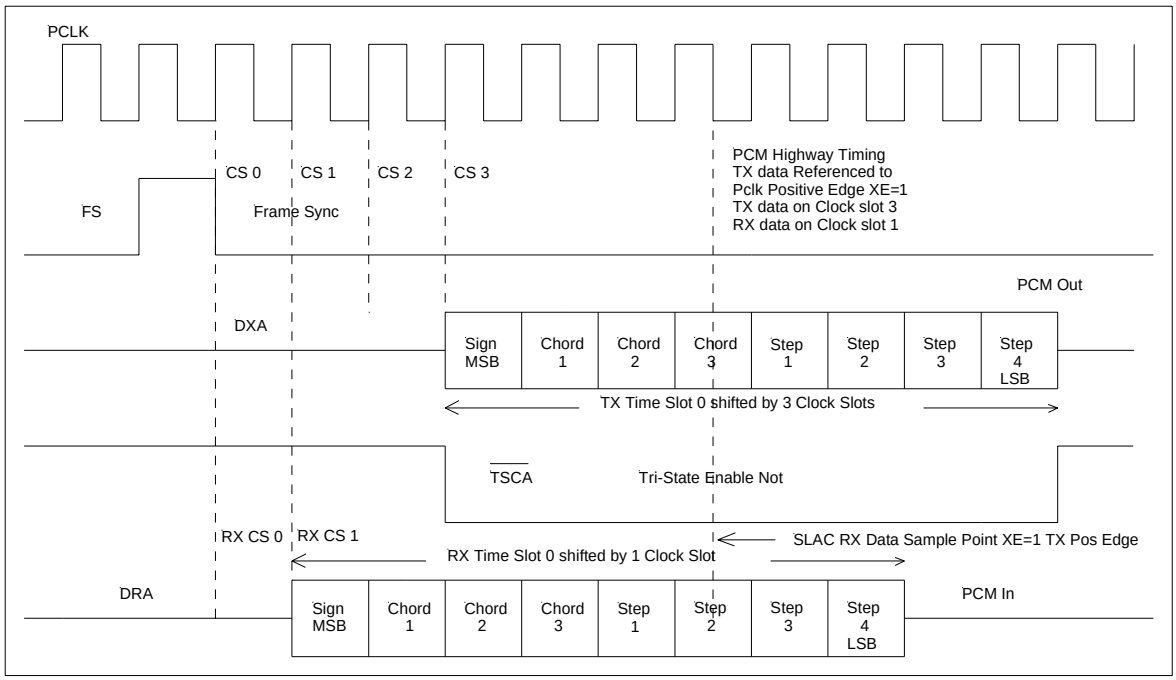


**Figure 6. Clock Slots**

Figure 6 shows a typical output and input of PCM from a SLAC device with skewed TX and RX PCM highways. Figure 4 shows the PCM data with the negative edge of PCLK selected as the timing reference. No clock skew or clock slot adjustment is shown. Figure 5 is the same as Figure 4, but with the positive clock edge as a reference. Figure 6 shows the PCM input and output set for reference to the positive PCLK edge using clock slot settings. The transmit timing is set for clock slot three, which delays the output by three clock cycles. The receive timing is set for one clock cycle of delay or one clock slot. This is clock slot One.

## Companded PCM Modes

Each time slot consists of eight bits. These eight bits normally consist of an MSB (most significant bit) or sign bit, three chord or range bits, and four steps-within-a-chord bits.

Figure 7 shows the sign, step, and chord bits of the byte or octet of PCM voice data. The 8-bit PCM data represents a wider dynamic range of voice signals than is possible with a linear code. This is made possible by compressing the voice signal before releasing the data from the SLAC device, and expanding the data into a full range voice signal as the data is taken into the SLAC device. A-law and μ-law companded modes (compressed-expanded) are included in the SLAC devices.

Figure 8 shows a typical compression slope. Instead of a linear slope relating input to output, a compressed slope uses an exponential curve. This means that an LSB (least significant bit) change represents a larger voltage input for bigger signals than for smaller signals. The step bits divide a chord segment into 16 steps. The chord bits select which of the eight chords, in the positive or negative quadrant, are to be divided.

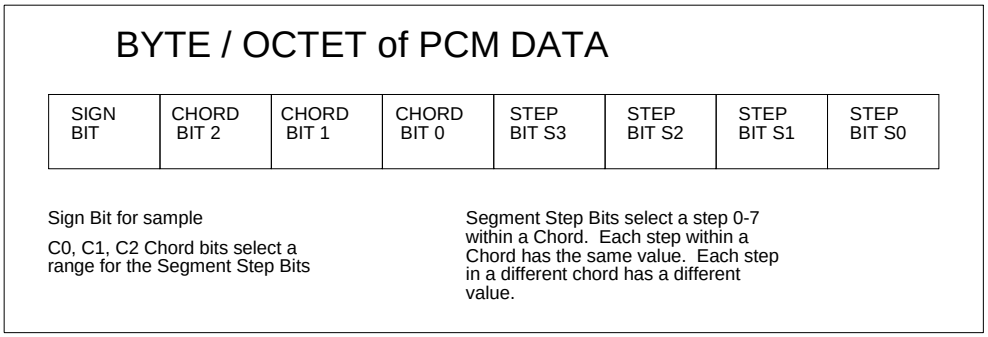


**Figure 7. Voice PCM Data**

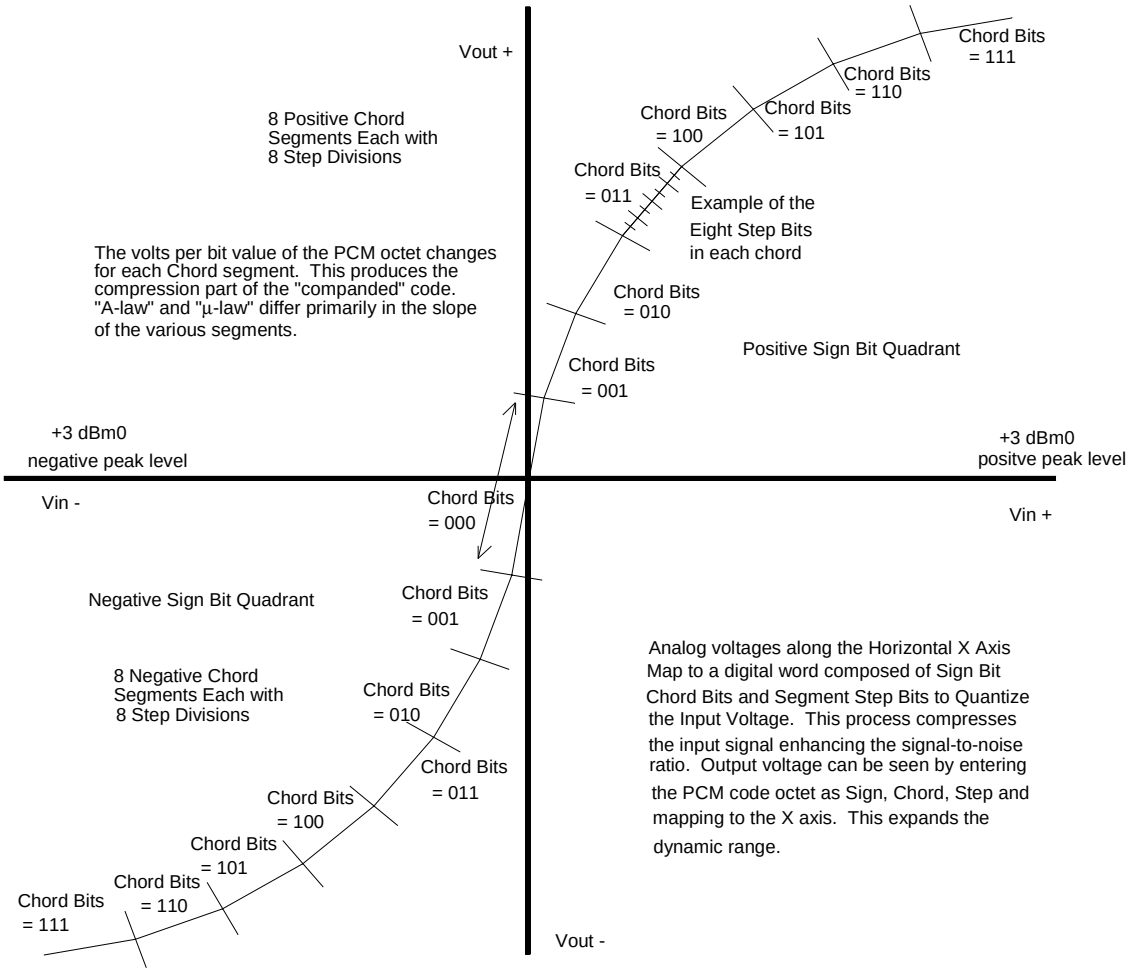


**Figure 8. Chords and Step Bit Meaning**

## A-Law PCM Output

There are two companded PCM modes supported in all AMD SLAC devices. Most countries, except North America and Japan, use the A-law mode. The most significant difference between A-law and μ-law is the even bit inversion used in A-law. This inversion increases the one's bit density in transmission systems. A-law coding produces excellent signal-to-noise ratio performance with signals in the normal range of volume (between –25 and 0 dBm). The code produces a slightly lower signal-to-noise ratio for weak signals. Table 2 shows code values for full scale (FS) and zero input.

**Table 2. A-Law Code (Includes Even Bit Inversion)**

| | Sign Bit | C1 Bit | C2 Bit | C3 Bit | Step 1 Bit | Step 2 Bit | Step 3 Bit | S4 LSB |
|---|---|---|---|---|---|---|---|---|
| +FS In | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| +0 V | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 V | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| FS In | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

## μ-Law PCM Output

The second companded PCM mode supported in all AMD SLAC devices is μ-law. The μ-law mode is used by North America and Japan. The most significant difference between μ-law and A-law is that μ-law does not use the even bit inversion used in A-law. μ-law coding provides excellent signal-to-noise ratio performance with signals in the weak range of volume (signals below –25 dBm). The μ-law code is not quite as good in terms of signal-to-noise ratio for loud signals as the A-law. Table 3 shows code values for full scale (FS) and for zero input.

**Table 3. μ-Law Code**

| | Sign Bit | C1 Bit | C2 Bit | C3 Bit | Step 1 Bit | Step 2 Bit | Step 3 Bit | S4 LSB |
|---|---|---|---|---|---|---|---|---|
| +FS In | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| +0 V | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 V | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| FS In | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Linear Mode Output

Some AMD SLAC devices have a linear mode of operation. This mode does not use A-law or μ-law PCM, but a linear code. The SLAC device outputs and it expects an input of a 16-bit binary word that has a sign bit and a 15-bit magnitude. The QSLAC device uses two contiguous time slots. For example, an assignment of time slot 0 that uses time slots 0 and 1: assigning of Time 1 uses time slots 1 and 2. Do not assign the last time slot because doing so produces an unwanted corruption of data. The Linear mode is useful for systems converting to ADPCM (Adaptive Delta PCM) or other codes. Figure 9 shows the two contiguous bytes of data on the PCM highway.

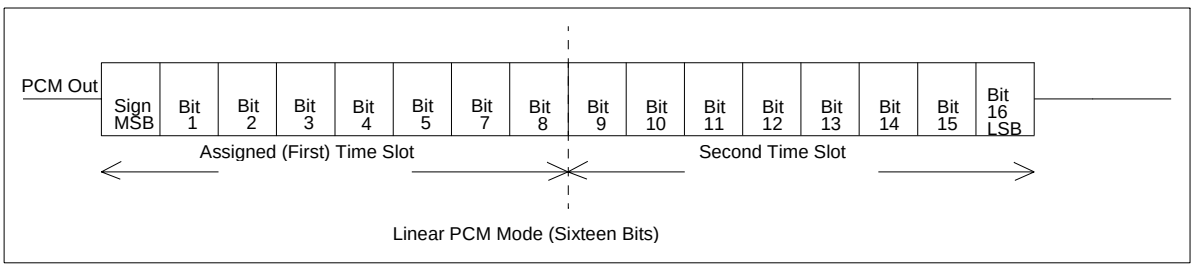


**Figure 9. Linear Mode Time Slots**

## Signaling on the Highway Mode

The QSLAC device also has another operational mode. Some systems process the signaling information bits with a microprocessor other than the normal MPI microprocessor. Some systems have a requirement for through supervision instead of the more common link-by-link supervision. These systems make the signaling data travel via the PCM highway so that all links can see the data simultaneously. Figure 10 shows how the QSLAC device sends the supervision data in the contiguous timeslot following the A-law or µ-law PCM voice data.

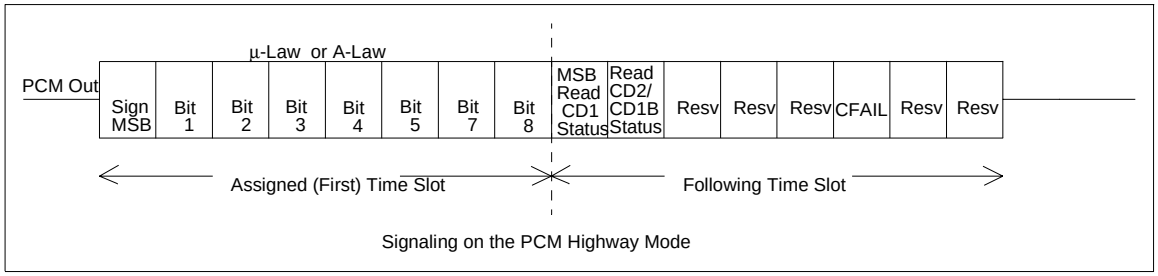


**Figure 10. Signaling on the PCM Highway**

## CONCLUSION

The flexible PCM highway operation and many modes of operation for AMD SLAC devices permit many ways to use SLAC devices in systems with differing requirements. The PCM highway is not just a simple bus to move voice data, but offers many different schemes for interface to telephony systems.