Am79C432A
ISM PhoX™ Controller for Digital Cordless Telephones
Technical Manual

1997

AMD

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CHAPTER

1 OVERVIEW

1.1 GENERAL DESCRIPTION

The Am79C432A PhoX™ Controller is a highly integrated, low-voltage implementation of the baseband functions needed by digital cordless telephones on a single chip, including audio processing, protocol control, data formatting, and peripheral functions.

The PhoX chip implements a 32 kbit/s voice channel and a 1-, 2-, or 16 kbit/s control channel between the handset and the base station. Under the control of the on-chip 8051-class microcontroller, the Formatter performs all of the protocol requirements as well as baseband transmission and reception.

Baseband transmit data is available unfiltered as a Non-Return to Zero (NRZ) pseudo-digital signal, which is passed to the external RF transceiver for filtering and transmission. Data can also be filtered on-chip to provide analog Gaussian minimum-shift key (GMSK) output for external RF transceivers that require this format.

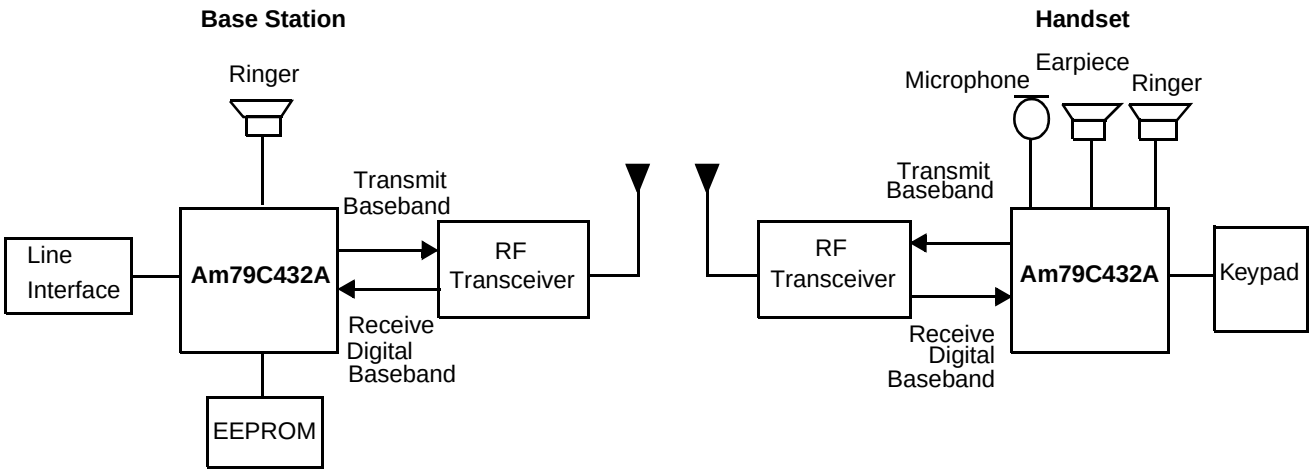
The voice channel is a 32 kbit/s ADPCM (Adaptive Differential Pulse Code Modulation) stream. The PhoX controller converts analog voice input at the microphone interface into ADPCM format and converts ADPCM received data into analog output at the earpiece or loudspeaker output. The device also provides digitally generated DTMF and ringing tones.

The Am79C432A incorporates many peripheral functions necessary for digital cordless telephones. For example, it has a 36-key keypad scanner, a serial port for interfacing to EEPROMs or serial LCDs, and a host of multifunction ports.

The brain of the PhoX chip is the 80C32T2, an 8051-class 8-bit microcontroller, which, with appropriate software, controls the audio path and services the various on-chip peripherals. The on-chip 1.25 Kbyte static RAM is used for variable storage. For software development, the chip interfaces directly to standard 8051 in-circuit emulators in Emulation mode.

The Am79C432A is designed for power management in a battery-operated environment. It has a low power dissipation while operating over a 2.7 to 3.6 V supply. The chip also includes a very low power Shutdown mode. For battery support, there is a battery-level measurement facility.

Figure 1-1 System Architecture



License

The Am79C432A PhoX device is covered by patents owned or controlled by the Common Air Interface Founders Group. AMD's license to such patents extends to use of the Am79C432A PhoX device. For information concerning additional applications, interested parties should contact:

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1.2 DISTINCTIVE CHARACTERISTICS

- Performs protocol, data formatting, audio processing, and peripheral functions for digital cordless telephones
- May be used in the base station or the handset
- Power and battery management features to extend battery life:
  - — Full CMOS design and low voltage operation
  - — Battery monitor to protect the cordless operation
- On-chip 8051-class microcontroller controls all functions
- Special Digital Formatter features:
  - — Link controller which performs all data transmission and reception
  - — Baseband I/Q GMSK modulator
  - — Receive signal strength indicator for channel scanning
  - — Fade detection and management
  - — Improved timing and symbol recovery
- Special audio features:
  - — ADPCM codec compliant with CCITT G.721
  - — DTMF generator
  - — Flexible audio multiplexing and gain control
  - — Includes 16 Ω speaker driver and a microphone interface
  - — Ringing tone generator
- Other on-chip peripheral functions include:
  - — 1.25 KByte static RAM (includes 256 bytes internal data space)
  - — 24 KByte mask-programmable ROM
  - — Serial port for EEPROM, LCD or synthesizer control
  - — 36-key scanner for dialing and special function keys
  - — Up to 10 general-purpose output ports
  - — Watchdog timer
  - — Clock Double mode for the microcontroller
- Other features:
  - — Peak-detect hardware to allow the implementation of a handsfree near full-duplex speakerphone capabilities
  - — Enhanced RSSI with peak detect hardware
  - — Antenna diversity control
- Built-in power management features:
  - — 2.7 V to 3.6 V low-power operation
  - — Low active power consumption, 24 mW
  - — Super low power Shutdown mode, 108 µW

- Battery-level detection

- Test and development features:
  - In-circuit 8051 emulator support for code development
  - Numerous test paths and loopbacks for bit error rate, continuity, and performance testing
  - Continuous transmit RF spectral measurement and modulator bypass features
- 84-pin PLCC package

Figure 1-2 Block Diagram

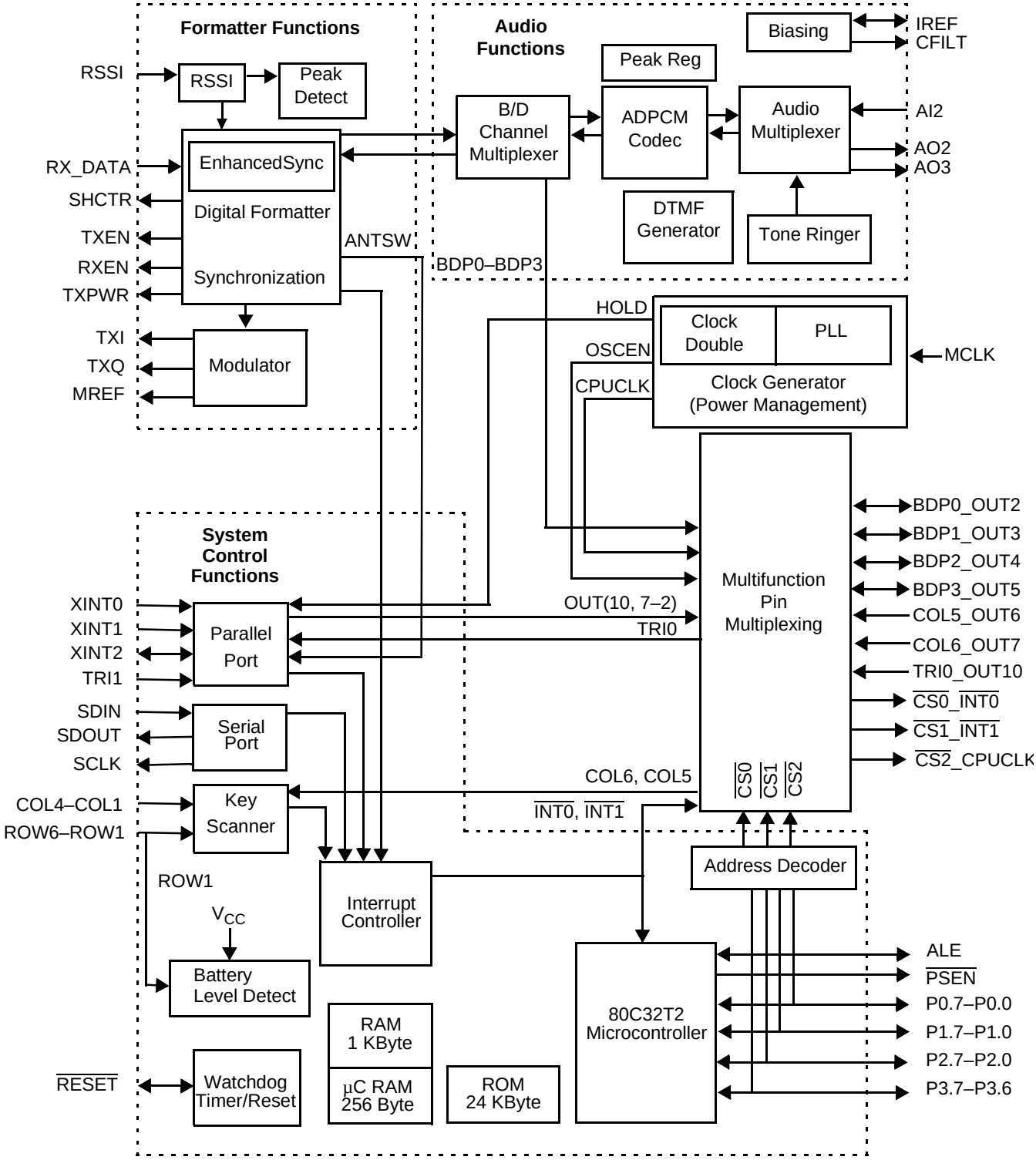
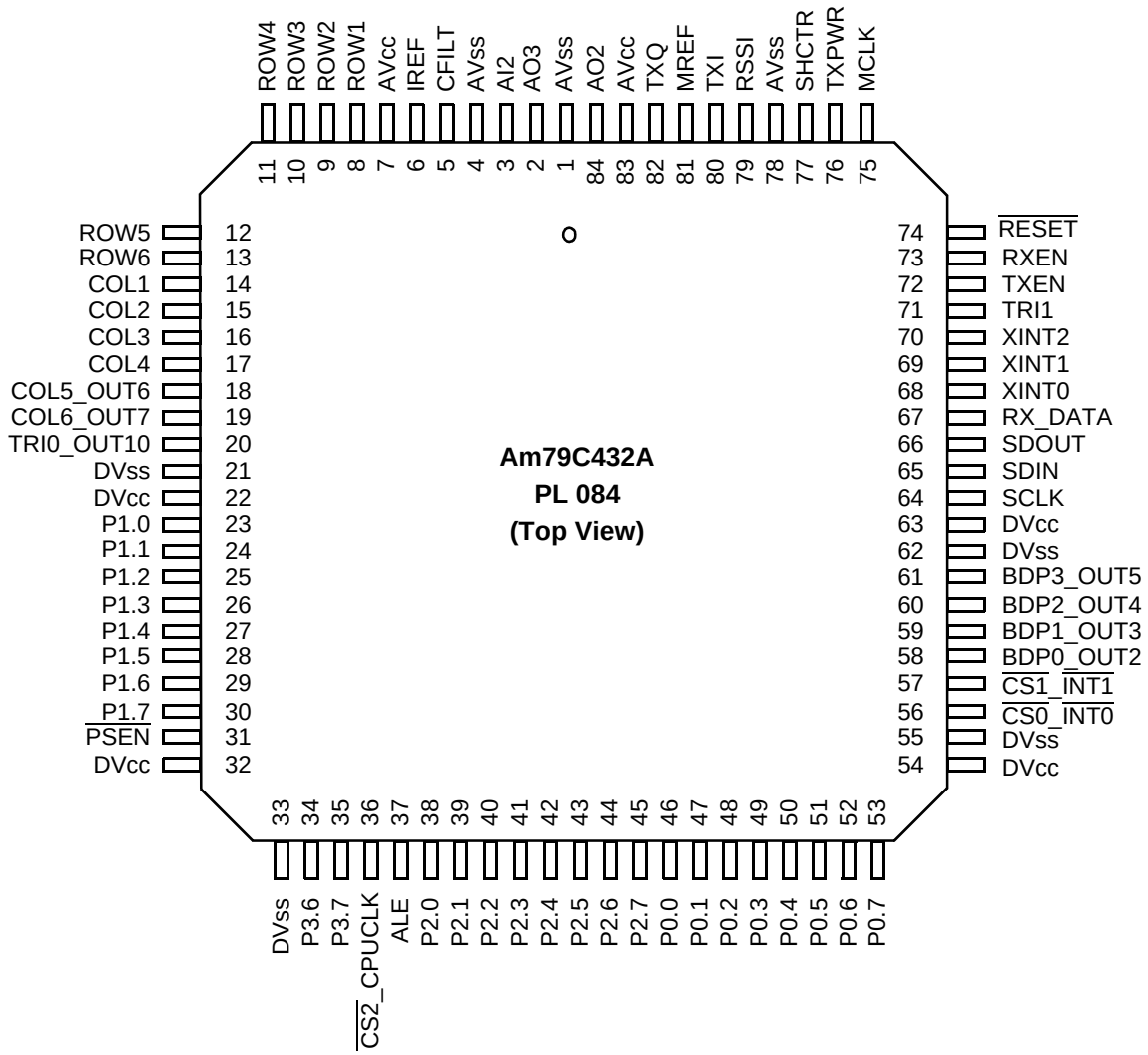


Figure 1-3 Connection Diagram



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Note:

Pin 1 marked for orientation purposes only.

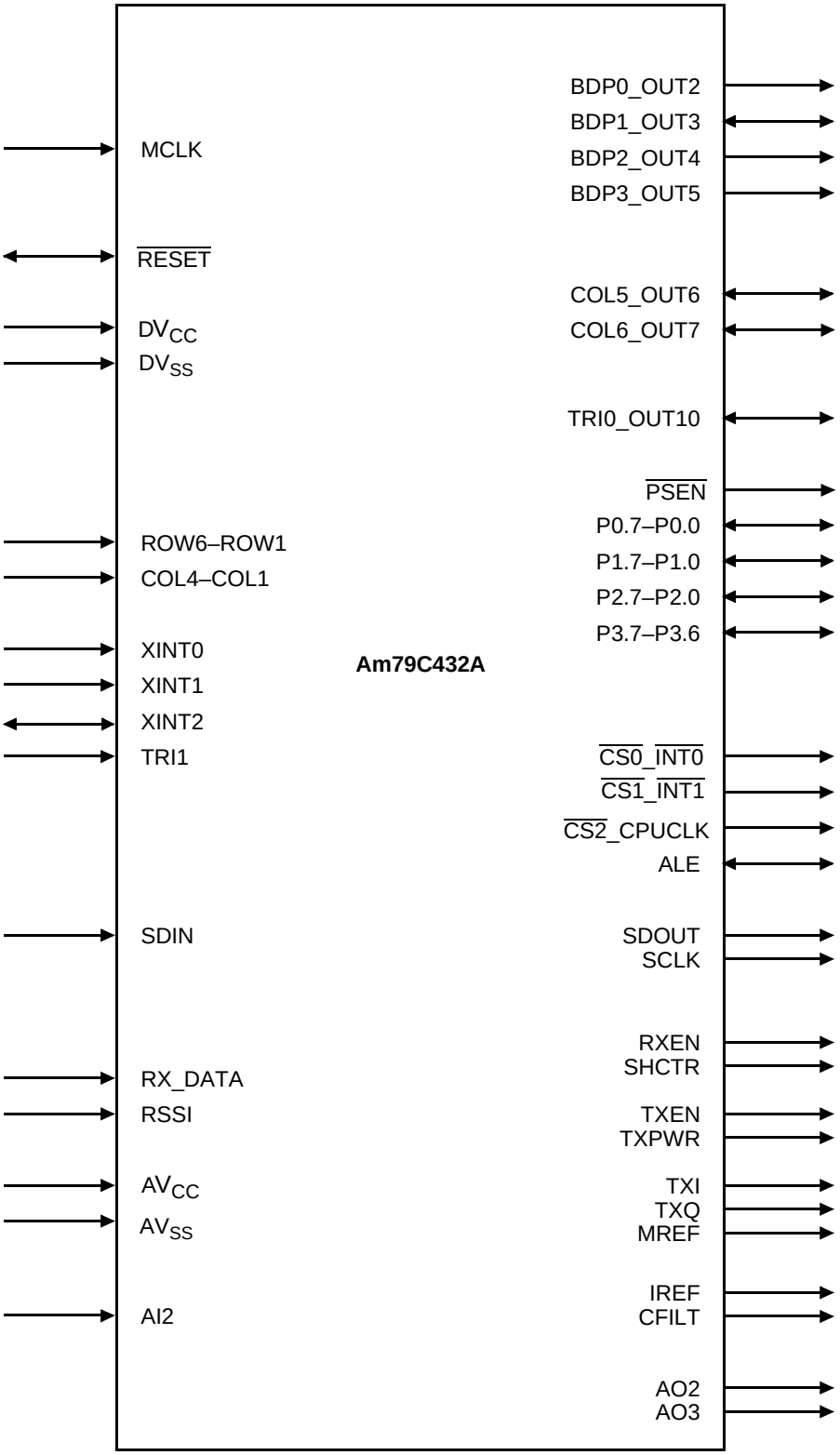
1.3 PIN LIST

Pin	Pin Name	Pad Type	Shutdown/ Idle State Conditions (Default Functions)†	Default Function or 80C32T2 Port Special Function†	Alternate Multifunction Pins†
1	AV_{SS}	ANALOG OUTPUT			
2	AO3	ANALOG OUTPUT	Z		
3	AI2	ANALOG INPUT	Z		
4	AV_{SS}	ANALOG POWER			
5	CFILT	ANALOG OUTPUT	R (reference)		
6	IREF	ANALOG OUTPUT	Z		
7	AV_{CC}	ANALOG POWER			
8	ROW1	ROWCOL	0R	ROW1	BATLEVEL (Z)
9	ROW2	ROWCOL	0R		
10	ROW3	ROWCOL	0R		
11	ROW4	ROWCOL	0R		
12	ROW5	ROWCOL	0R		
13	ROW6	ROWCOL	1R		
14	COL1	ROWCOL	1R		
15	COL2	ROWCOL	1R		
16	COL3	ROWCOL	1R		
17	COL4	ROWCOL	1R		
18	COL5_OUT6	ROWCOL	1R	COL5 (1R)	OUT6 (Q)
19	COL6_OUT7	ROWCOL	1R	COL6 (1R)	OUT7 (Q), OSCEN (Q)
20	TRI0_OUT10	TRI-INPUT	Z	TRI0 (Z)	OUT10 (Q)
21	DV_{SS}	POWER			
22	DV_{CC}	POWER			
23	P1.0	TSIO (pu)	SFR (0, 1R)		
24	P1.1	TSIO (pu)	SFR (0, 1R)		
25	P1.2	TSIO (pu)	SFR (0, 1R)		
26	P1.3	TSIO (pu)	SFR (0, 1R)		
27	P1.4	TSIO (pu)	SFR (0, 1R)		
28	P1.5	TSIO (pu)	SFR (0, 1R)		
29	P1.6	TSIO (pu)	SFR (0, 1R)		
30	P1.7	TSIO (pu)	SFR (0, 1R)		
31	$\overline{PSEN}$	TSIO (pu)	1R		
32	DV_{CC}	POWER			
33	DV_{SS}	POWER			
34	P3.6	TSIO (pu)	1R	$\overline{WR}$	
35	P3.7	TSIO (pu)	1R	$\overline{RD}$	
36	$\overline{CS2}$_CPUCLK	OUTPUT	Q	$\overline{CS2}$	CPUCLK
37	ALE	TSIO	1		
38	P2.0	TSIO (pu)	SFR (0, 1R)	A[8]	
39	P2.1	TSIO (pu)	SFR (0, 1R)	A[9]	
40	P2.2	TSIO (pu)	SFR (0, 1R)	A[10]	
41	P2.3	TSIO (pu)	SFR (0, 1R)	A[11]	
42	P2.4	TSIO (pu)	SFR (0, 1R)	A[12]	
43	P2.5	TSIO (pu)	SFR (0, 1R)	A[13]	
44	P2.6	TSIO (pu)	SFR (0, 1R)	A[14]	
45	P2.7	TSIO (pu)	SFR (0, 1R)	A[15]	

Pin	Pin Name	Pad Type	Shutdown/ Idle State Conditions (Default Functions)†	Default Function or 80C32T2 Port Special Function†	Alternate Multifunction Pins†
46	P0.0	TSIO (keeper)	QZ	A/D[0]	
47	P0.1	TSIO (keeper)	QZ	A/D[1]	
48	P0.2	TSIO (keeper)	QZ	A/D[2]	
49	P0.3	TSIO (keeper)	QZ	A/D[3]	
50	P0.4	TSIO (keeper)	QZ	A/D[4]	
51	P0.5	TSIO (keeper)	QZ	A/D[5]	
52	P0.6	TSIO (keeper)	QZ	A/D[6]	
53	P0.7	TSIO (keeper)	QZ	A/D[7]	
54	DV_{CC}	POWER			
55	DV_{SS}	POWER			
56	$\overline{CS0}$_$\overline{INT0}$	OUTPUT	Q	$\overline{CS0}$	$\overline{INT0}$
57	$\overline{CS1}$_$\overline{INT1}$	OUTPUT	Q	$\overline{CS1}$	$\overline{INT1}$
58	BDP0_OUT2	OUTPUT	Q	BCHOUT	OUT2 (Q), BDTXCLK
59	BDP1_OUT3	TSIO	Z	BCHIN	OUT3 (Q), BDTXD
60	BDP2_OUT4	OUTPUT	Q	BCLK	OUT4 (Q), BDTXEN
61	BDP3_OUT5	OUTPUT	Q	CLK8K	OUT5 (Q), CLK8K
62	DV_{SS}	POWER			
63	DV_{CC}	POWER			
64	SCLK	OUTPUT	Q	SCLK	
65	SDIN	INPUT (keeper)	QZ	SDIN	
66	SDOUT	OUTPUT	Q	SDOUT	
67	RX_DATA	INPUT	Z		
68	XINT0	INPUT	Z		
69	XINT1	INPUT	Z	XINT1	HOLD
70	XINT2	INPUT	Z	XINT2	ANTSW (Q)
71	TRI1	TRI-INPUT (pu)	1R		
72	TXEN	OUTPUT	Q		
73	RXEN	OUTPUT	Q		
74	$\overline{RESET}$	TSIO (od)	Z (ext pu)		
75	MCLK	INPUT	Z		
76	TXPWR	OUTPUT	Q		
77	SHCTR	OUTPUT	Q		
78	AV_{SS}	ANALOG POWER			
79	RSSI	ANALOG INPUT	Z		
80	TXI	ANALOG OUTPUT	Z	TXI	NRZTXD
81	MREF	ANALOG OUTPUT	Z		
82	TXQ	ANALOG OUTPUT	Z	TXQ	$\overline{NRZTXD}$
83	AV_{CC}	ANALOG POWER			
84	AO2	ANALOG OUTPUT	Z		

† *Q: Keeps previous state*
1: Output drives high
0: Output drives low
R: Resistive
Z: High impedance
SFR: Register

1.4 LOGIC SYMBOL



1.5 PIN DESCRIPTION

All signals are CMOS levels unless otherwise stated. See Section 1.6 for a summary of multifunction pins.

1.5.1 Formatter Pins

Pin	Pin Name	Type	Description
58	BDP0_OUT2	O†	Digital B or D channel or clock. In Shutdown mode, the pin retains its value.
59	BDP1_OUT3	I/O†	Digital B channel input, D channel I/O, B+D transmit data (BDTXD signal) or modulator test data input. As an output in Shutdown mode, the pin retains its value.
60	BDP2_OUT4	O†	Digital B or D channel clock output. In Shutdown mode, the pin retains its value. Also the BDTXEN pulse, which is active during transmission when properly configured.
61	BDP3_OUT5	O†	Digital B or D channel clock output. In Shutdown mode, the pin retains its value.
67	RX_DATA	I	72 kHz digital receive data with CMOS levels. Not internally Schmitt triggered.
81	MREF	O	Modulator DC reference. $0.5 \bullet V_{CC} \pm 5\%$. When disabled, the pin looks like a 25 kΩ resistance to analog ground.
79	RSSI	I	Receive signal strength indicator analog input. High impedance, DC-coupled. For noise rejection, a small filter capacitor may be tied between RSSI and analog ground.
73	RXEN	O	Active High strobe indicating the receive window for enabling receiver IF and RF circuits.
77	SHCTR	O	Sample/hold control for maintaining receiver discriminator DC level between receive windows.
72	TXEN	O	Active High strobe indicating the transmit window for enabling transmitter IF and RF circuits.
80	TXI	O	Modulator in-phase output. ±0.5 V peak, DC-coupled, internally DC-biased to MREF. Also NRZ+ output. When disabled, the pin looks like a 25 kΩ resistance to analog ground.
76	TXPWR	O	Normal power/low power transmitter mode control output.
82	TXQ	O	Modulator quadrature output. ±0.5 V peak, DC-coupled, internally DC-biased to MREF. Also NRZ+ output. When disabled, the pin looks like a 25 kΩ resistance to analog ground.
70	XINT2	I/O†	Antenna Switch RF Timing control output.

† *Indicates multifunction pins whose characteristics depend on software configuration.*

1.5.2 Audio Pins

Pin	Pin Name	Type	Description
3	AI2	I	Analog audio input. ±0.354 V_{peak}, AC-coupled, internally DC-biased to 0.5 • V_{CC}. Programmable gain applied internally. R_{IN} > 10 kΩ. Typically used for microphone input.
34	AO2	O	High current drive analog audio output. ±1.0 V_{peak}, AC-coupled, internally DC-biased to 0.5 • V_{CC}. Programmable gain applied internally. Maximum load: R_{load} ≥ 13 Ω, C_{load} ≤ 100 pF. When disabled or in Shutdown, output is high impedance. Typically used for loudspeaker driver.
2	AO3	O	Analog audio output. ±1.0 V_{peak}, AC-coupled, internally DC-biased to 0.5 • V_{CC}. Programmable gain applied internally. Maximum load: R_{load} ≥ 160 Ω, C_{load} ≤ 100 pF. When disabled or in Shutdown, output is high impedance. Typically used for earpiece driver.
58	BDP0_OUT2	O†	32 kbit/s ADPCM B channel output. In Shutdown mode, the pin retains its value.
59	BDP1_OUT3	I/O†	32 kbit/s ADPCM B channel input.
60	BDP2_OUT4	O†	Digital B channel bit clock output. In Shutdown mode, the pin retains its value.
61	BDP3_OUT5	O†	Digital B channel frame clock output. In Shutdown mode, the pin retains its value.
6	IREF	O	Current reference output, which must be tied to a temperature-stable resistor connected to analog ground and located as close as possible to the IC to minimize noise. The resistor should be 61.9 kΩ with 1% tolerance, creating a ≈20 µA reference. The pin goes to high impedance in Shutdown mode.
5	CFILT	O	0.5 • V_{CC} DC bias filter pin. Must be connected to 11 µF (10 µF low-frequency capacitor in parallel with 1 µF high-frequency capacitor) tied to ground and located close to the IC to minimize noise. The pin is not disabled by Shutdown or reset.

† *Indicates multifunction pins whose characteristics depend on software configuration.*

1.5.3 Microcontroller and Address Decoder Pins

Pin	Pin Name	Type	Description
37	ALE	I/O†	This multifunction pin is configured by software and basic mode selection to be an ALE input or an ALE output (default) The ALE signal is the 80C32T2 address latch enable for latching the lower order address on the P0 bus during external accesses. In Emulation mode, the pin is the ALE input for addressing on-chip memory and registers. During Quiet mode, the pin is disabled and only internal memory can be accessed.
56	$\overline{CS0}$_$\overline{INT0}$	O†	In normal mode $\overline{CS0}$_$\overline{INTO}$ drives the $\overline{CS0}$ output, an active Low address space decode. In Emulation mode it drives the $\overline{INT0}$ signal, which is ordinarily connected to the 8051 emulator $\overline{INT0}$ input.
57	$\overline{CS1}$_$\overline{INT1}$	O†	In normal mode $\overline{CS1}$_$\overline{INT1}$ drives the $\overline{CS1}$ output, an active Low address space decode. In Emulation mode it drives the $\overline{INT1}$ signal, which is ordinarily connected to the 8051 emulator $\overline{INT1}$ input.
36	$\overline{CS2}$_CPUCLK	O†	This multifunction pin is configured by software and Emulation mode selection to be either the $\overline{CS2}$ address space decode output or the 80C32T2 clock output.
46–53	P0.7–P0.0	I/O	Port 0 is the multiplexed data and lower order address bus for external data and program memory access, using strong internal pull-ups when driving 1s. For detailed information, see Appendix B.5, *80C32T2 Appendices, PhoX™ Controller for Digital Cordless Telephones*. P0.7–P0.0 are held weakly High during reset. In Shutdown mode, they are held strongly Low or weakly High, depending on the last operation performed on them. They are high impedance in Emulation mode. During Quiet mode, the pin is disabled and only internal memory can be accessed.
23–30	P1.7–P1.0	I/O	Port 1 is an 8 bit I/O port with internal pull-ups. Port 1 pins written to 1 s are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins externally pulled Low source current because of the pull-ups. All Port 1 pins may be programmed to generate interrupts in response to changes of state. For detailed information, see Appendix B.5, *80C32T2 Appendices, PhoX™ Controller for Digital Cordless Telephones*. P1.7–P1.0 are held weakly High during reset and retain their programmed values in Shutdown mode. They are high impedance in Emulation mode. The pullup associated with each pin can be individually disabled.
38–45	P2.7–P2.0	I/O	Port 2 is the upper order address byte during fetches from program memory and during access to external data memory that use the MOVX @DPTR instruction. In this application, it uses strong pull-ups when emitting 1s. During accesses to external data memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 special function register. P2.7–P2.0 are held weakly High during reset and in Shutdown mode and are high impedance in Emulation mode. The pullup associated with each pin can be individually disabled. During Quiet mode, the pin is disabled and only internal memory can be accessed.

Pin	Pin Name	Type	Description
34	P3.6	I/O	The P3.6 pin is the $\overline{WR}$ signal, which is the active Low external data memory write strobe. In normal mode, P3.6 is the $\overline{WR}$ output for external components. In Emulation mode, it is the $\overline{WR}$ input for writing on-chip memory and registers. During Quiet mode, the pin is disabled and only internal memory can be accessed.
35	P3.7	I/O	The P3.7 pin is the $\overline{RD}$ signal, which is the active Low external data memory read strobe. In normal mode, P3.7 is the $\overline{RD}$ output for external components. In Emulation mode, it is the $\overline{RD}$ input for reading on-chip memory and registers. During Quiet mode, the pin is disabled and only internal memory can be accessed.
31	$\overline{PSEN}$	O	$\overline{PSEN}$ is the active Low read strobe to external program memory. In Shutdown, $\overline{PSEN}$ is held weakly High. In Emulation mode, the pin is high impedance.

† *Indicates multifunction pins whose characteristics depend on software configuration.*

1.5.4 Parallel Port Pins

Pin	Pin Name	Type	Description
58 59 60 61 18 19	BDP0_OUT2 BDP1_OUT3 BDP2_OUT4 BDP3_OUT5 COL5_OUT6 COL6_OUT7	O† I/O† O† O† I/O† I/O†	General purpose outputs OUT7–OUT2 are functions that share configurable multifunction pins. When programmed for the OUT function, the pin drives the level programmed in the associated GPOCTR0 or GPOCTR1 registers and retains that value when the chip goes into Shutdown mode. Outputs default to 1 at reset.
20	TRI0_OUT10	I/O†	TRI0_OUT10 is a multifunction pin configured to provide the TRI0 input or the OUT10 output. As TRI0, it is a software readable 3-level input detecting V_{SS}, V_{CC}, and open (no connect). As OUT10, it is driven to the state programmed by software in the GPOCTR1 register.
71	TRI1	I	3-level software readable input: V_{SS}, V_{CC}, and open (no connect). During reset, the state on TRI1 determines the operating mode of the chip.
68	XINT0	I	External interrupt 0 generates an interrupt on a change of state.
69	XINT1	I†	External interrupt 1 generates an interrupt on a change of state.
70	XINT2	I†	External interrupt 2 generates an interrupt on a change of state.

† *Indicates multifunction pins whose characteristics depend on software configuration.*

1.5.5 Key Scanner and Serial Port Pins

Pin	Pin Name	Type	Description
14–17	COL1–COL4	I	Key scanner matrix column inputs. Each input has an internal weak pullup. Small capacitors (≈0.1 µF) between the pins and DV_{SS} may be applied to improve noise immunity.
18 19	COL5_OUT6 COL6_OUT7	I/O† I/O†	Key scan COL5 and COL6 inputs with weak internal pull-ups. Small capacitors (≈ 0.1 µF) between the pins and DV_{SS} may be applied to improve noise immunity.
8 9–13	ROW1 ROW2–ROW6	I† I	Key scanner matrix row inputs. Each input has an internal weak pull-down. Small capacitors (≈0.1 µF) between the pins and DV_{SS} may be applied to improve noise immunity. ROW1 may also serve as a battery level input for the battery level detector.
64	SCLK	O†	Serial port clock output function. It is pulled Low when the serial port is disabled or when the chip is in Shutdown.
65	SDIN	I†	Serial port data input function.
66	SDOUT	O†	Serial port data output function. The pin is pulled Low when the serial port is disabled or when the chip is in Shutdown.

† *Indicates multifunction pins whose characteristics depend on software configuration.*

1.5.6 Clock, Reset, and Power Supply Pins

Pin	Pin Name	Type	Description
83, 7	AV_{CC}	I	Analog power supply, which must be connected to the digital power supply. It is important to provide decoupling capacitors of ≈1 µF across the following pin combinations: Decouple pin 83 to ground pin 78 (modulator and RSSI supply), decouple pin 83 to ground pin 1 (analog audio outputs supply), decouple pin 7 to ground pin 4 (analog inputs, audio mux, A/D, D/A, and battery detector supply)
78, 1, 4	AV_{SS}	O	Analog ground. Analog and digital grounds must be connected. Pin 78 is the reference for the modulator and RSSI functions. Pin 1 is the ground reference for audio outputs AO2 and AO3. Pin 4 is the reference for analog input AI2.
19	COL6_OUT7	I/O†	Oscillator Enable (OSCEN) output.
22, 32, 54, 63	DV_{CC}	I	Digital power supply. Digital and analog supplies must be tied together. It is important to provide decoupling capacitors of ≈ 0.1 µF across the following pin combinations: Decouple pin 22 to ground pin 21, decouple pin 32 to ground pin 33, decouple pin 54 to ground pin 55, decouple pin 63 to pin 62.
21, 33, 55, 62	DV_{SS}	O	Digital ground. Digital and analog grounds must be connected.
75	MCLK	I	12.8 MHz 50% duty cycle CMOS-level master clock input, timing source for the entire chip.
74	$\overline{\text{RESET}}$	I/O	Active Low, open-drain reset input returns chip to default state. The pin must be externally pulled up. Watchdog timer function drives the pin Low when timer expires. In Emulation mode, the pin is an input only.
69	XINT1	I†	Shutdown HOLD control input.

† *Indicates multifunction pins whose characteristics depend on software configuration.*

1.6 AM79C432A PIN MULTIPLEXING

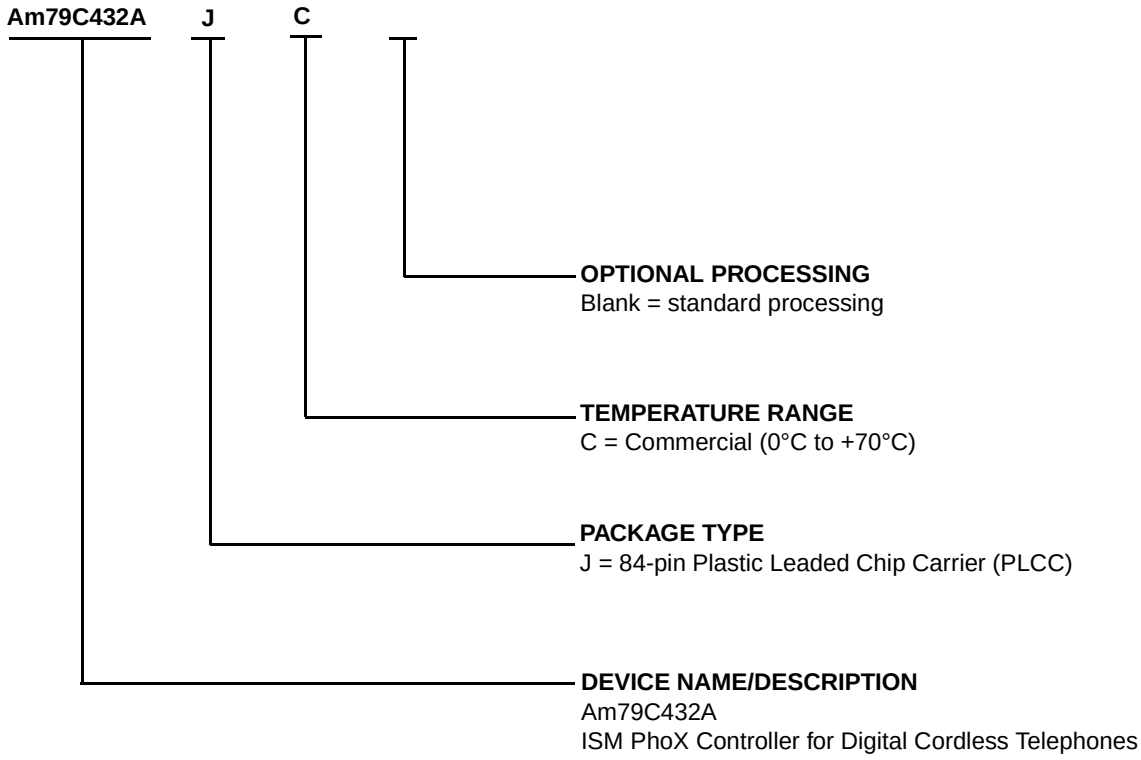
The following table lists multifunction pins and their function selection controls.

Pin Name	Pin	Multiplexed Functions	Function Selection	Page
ALE	37	• 80C32T2 ALE output • 80C32T2 ALE input	Normal mode Emulation mode	— 2-42
BDP0_OUT2	58	• 32 kbit/s B channel output • General-purpose output port 2 • Receive D channel monitor data • 72 kHz clock output	BDMUX[6:5]	2-43
BDP1_OUT3	59	• 32 kbit/s B channel input • General-purpose output port 3 • Transmit D channel data I/O • 72 kHz digital data output • Modulator test data input	BDMUX[6:5], MODTST	2-44
BDP2_OUT4	60	• 32 kHz B channel clock out • General-purpose output port 4 • Receive D channel monitor clock • 500 Hz transmit window	BDMUX[6:5]	2-44
BDP3_OUT5	61	• 8 kHz B channel output • General-purpose output port 5 • Transmit D channel I/O clock	BDMUX[6:5]	2-44
COL5_OUT6	18	• Key scanner column 5 input • General-purpose output 6	GPOCTR1[5]	2-8, 2-21
COL6_OUT7	19	• Key scanner COLUMN input • General-purpose output OUT7 • Oscillator enable OSCEN output	GPOCTR1[6,4]	2-8, 2-21
$\overline{CS0}$_$\overline{INT0}$	55	• Chip select output 0 • INT0 interrupt output	Emulation mode	2-42
$\overline{CS1}$_$\overline{INT1}$	56	• Chip select output 1 • INT1 interrupt output	Emulation mode	2-42
$\overline{CS2}$_CPUCLK	30	• Chip select output 2 • 80C32T2 clock output	Emulation mode ADRDEC[1]	2-8, 2-42
ROW1	8	• Key scanner ROW input • Battery Level input	BATLEV[6]	2-8
TRI0_OUT10	20	• 3-level input 0 • General-purpose output 10	GPOCTR1[7]	2-12
TXI	80	• In-phase modulator output • NRZ+ output	MODTST[4]	2-22, 2-27
TXQ	82	• Quadrature modulator output • NRZ– output	MODTST[4]	2-27, 2-28
XINT1	69	• External interrupt input • HOLD input for low battery	UCCCTR[5]	2-1, 2-12
XINT2	70	• External interrupt input • ANTSW antenna switch output	RDELAY[5]	2-12, 2-28

1.7 ORDERING INFORMATION

1.7.1 Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (valid combination) is formed by a combination of the elements below:



Valid Combinations	
Am79C432A	JC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

1.8 GLOSSARY OF TERMS

The following terms are used frequently throughout the text:

ADPCM	Adaptive Differential Pulse Code Modulation, a voice compression and encoding technique
B Channel	Voice Channel, 32 kbit/s
CCITT	International Telegraph and Telephone Consultative Committee
CFP	Cordless Fixed Part (base station)
CHM (CHMF, CHMP)	Channel Marker. Suffixes F and P refer to Fixed parts and Portable parts (CFP and CPP)
CPP	Cordless Portable Part (handset)
CRC	Cyclic Redundancy Check
D Channel	Control Channel
DTMF	Dual-Tone Multifrequency
GMSK	Gaussian minimum-shift key
IDLE_D	D Channel Idle fill pattern
MUX	Multiplex, a time-division duplex structure
NRZ	Non-Return-to-Zero
PCM	Pulse Code Modulation, a logarithmic encoding technique
PLL	Phase-locked loop
POTS	Plain Old Telephone Service (i.e., standard analog line service)
PSTN	Public Switched Telephone Network
RSSI	Receive Signal Strength Indicator
SFR	8032 Microcontroller Special Function Register
SYN Channel	Synchronization Channel
SYNC (SYNCF, SYNCP)	Synchronization Pattern. Suffixes F and P refer to Fixed and Portable parts (CFP and CPP)
SYNCD	D Channel Synchronization pattern

CHAPTER

2 FUNCTIONAL DESCRIPTION

2.1 GLOBAL FUNCTIONS

2.1.1 Reset and Basic Mode Establishment

The reset pin is an active Low I/O that resets the chip to its default state when driven Low. The chip drives reset Low due to watchdog timer expiration or software reset. A software reset may be induced by writing 00 hex to the WDTKEY register.

The basic operating mode is defined by the level of the TRI1 pin at reset, according to Table 2-1. This pin must remain in its reset configuration for proper functioning.

Table 2-1 Establishing the Basic Operating Mode

Basic Operating Mode	Processor	ROM Configuration	TRI1 Pin During Reset
Normal Mode	Internal	Internal (External Optional)	V_{CC}
External Mode	Internal	External	Unconnected
Emulation Mode	External	External	V_{SS}

Normal mode is for typical chip applications. This mode uses the embedded 80C32T2 processor and ROM (code user-supplied) as well as additional external ROM, if required. External mode bypasses the internal ROM, mapping that space to external ROM. Emulation mode is for code development with an 8051 in-circuit emulator.

2.1.2 Power Management and Shutdown Mode

The power management features of the PhoX chip are centralized in a block called the clock generator. Each functional block in the chip is individually enabled or disabled by programming the appropriate bit in the MECTR0 or MECTR1 register.

The shutdown state disables all synchronous and analog circuits, minimizing power consumption. Programming UCCCTR[7] initiates the shutdown sequence, which brings the PhoX chip cleanly to a static state. The shutdown sequence takes 3.56 ms to 7.2 ms to complete, depending on the initial conditions, so software has 3.56 ms to perform housekeeping tasks necessary before all clocks on the chip stop and analog circuits power down. These tasks should include disabling the codec and analog interfaces and programming the 80C32T2 for Idle mode. Any enabled interrupt occurring during the sequence will cause it to abort.

Any enabled interrupt awakens the chip from shutdown. The wake-up sequence takes 3.56 ms, as determined by counting PLL clock periods, and returns the chip to its condition before shutdown. Analog circuits take approximately 300 µs to reactivate and stabilize.

The OSCEN (oscillator enable, active high) output brings the internal shutdown status out to the COL6_OUT7 pin so that it may be used to enable an external 12.8 MHz clock source.

The control is located in the GP0CTR1 register. COL6_OUT7 resets to a pulled-High (active) state.

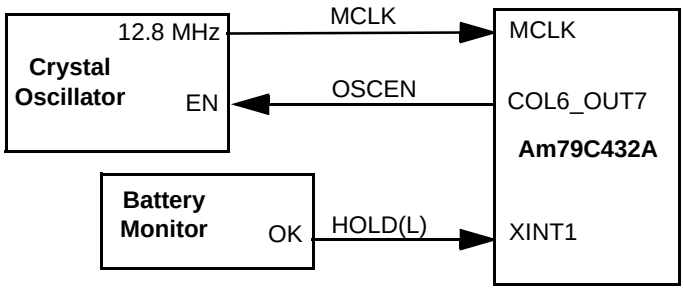
Note: *The PLL starts running as soon as OSCEN goes active.*

The hold function masks all interrupts such that they do not cause the device to exit shutdown when battery levels are marginal, as doing so might cause erroneous operation and violation of spurious emissions specifications. The HOLD input appears on the XINT1 input pin and is intended to be driven by an external battery monitor device, which drives the pin Low when the battery level is too low (< 2.7 V). Figure 2-1 shows an application using the OSCEN and HOLD features. Software is expected to respond to the interrupt on XINT1 caused by the level transition of the HOLD signal by programming the UCCCTR register to place the PhoX chip in Shutdown mode. Once in Shutdown mode, the chip will not wake up as long as HOLD is Low. The Hold mode, therefore, keeps the PhoX device from generating spurious transmissions when battery levels are marginal. After HOLD returns High (e.g., the user recharges or replaces the battery), any ordinary wake-up stimulus, including the XINT1 interrupt driven by the HOLD signal, will awaken the PhoX device from shutdown.

To use the hold function, UCCCTR[5] must be programmed High. Otherwise, the hold function is deactivated and the XINT1 pin acts only as an interrupt input.

The 80C32T2 clock rate is programmable in the UCCCTR register for reduced power consumption. The clock rate control mechanism includes an automatic speedup feature, which allows any interrupt to increase the clock rate immediately to maximum speed for fast interrupt service. When enabled, auto speedup responds to interrupts on the 8032 $\overline{INT0}$ or $\overline{INT1}$ interrupts. These interrupts are internal to the chip and are driven by the interrupt controller.

Figure 2-1 OSCEN and HOLD Application



2.2 SYSTEM CONTROL BLOCK FUNCTIONS

2.2.1 80C32T2 Microcontroller

The microcontroller in the PhoX chip is a member of the 8051 family of microcontrollers, with the standard 8051-family architecture and instruction set. The microcontroller is referred to throughout this manual as an 80C32T2 (or simply 8032). A key feature of the 80C32T2 is its dual data pointer. Appendices B, C, and D in the *80C32T2 Appendices, PhoX™ Controller for Digital Cordless Telephones* define the architecture, programming requirements, and instruction set for the 8032.

2.2.1.1 Memory

Tables 2-2 and 2-3 identify the separate program and data spaces of the 8032. Data space is further divided into internal and external spaces, which are accessed by different means.

Table 2-2 Program Memory Map

Program Space	Address Range	Size
Normal Mode TRI1 = V_{CC} Internal ROM Reserved Expansion ROM	 0000–5FFE 5FFF 6000–FFFF	 24 Kbyte 1 byte 40 Kbyte
External or Emulation Mode TRI1 ≠ V_{CC} External ROM	0000–FFFF	64 Kbyte

Table 2-3 Data Memory Map

8032 Internal Data Space	Address Range	Size
Internal RAM, direct/indirect access	00–7F	128 byte
Internal RAM, indirect access only	80–FF	128 byte
Special Function Registers (SFRs), direct access only	80–FF	27 byte

8032 External Data Space (Access by Movx)	Address Range	Size
Internal RAM (if not ADRDEC[7])	0000–03FF	1 Kbyte
$\overline{CS1}$ (if ADRDEC[7]) $\overline{CS1}$ (if not ADRDEC[7])	0000–EFFF 0400–EFFF	60 Kbyte 59 Kbyte
$\overline{CS0}$	F000–F3FF	1 Kbyte
$\overline{CS2}$	F400–F7FF	1 Kbyte
(Unmapped)	F800–FEFF	2 Kbyte
PhoX Chip Memory Mapped Registers	FF00–FFFF	256 byte

2.2.1.2 Clock Input

The microcontroller clock is supplied by an internal signal called CPUCLK, which is derived from the MCLK pin. The frequency of CPUCLK is programmable from 72 kHz to 9.216 MHz in the UCCCTR register. By programming UCCCTR for Shutdown mode, CPUCLK stops entirely. The Automatic Speedup mode enables hardware to immediately increase the CPUCLK speed to its maximum when triggered by an interrupt at either of the 8032 external interrupts, $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$. The auto speedup feature does not respond to the 8032 timer/counter or serial port interrupts.

2.2.1.3 Reset

The reset input is active Low, different than standard 8051-family microcontroller reset inputs.

2.2.1.4 $\overline{\text{EA}}$

The PhoX chip has no external address select ($\overline{\text{EA}}$) pin, present in standard 8051-family microcontrollers. This function is controlled instead by the three-level pin TRI1 (see Section 2.1, Global Functions).

2.2.1.5 Microcontroller Port Modifications

The microcontroller ports support CMOS levels. When the device is in Emulation mode, ports assume a high impedance state.

In order to eliminate spurious glitches during reset, all ports are driven to the “float high” condition during reset.

To minimize power consumption, the Port 1, 2, and 3 buffers are capable of disabling the weak pull-ups by software control of the Port Control Register Bit special function registers.

2.2.1.6 SFR Map Additions

The special function registers listed in Table 2-4 are added to the standard 8032 SFR map to disable microcontroller port pin weak pull-ups. SFRs marked with an asterisk can be accessed only when PCFIG[0] has been set High.

Table 2-4 SFR Additions

SFR Name	SFR Address	SFR Default After Reset
PCFIG	A1H	00H
P1PCRB	90H*	00H
P2PCRB	A0H*	00H
P3PCRB	B0H*	00H

These SFRs can be accessed only when PCFIG[0] has been set High.

Each P*x*PCRB (Port [1,2,3] Port Control Register Bit) SFR contains 8 bits corresponding to the 8 bits in each of the P1, P2, and P3 ports. When a P*x*PCRB bit is cleared, the associated port behaves as a standard 8032 port, where an internal weak pull-up is applied to a port driving a 1. Setting a P*x*PCRB bit disables the weak pull-up in the respective port bit, making it a high impedance input port when the port SFR is programmed to 1.

Notice that the P*x*PCRB SFRs share the same address as the port SFRs. PCFIG is a 1-bit register and bit PCFIG[0] selects access to either the port SFR or the P*x*PCRB SFR. PCFIG[0] must be set to access the P*x*PCRB registers and must be cleared to access the port SFRs.

2.2.1.7 $\overline{\text{PSEN}}$ Modifications

To reduce power consumption during instruction fetches from external program ROM, the $\overline{\text{PSEN}}$ pulse width is reduced when the CPUCLK clock signal is programmed below 9.216 MHz.

2.2.1.8 Interrupt Modifications

The $\overline{\text{INT0}}$ (P3.2) and $\overline{\text{INT1}}$ (P3.3) interrupt inputs are driven internally. The interrupt sources on the PhoX chip, reported in the MISRC0 and MISRC1 registers, are fundamentally level-sensitive in nature. Therefore, TCON[2,0] should be programmed Low for proper interrupt response.

The 8032 Idle mode bit (PCON[0]) supports the low-power Shutdown mode such that the controller clock can be stopped indefinitely. To avoid the possibility of entering the Idle mode with all interrupts disabled and therefore being incapable of awakening without a full reset, the 8032 ignores the interrupt mask bits IE[7,2,0] when in Idle mode. Both external interrupts are enabled but the IE bits themselves are unchanged.

For software development purposes in the in-circuit emulator environment, software should always enable interrupts in IE before programming the Idle mode bit, since the wakeup safeguard is not present in standard 8051-family emulators.

2.2.1.9 T0 and T1

The T0 (P3.4) and T1 (P3.5) signals do not appear as pins on the PhoX chip. They are internally tied to a 18 kHz clock source enabled in the MECTR0 register, located in external data space.

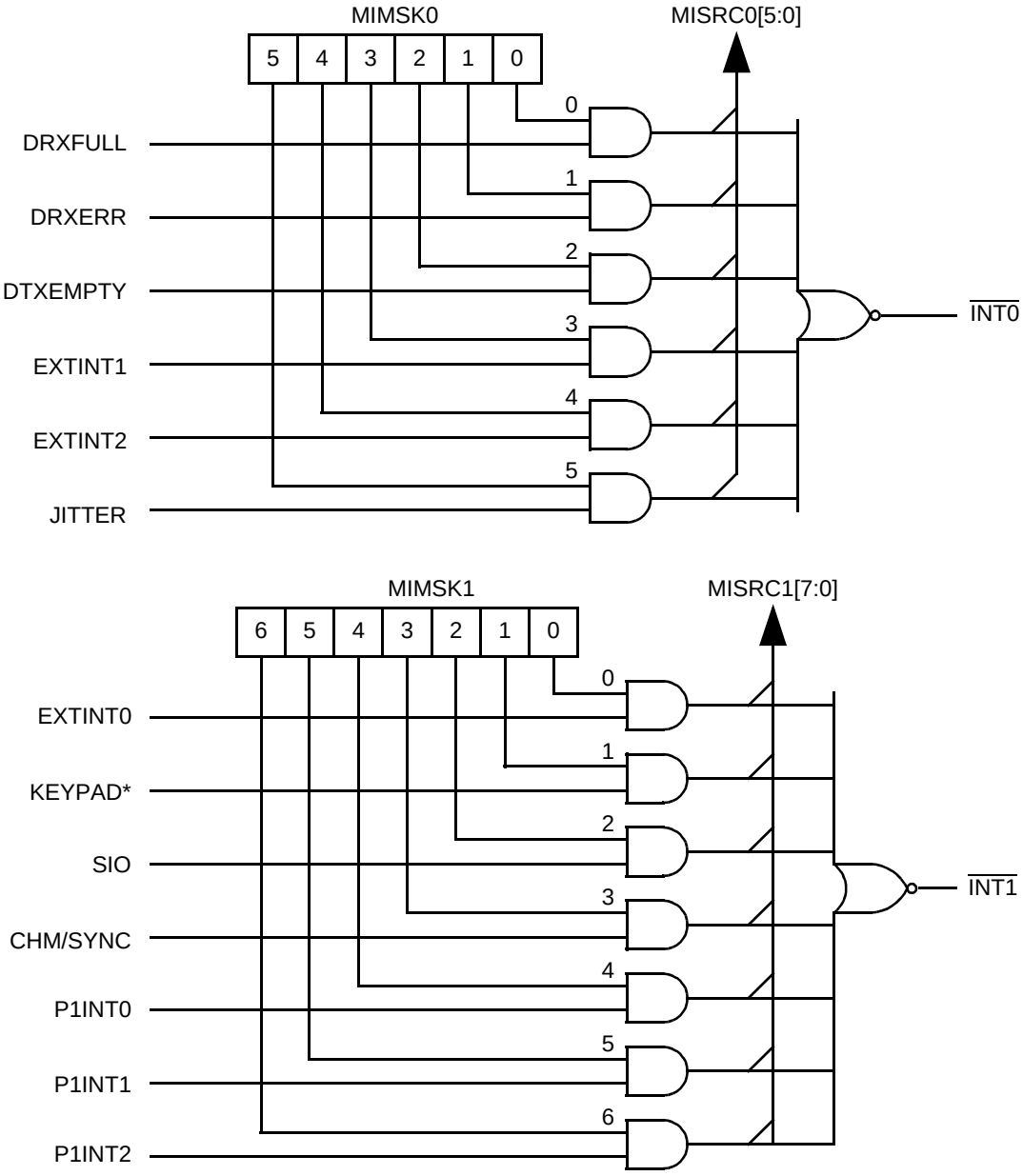
When using the counter functions, care must be taken with regard to the T0 and T1 clock input and the CPUCLK rate. In Counter mode, the 8032 samples the T0 and T1 inputs once per machine cycle and increments the counter only on negative transitions of the sampled counter input; therefore, the counter function works normally only for CPUCLK rates greater than 24 • 18 kHz (i.e., 576 kHz to 9.216 MHz).

2.2.2 Interrupt Controller

The centralized interrupt controller incorporates all interrupts generated by the various on-chip functions into the $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ interrupts recognized by the 8032 microcontroller. Software controls masking in the MIMSK0 and MIMSK1 registers and determines interrupt sources by reading status registers MISRC0 and MISRC1. Figure 2-2 shows the interrupt tree. For proper response to all interrupts, the 8032 should be programmed for level-sensitive interrupts. Tables 2-5 and 2-6 list all interrupt sources and service requirements.

Any unmasked interrupt causes a PhoX device in shutdown to awaken. The key scan interrupts are automatically enabled during shutdown for system viability and their masks are automatically returned to their previous condition after the system awakens and recognizes the interrupt source. The HOLD feature (Section 2.1.2) blocks all interrupts while the device is in Shutdown mode.

Figure 2-2 Interrupt Tree



**KEYPAD is automatically enabled during Shutdown mode.*

Table 2-5 8032 $\overline{\text{INT0}}$ Interrupt Sources

MISRC0 Bit	Interrupt Mnemonic	Source	Description
0	DRXFULL	Digital Formatter	D channel receive buffer full or half-full. Cleared by reading RXBUF5.
1	DRXERR	Digital Formatter	CRC, parity, or overflow error detected in received D channel. Cleared by reading DCHSTAT.
2	DTXEMPTY	Digital Formatter	D channel transmit buffer empty or half empty. Cleared by writing TXBUF5.
3	EXTINT1	Parallel Port	A transition on the XINT1 pin has occurred. Cleared by reading XISTAT1.
4	EXTINT2	Parallel Port	A transition on the XINT2 pin has occurred. Cleared by reading XISTAT2.
5	JITTER	Noise Suppression	Jitter or B channel noise on receive data exceeds programmed threshold or detection of ADPCM = 0. Cleared by reading NSCTR.

Table 2-6 8032 $\overline{\text{INT1}}$ Interrupt Sources

MISRC0 Bit	Interrupt Mnemonic	Source	Description
0	EXTINT0	Parallel Port	A transition on the XINT0 pin has occurred. Cleared by reading XISTAT0.
1	KEYPAD*	Key Scanner*	Activity at the keypad. Cleared by reading KPSTAT. Nonmaskable in Shutdown mode.
2	SIO	Serial Port	Transmit buffer empty or receive data available. Cleared by writing to the transmit buffer or reading from the receive buffer, respectively.
3	CHM/SYNC	Digital Formatter	A CHM/SYNC interrupt has occurred, as reflected in the CMSSRC register. Cleared by reading CMSSRC.
4	P1INT0	Parallel Port	An unmasked event has occurred on P1.1–P1.0. Cleared by reading P1SRC0.
5	P1INT1	Parallel Port	An unmasked event has occurred on P1.3–P1.2. Cleared by reading P1SRC1.
6	P1INT2	Parallel Port	An unmasked event has occurred on P1.7–P1.4. Cleared by reading P1SRC2.

**KEYPAD is automatically enabled during Shutdown mode.*

2.2.3 Address Decoder and Latch

The address decoder decodes the 8032 external data spaces listed as $\overline{CS0}$ (Chip Select 0), $\overline{CS1}$, and $\overline{CS2}$ in Table 3-1. The active Low signals are present on multifunction pins $\overline{CS0}$_$\overline{INT0}$, $\overline{CS1}$_$\overline{INT1}$, and $\overline{CS2}$_CPUCLK respectively when enabled in the ADRDEC register. The pins are automatically reconfigured in Emulation mode to provide the alternate functions $\overline{INT0}$, $\overline{INT1}$, and CPUCLK, so the chip selects are not available. They can be easily regenerated externally using standard decode logic.

2.2.4 1 Kbyte On-Chip RAM (Data RAM)

The on-chip, 1 Kbyte static RAM (data RAM) is available only when enabled in the ADRDEC register and maps into the lowest 1 Kbyte of 8032 external data space (0000-03FF).

2.2.5 Battery-Level Detection

The main battery level at V_{CC} is reflected in the BATLEV register. Software writes a value to BATLEV[3:0] and the level detector indicates whether the battery level exceeds the programmed value in BATLEV[7].

For voltage-regulated systems where V_{CC} does not represent the actual battery voltage, the ROW1 pin can be configured as a scaled input of the actual main battery level. In order to properly configure the ROW1 pin for battery input, software must set BATLEV[6]. The main battery level, as determined by the level at the ROW1 pin, is reflected in the BATLEV register. The voltage at ROW1 should be scaled to match the 0.645 to 1.25 V input range and must be kept below the actual chip V_{CC} in order to avoid device damage, so a voltage dividing resistor network with a protection diode is recommended. To request a conversion, software writes a value to BATLEV[6,3:0] and the level detector indicates whether the battery level exceeds the programmed value in BATLEV[7].

2.2.6 Watchdog Timer (WDT) and Software Reset

Software must perform the watchdog timer (WDT) key sequence *uninterrupted* at least once every 1.82 s. Failure to correctly perform the key sequence results in a 1.78 ms output pulse on the reset pin and returns the chip to its default condition. The key sequence is:

write WDTKEY = A5 hex
write WDTKEY = 5A hex

It is recommended that interrupts be disabled while performing the watchdog timer sequence or that the timer be serviced in a high priority interrupt routine that cannot be interrupted by another interrupt source.

Software may induce a software reset by writing WDTKEY=00. In fact, if any value is written to WDTKEY other than those listed in the key sequence, a reset results. Reset also occurs if the key sequence is incorrectly performed.

2.2.7 Key Scanner

The key scanner is an interrupt-driven, asynchronous keypad detection mechanism requiring software debouncing. It operates in Enabled and Disabled modes, under control of MECTR0[7] and supports a 6×6 keypad configuration. Special functions include multiple-key detection and nonmaskable any-key detection for system wakeup.

When the scanner is enabled, it generates a key scan interrupt in response to a change in keypad status (e.g., a key is pressed or released). If the scanner reports multiple keys down and another key is depressed, a second interrupt will not be generated since the keypad status is still “multiple keys down.” The interrupt appears in MISRC1[1] and may be masked in MIMSK1[1]. The KPSTAT register reports the keypad status. When the scanner is disabled, it still generates an interrupt but KPSTAT returns a fixed code, 7E hex. When the

PhoX chip enters Shutdown mode, the interrupt mask bit is temporarily bypassed so that key activity always generates an interrupt that awakens the chip. The mask bit remains bypassed until software recognizes the source of the interrupt by reading MISRC1.

The scanner input thresholds recognize a key depression as a switch closure between a row and a column pin. Row pins have weak pull-downs and column pins have weak pull-ups. When the switch closes, the level at the pins approaches mid-supply and is recognized as active at both the row and column inputs. Switch characteristics are limited by:

1. Open circuit resistance ≥ 150 kΩ between a row and a column
2. Closed circuit resistance ≤ 2 kΩ between a row and a column

If several keys in a single row or in a single column are simultaneously depressed, the level presented at the pins will not be mid-supply and may actually be close to one of the input thresholds. Noise added to inputs near the threshold levels may cause multiple occurrences of the key scanner interrupt. Capacitive coupling to ground (DV_{SS}) may help reduce noise. Current-limiting, 510 Ω resistors can be added to each row and column pin for protection against static discharge.

The inputs for columns 5 and 6 are on the multifunction pins COL5_OUT6 and COL6_OUT7 and are available only when selected in GPOCTR1[6:5]. When they are not selected, columns 5 and 6 are not recognized.

The ROW1 input is also on a multifunction pin and must be configured in BATLEV[6].

2.2.8 Serial Port

The serial port is a synchronous peripheral residing in 8032 external data space and is not the same as the 8032 serial interface. It provides a clean interface to popular serial EEPROMs and synthesizers, and performs two functions:

1. Serial output only
2. Serial output followed by input

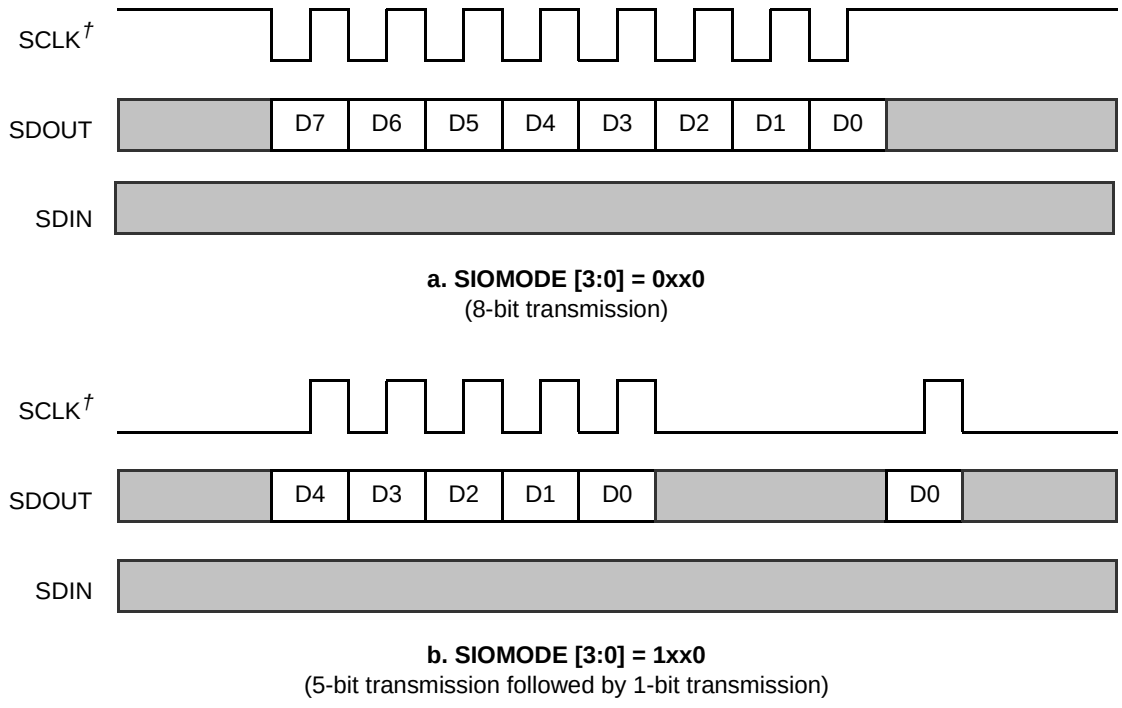
Programmable features include transmit and receive buffer lengths, clock rate, and clock polarity and are under the control of the SIOTLB, SIOTMG, and SIOMODE registers. Interrupts are enabled in the SIOMASK register and are reported in the SIOSTAT and SIOSRC registers. Figure 2-3 through Figure 2-7 demonstrate the various clock and data relationships programmable in the SIOMODE register. Note that the clock (SCLK) can be inverted by programming SIOMODE[4] = 1.

Some serial devices require one additional bit of delay between transmit and receive data bits, which can be accommodated by programming the serial port to transmit one extra bit after the normal address field has been transmitted.

In order to service several serial devices, drive the serial device chip select controls with any of the software-controlled PhoX chip ports to avoid contention.

For power management, the serial port operates in Enabled and Disabled modes, according to MECTR0[4]. When disabled, the SCLK and SDOUT pins are pulled Low. The serial port interrupt is disabled by programming MIMSK1[2] = 1.

Figure 2-3 Serial Port Write-Only Timing Example

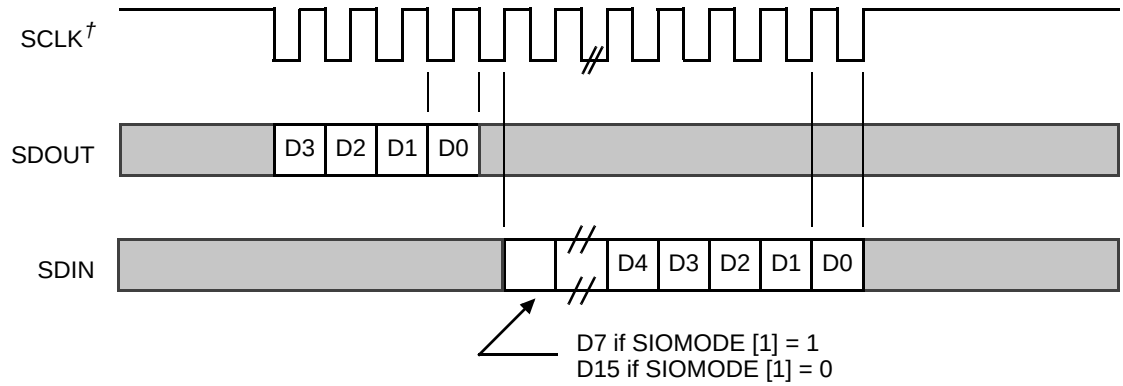


a. SIOMODE [3:0] = 0xx0
(8-bit transmission)

b. SIOMODE [3:0] = 1xx0
(5-bit transmission followed by 1-bit transmission)

† *SCLK is inverted when SIOMODE[4] = 1.*

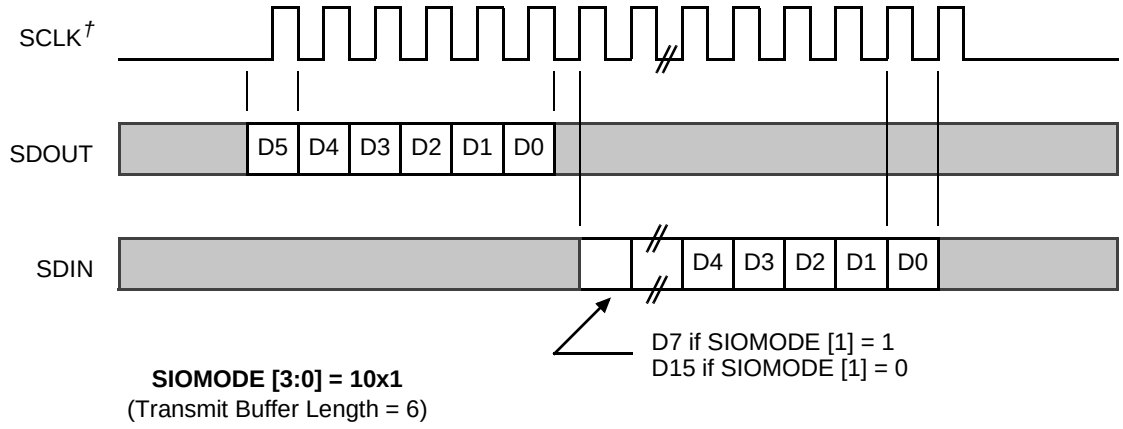
Figure 2-4 Serial Port Write/Read Timing Example 1



SIOMODE [3:0] = 00x1
(Transmit Buffer Length = 4)

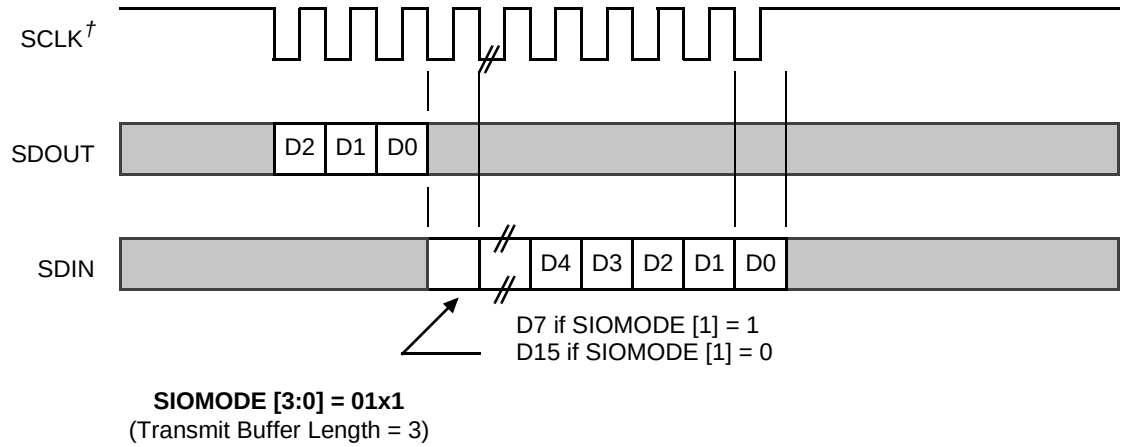
† *SCLK is inverted when SIOMODE[4] = 1.*

Figure 2-5 Serial Port Write/Read Timing Example 2



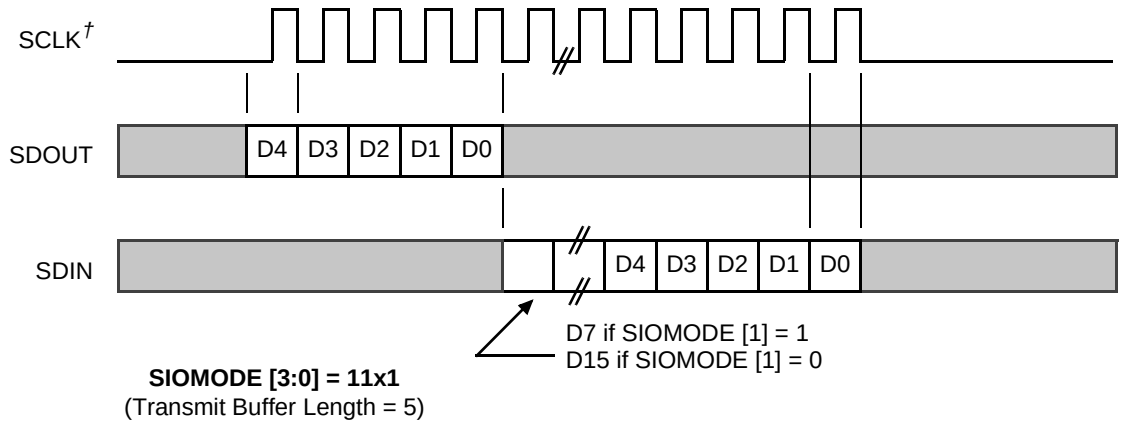
† *SCLK is inverted when SIOMODE[4] = 1.*

Figure 2-6 Serial Port Write/Read Timing Example 3



† *SCLK is inverted when SIOMODE[4] = 1.*

Figure 2-7 Serial Port Write/Read Timing Example 4



† *SCLK is inverted when SIOMODE[4] = 1.*

2.2.9 Parallel Port

The parallel port is a grouping of four independent functions:

- P1 interrupts
- External interrupts
- General-purpose output latches
- Tri-level inputs

The P1 interrupt function recognizes events at the eight 8032 P1 port pins and generates maskable interrupts in response. An event may be either a positive or negative transition of a pin, as programmed in the P1TRIG register. Bits are individually masked in the P1MASK register. Events are reported in the P1SRC0, P1SRC1, and P1SRC2 registers.

Three external interrupt inputs are provided on the XINT0, XINT1, and XINT2 pins. Any change of state on an XINT pin sets a latch causing an interrupt to appear in the interrupt controller MISRC0 or MISRC1 register. The interrupts are enabled in the MIMSK0 and MIMSK1 registers. Reading XISTAT0, XISTAT1, or XISTAT2, which report the current level of the pins, clears the respective interrupt. The XINT1 has alternate uses as system hold control, described in Section 2.1.2. The XINT2 pin has an alternate use as an RF antenna switch control, described in Section 2.3.1.10, and can therefore provide interrupts timed to the Digital Formatter frame timing.

The seven general-purpose outputs (OUT7–OUT2, OUT10) drive their respective pins to values programmed in the GPOCTR0 and GPOCTR1 registers. Each output uses a multifunction pin and is available only when that pin is programmed for the general-purpose output function in the BDMUX or GPOCTR1 registers. Outputs are designed for high current drive. For noise immunity under heavy load conditions, no more than four output levels should be changed at one time.

The two tri-level inputs are the TRI1 and TRI0_OUT10 pins. TRI0_OUT10 is a multifunction pin and the TRI0 function is available only if GPOCTR1[7] is programmed to 0. Each input converts a three-level input (low, high, and mid-supply) to a 2-bit value in the XISTAT0 register. The pins are weakly driven to $V_{CC}/2$ during reads so that the mid-supply level results if the pin is not connected. The TRI1 pin determines the basic operating mode of the PhoX chip at reset, according to Table 2-1. This pin must remain in its reset configuration for proper functioning.

2.3 RADIO INTERFACE SPECIFIC FUNCTIONS

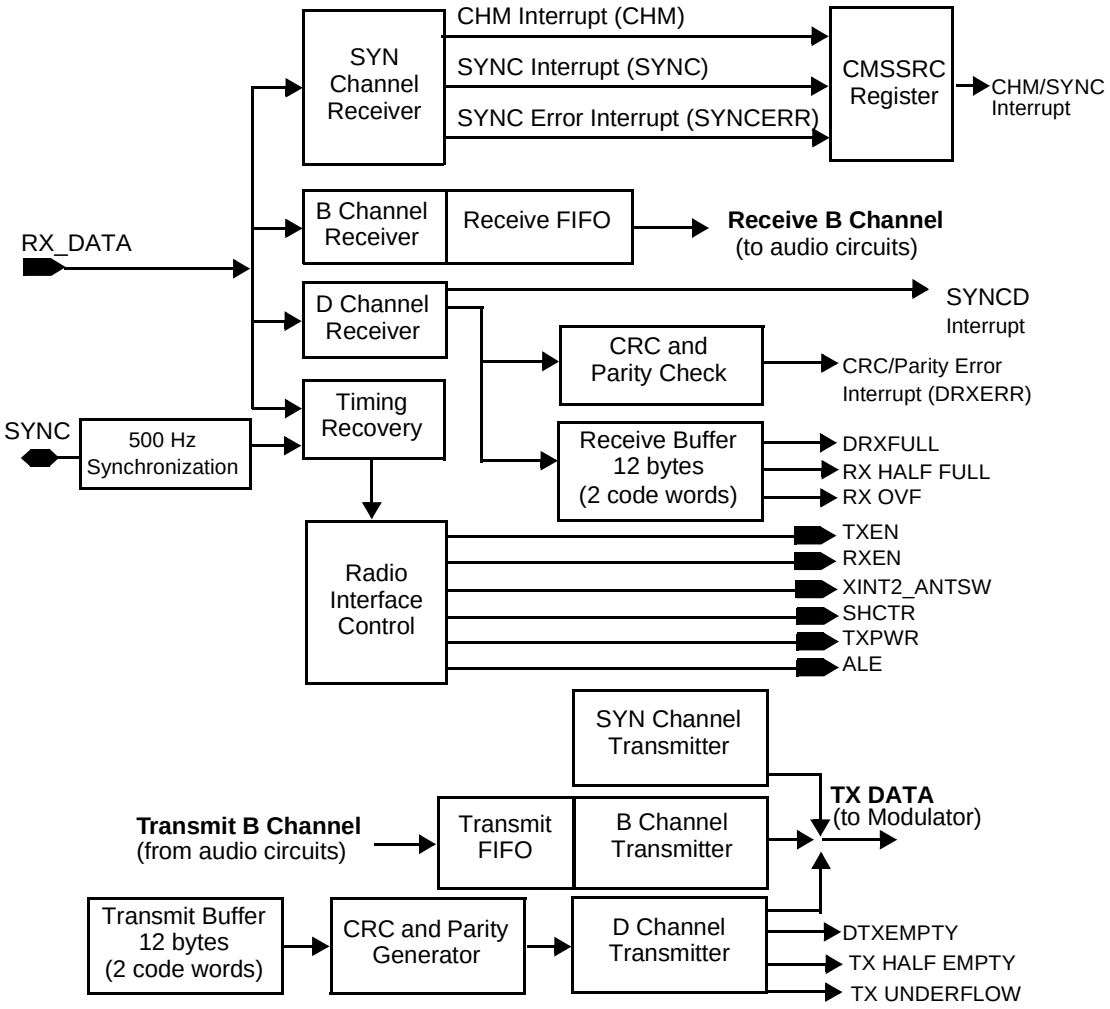
2.3.1 Digital Formatter

2.3.1.1 Block Diagram

The Digital Formatter includes a synchronization (SYN) channel handler, a control (D) channel handler with hardware CRC (Cyclic Redundancy Check), and parity generation and checking, an audio (B) channel handler, and timing recovery. Figure 2-8 is a block diagram of the Formatter.

The Formatter is enabled by programming MECTR1[3:2] to 11.

Figure 2-8 Digital Formatter Block Diagram



2.3.1.2 Device Selection: CFP/CPP

The DEVMODE register determines whether the PhoX device acts as a CFP (Cordless Fixed Part or base station) or a CPP (Cordless Portable Part or handset). The mode can be changed only while the Digital Formatter is held in Clear mode by programming the RXMUX and TXMUX registers for clear.

2.3.1.3 Multiplex Selection and Formatter Clear

The Am79C432A defines four different burst structures: MUX1.2, MUX1.4, MUX2, and MUX3. In this document, the term MUX1 refers to either MUX1.2 or MUX1.4. The multiplex modes for the transmitter and receiver are programmed in the TXMUX and RXMUX registers, respectively. Software selects the appropriate multiplex depending on the device mode and call status. In order to accommodate protocol requirements, the Receive and Transmit Multiplex modes are independent; for example, it is possible to transmit packets in MUX2 and receive packets in MUX1.2.

The Digital Formatter is in Clear mode when both RXMUX and TXMUX are programmed to 03 hex. Clearing the Formatter resets the state machines in the Formatter, but does not return user-accessible registers to their default values.

When the CPP transmits in MUX3 mode, its receiver should be programmed to receive MUX2. When the CFP is receiving in MUX3 mode, its transmitter should be programmed for MUX2 mode, and transmission should not be allowed to start until the appropriate protocol is received from the CPP.

Hardware disallows transmission of MUX1 until RXTMGR[7] indicates that the receiver is synchronized.

2.3.1.3.1 Software Notes:

1. When changing the transmit multiplex, program TXMUX while the transmit buffer is empty.
2. When the CFP switches from MUX3 to MUX2, it must release its synchronization to the CPP by writing to SYNCTR.
3. For optimal performance, the Formatter should be enabled or disabled in MECTR1[3:2] only when RXMUX and TXMUX are programmed for Clear mode. Configure all Formatter registers before exiting Clear mode. Clear MECTR1[3:2] before putting the device in Shutdown mode.

2.3.1.4 Starting and Stopping Transmission

To initiate transmission, the transmit buffer must be filled with a code word and TXDISAB[1:0] must be cleared. If the transmitting device is a timing slave, that is, a CPP in MUX1 or MUX2 or a CFP in MUX3, then it must also have synchronized its receiver by having detected a SYN channel pattern. The synchronization status can be read in the RXTMGR register.

Transmission stops at the end of the frame carrying the last bit of the current code word, including CRC and parity bits after TXDISAB[0] is set. TXDISAB[1] aborts transmission immediately at the end of the current frame. The CPP MUX3 transmission stops automatically immediately after reception of a valid SYNCF marker from the CFP.

2.3.1.5 Timing Recovery

The CFP is generally the timing master, deriving its bit-rate timing from the 12.8 MHz external clock source connected to the PhoX chip. Even as a timing master, the CFP's data recovery circuit is capable of extracting and tracking receive data bit timing in order to locate the data sampling window, but this tracking does not affect RF control signals or transmission time.

The CPP is a timing slave to the CFP in multiplex modes MUX1 and MUX2, deriving its reference timing from the receive data bit stream. This extracted timing is then used to set the transmitter timing. Adjustments to the timing are made only during the receive portion of the frame, and are based on receive data transitions.

MUX3 is the exception condition that reverses the master and slave roles of the CFP and CPP, such that the CPP is the timing master and the CFP is the timing slave. In this case, the CFP tracks the data rate of the received CPP transmission in order to completely recover the entire MUX3 data sequence.

The RXTMGR register controls timing recovery functions.

A dual-speed digital phase-locked loop recovers the receive clock based on data level transitions. High speed (651 ns/bit adjustment max) is used for quick timing acquisition (e.g., at the beginning of a MUX3 reception) and low speed (108 ns/bit max) is used to maintain phase lock once the timing reference has been established. The acquisition speed function is largely automatic, although speed can be forced to the Slow mode by programming RXTMGR[1]. The speed automatically switches to low speed when the receiver detects a SYN channel marker, as reflected in RXTMGR[6].

Receive data is sampled either once, at the midpoint of the predicted bit interval, or three times, separated by 1.7 µs centered at the midpoint of the predicted bit interval, under control of RXTMGR[2].

RXTMGR[0] is called Receive Timing Recovery Enable. It enables two functions in the CPP:

- Adjustment of data sampling according to receive data edges. Under normal conditions, the PLL attempts to locate the sampling instant 6.9 µs after the previous valid data boundary. This function allows the receiver to move the sampling point for robust reception as the data position fluctuates with variations in radio conditions and receiver slicer level tracking.
- Adjustment of receiver radio timing and transmitter timing. The receiver radio control signals as well as the subsequent transmission timing will be affected by the adjustments made by the phase-locked loop attempting to track the receive data.

The control bit must be set to allow the CPP to track the CFP timing in Muxes 1 and 2.

In the CFP, Receive Timing Recovery Enable functions differently. The radio control timing (transmit and receive) and the data transmission timing are unaffected by the phase-locked loop, regardless of the state of Receive Timing Recovery Enable. If the bit is cleared, data sampling is fixed and will be located at the middle of the adjusted ideal bit timing. The adjusted ideal bit timing is defined to be the ideal timing at the antenna, modified by the programmed modem delay. For the CFP case, setting Receive Timing Recovery Enable enables adjustment of data sampling, as described above for the CPP. In general, allowing this sampling time adjustment increases CFP tolerance to receive drift and jitter.

MUX3 is an exception for both the CFP and the CPP. Receive Timing Recovery must be enabled in both CFP and CPP in order to best recover the MUX3 frame. The CFP will actually track the receive data timing. The CPP will not track the CFP timing, but it will adjust its receive sampling location to the middle of the actual recovered bit.

Although the CFP is the radio link timing master, except in MUX3, it can be in turn slaved to the 500 Hz SYNC signal, effectively making the SYNC source the link timing master.

2.3.1.5.1 Fade Management Extensions

Several control mechanisms that improve the performance of the system (CPP/CFP) during fade conditions (loss of radio signal) include programmable phase acquisition and tracking, autotracking, and fade detection.

During signal fades, the processor can assert HOLD ADJ (RXTMGR[3]). This control stops adjustment of receive timing and maintains the latest phase information for receive data

sampling until the bit is cleared. HOLD ADJ functions only when timing recovery is enabled in RXTMGR[0].

For short-term receive phase measurement, the phase-locked loop operates in either Acquisition or Tracking mode. In Acquisition mode, the filter constant is programmed in the FAST TAU field of the PLLCTRL register (bits [1:0]). This filter constant defaults to the fastest setting of 13 µs. Acquisition ceases when a SYNC word is detected in the multiplex frame. In Tracking mode, large phase errors are de-emphasized relative to small errors, which demonstrates that the PLL has correctly settled to the appropriate phase. The loop filter constant for the Tracking mode is programmed in the SLOW TAU field of PLLCTRL (bits [3:2]). This filter constant defaults to the fastest setting of 48 µs.

The long-term frequency offset between the remote CFP's data rate and the PLL local crystal reference is evaluated by the PLL upon initial synchronization of the link and upon resynchronization. When the SYNC pattern is detected and synchronization is locked, the average of all PLL adjustments is taken over the next 32-frame period. Upon completion of the measurements, the measured frequency error is added to the CPP's PLL at all times. This feature is enabled only in the CPP by setting the LT_EN bit in PLLCTRL[7]. Frames during which fades are detected are included with the average and assumed to have been zero.

When Fade Detect is set (PLLCTRL[5]), the PLL stops evaluating data for timing recovery. In the case of the CPP, the long-term frequency offset circuit continues to add the offset to the PLL, and the CPP continues to track to CFP timing master during a deep fade. In the case of the CFP, the PLL stops evaluating data during a detected fade; however, no long-term drift offset is added.

Hardware fade detection within the PLL performs the following functions:

- During odd-numbered frames, the number of PLL timing triggers occurring outside a window around the expected periodic location (i.e., jitter events) accumulates during each frame. When the number of jitter events exceeds the event threshold programmed in the JITCTR register, a fade indicator latch is set. That latch remains set until a frame that does not violate the jitter events threshold is received. The size of the window is specified in the PHASE THRESH field of the JITCTR register.
- During even-numbered frames, the number of PLL timing triggers occurring within the expected phase window is accumulated. If that number does not reach 8 during a frame, the fade indicator latch is set, and it remains set until a frame containing more than 8 valid timing triggers occurs. This function is used for situations in which received data input ceases to toggle during a fade. Because the PLL is event-driven by data transitions, a lack of transitions otherwise fails to stimulate the PLL to maintain lock.

Occurrence of either of the two conditions above results in a jitter interrupt.

In the CFP case only, the phase-locked loop tracks bit timing within the timing window. When the receive data crosses the tracking limits, the PLL slips its timing one bit. This is undesirable in MUX1 because there are no synchronization patterns to identify the framing slip.

When the Receive Independent Timing mode is set in PLLCTRL[4], the CFP receiver data window is allowed to float with the received data. This is useful when the CPP undergoes a fade and its timing reference starts slipping relative to the CFP timing reference. The effect of this feature is to tolerate a larger degree of phase slipping to reduce the probability of a loss of synchronization that would require link reestablishment.

When the Receive Independent Timing mode is set in the CFP, the programmable delay parameter (MODDLY) is not used and defaults to a setting of 0 by setting MODTMG[1] = 1. Thus, data can be received anytime during the receiver's "ON" period (when RXEN is high). When the end of the SYNC pattern is detected within this window (MUX2), the CFP establishes the moment of detection as the frame reference for future frames. This frame reference can vary with the receive data stream from the CPP; however, the frame reference must not vary to the extent that the receive data stream is outside the receive window or a loss of Receive Data results.

2.3.1.6 SYN Channel Operation and Link Synchronization

The synchronization (SYN) channel is present in multiplexes MUX2 and MUX3 in order to gain burst synchronization. In MUX2, the SYN channel is a 10-bit preamble and a 24-bit CHM (Channel Marker) or SYNC (Synchronization) pattern. In MUX3, it is a 12-bit preamble and a CHMP (CHM for a CPP) pattern. The RXMUX and TXMUX registers control the CHM/SYNC selection for the receiver and transmitter, respectively. The polarity of the CHM or SYNC (i.e., CFP or CPP) is determined by the DEVMODE register.

The receiver searches the incoming data stream for either a CHM or a SYNC pattern and reports the synchronization status in the RXTMGR register. Once a CHM or SYNC pattern is received, a CHM/SYNC interrupt is propagated to the central interrupt controller. The cause of the CHM/SYNC interrupt is reported in the CMSSRC register. Individual bits in CMSSRC are enabled in the CMSMASK register. Once the CHM or SYNC pattern is located, the receiver frame timing remains locked. If the receiver fails to receive subsequent expected CHM or SYNC patterns, it generates a CHM/SYNC interrupt, which is reported as a sync error in CMSSRC[3], subject to masking in CMSMASK[3].

Writing the SYNCTR command releases the receiver to resynchronize by seeking the next CHM or SYNC pattern. SYNCTR must be written to initiate reception and to reestablish link timing; for example, when a CFP completes MUX3 reception and starts MUX2 transmission. Since the transmitter timing is linked to the receiver, transmissions are also stopped on a SYNCTR command.

Ordinarily, the SYN channel must be received entirely without error to cause frame timing to lock or to avoid error interrupts after frame timing is already locked. The error tolerance feature offers the option of recognizing the SYN pattern with up to one error in any bit location. It is enabled in RXMUX[3] and may be used dynamically to lock the timing to even a corrupted SYN channel and then to report any bit errors that occur after lock by switching error tolerance off.

2.3.1.7 D Channel Operation

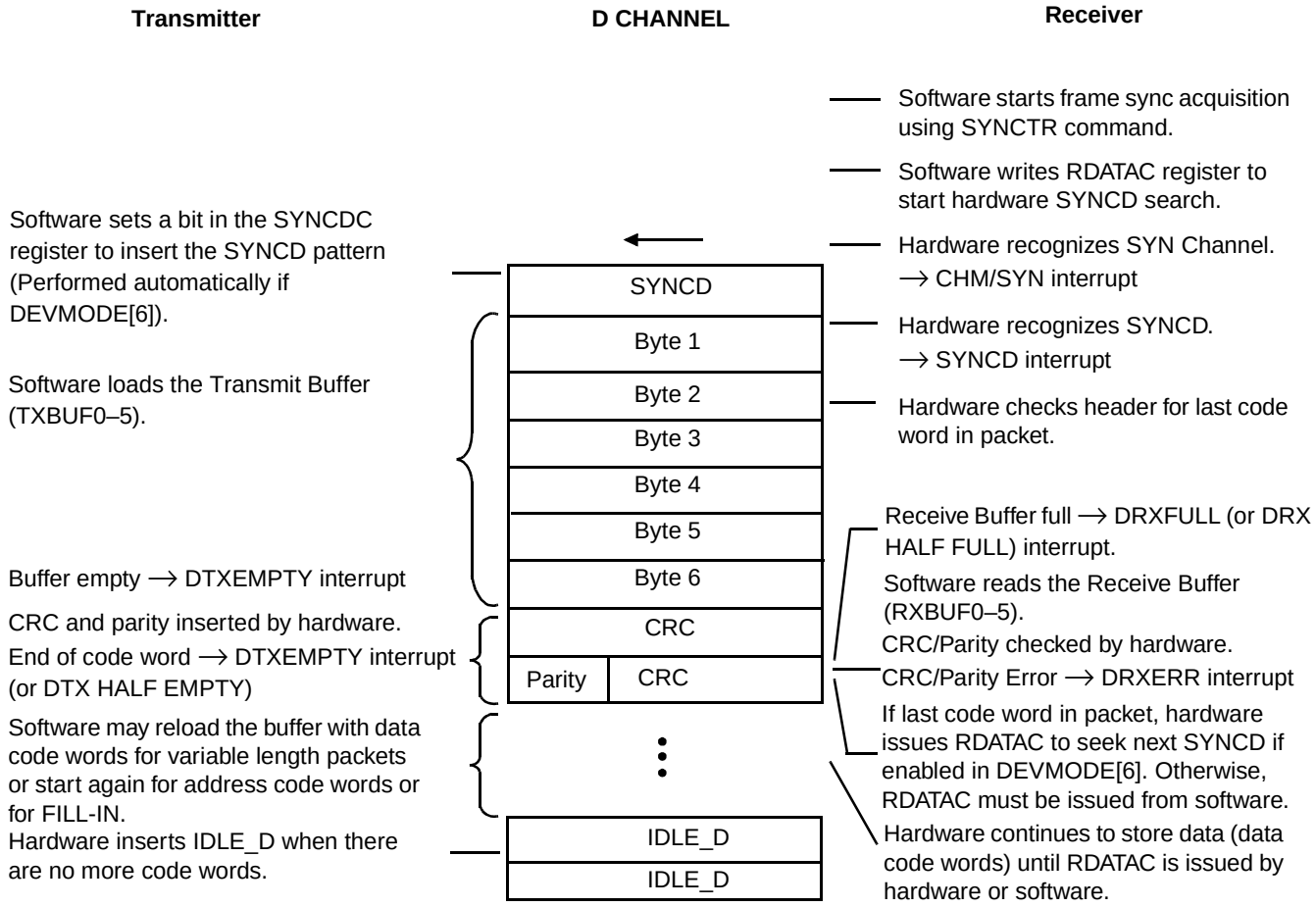
The D channel exists in all multiplexes for link management. Layer three messages consist of a number of packets, each made up of one to six code words. Code words are eight bytes long. Each code word includes six data bytes, followed by 15 CRC bits and one parity bit such that the whole 64-bit code word has even parity. The first code word of each packet is preceded with a D Channel Synchronization (SYNCD) pattern. Between packets, either a predefined FILL-IN packet or an IDLE_D pattern (alternating ones and zeroes) is transmitted to fill unused D channel bandwidth.

Hardware handles SYNCD, IDLE_D, CRC, and parity insertion and checking. Generation and interpretation of the data bytes are left to software.

The Am79C432A has double buffers capable of retaining two entire code words. Selection between single and double buffering is made in DEVMODE[6], which must be programmed while the Formatter is in the Clear mode (see Section 2.3.1.3).

Figure 2-9 summarizes how the PhoX IC operates the D channel.

Figure 2-9 Operation of the D Channel



2.3.1.7.1 D Channel Transmit Operation

When a packet is to be transmitted, software loads the transmit buffer with the six data bytes of the code word. If the actual content of the code word is less than 6 bytes, all 6 bytes need not be written, but TXBUF5 must always be written in order to trigger the hardware response. Transmission is enabled by programming the TXDISAB register. The transmitter drives the data bytes, preceded by the SYNCD pattern as necessary and followed by the automatically generated CRC field and the parity bit. When in MUX2, hardware always locates the SYNCD pattern in the last 16 D channel bits of the MUX2 frame.

The transmitter functions in Single or Double Buffer mode. Double Buffer mode is available to increase the real-time available for processing code words, especially in MUX2.

In Single Buffer mode, software must control the insertion of SYNCD by programming SYNCDC before the code word is written to the buffer. When the buffer empties, the Formatter propagates a DTXEMPTY interrupt to the central interrupt controller through the MISRC0 register, subject to masking in MIMSK0, indicating available buffer space for an additional code word. DTXEMPTY status is reported in the DCHSTAT register and occurs either when hardware reads the last transmit buffer byte or when the end of the code word (parity bit) is transmitted, depending on how DTXCTR[1] is programmed. Software must respond to DTXEMPTY within approximately 1 ms in MUX2 if the buffer requires reloading, as is the case with a data code word directly following an address code word, as shown in Figure 2-10.

The transmit buffer may be loaded with up to two complete code words if double buffering is selected in DEVMODE[6], relieving the 1 ms processing speed requirement just mentioned and allowing instead approximately 7 ms in MUX2, as shown in Figure 2-11. When double buffering is enabled, automatic SYNCD insertion is also enabled, effectively obsoleting the SYNCDC register by automatically inserting SYNCD only before all legal address code words. In Double Buffer mode, interrupts are generated when the buffer is empty and half-empty, indicating buffer space for either one or two code words. In the figure, the empty indicator at the right is shown in parentheses to demonstrate that it occurs only if software fails to write a new code word after the half-empty interrupt.

Figure 2-10 D Channel Transmit Timing Constraints, MUX2, Single Buffering

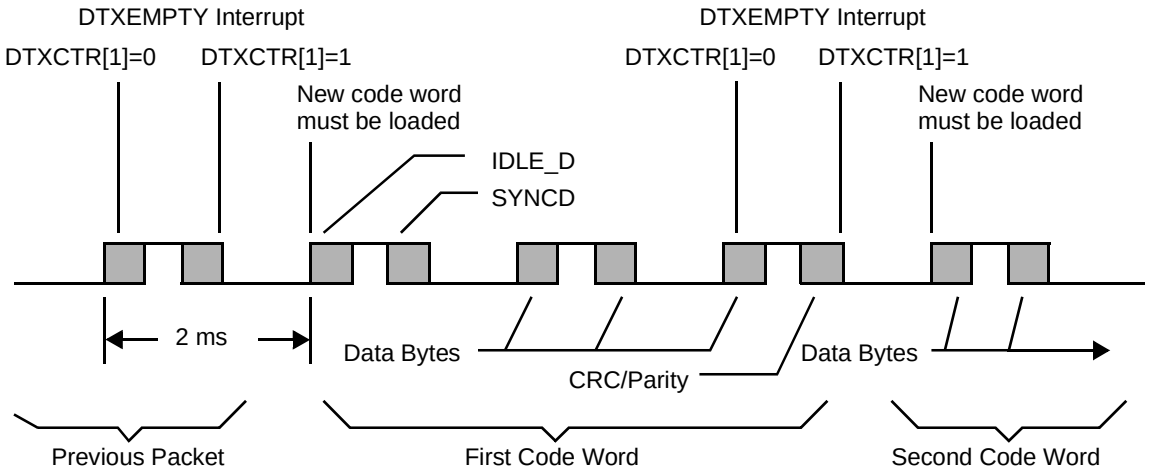
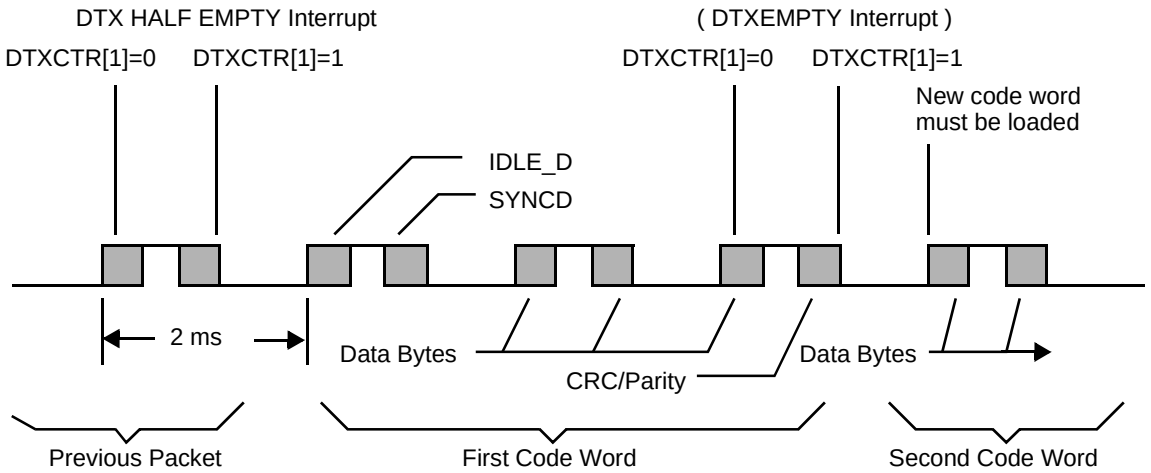


Figure 2-11 D Channel Transmit Timing Constraints, MUX2, Double Buffering



Software must observe the following programming order when using the double buffers:

1. Establish Double Buffer mode in DEVMODE[6] before enabling the Formatter.
2. Recognize Transmit Buffer Empty or Half-Empty Interrupt, if applicable.
3. Program DTXCTR, if a change is necessary.
4. Load the buffer, TXBUF0–TXBUF5.
5. Program TXDISAB, if necessary, to start or stop transmission.

After the first code word of a packet is sent, the transmitter continues transmission in one of three ways:

1. If the buffer has not been loaded with a new code word, it sends IDLE_D after the check field and parity bit.
2. If a data code word is loaded in the buffer, the transmitter begins sending new code words, prefixed with SYNCD in the case of address code words, in the next bit position after the check field and parity bit.
3. If continuous transmission is enabled in DTXCTR[0], the six bytes will be repeated in successive fixed-length packets, separated by 48 IDLE_D bits. The DTXEMPTY interrupt is not asserted in this mode.

FILL-IN: Continuous Transmission mode is intended for transmission of the predefined fixed-length FILL-IN code word in MUX2. The FILL-IN bytes must be written to the buffer in the same manner as any other code word. Once DTXCTR[0] is set, the code word will repeat indefinitely until DTXCTR[0] is cleared. Each transmitted packet is prefixed with SYNCD and separated by 48 bits of the IDLE_D pattern. In MUX1, the 48 IDLE_D bits are not inserted because that would violate the minimum code word transmission rate.

IDLE_D: When the transmit buffer empties and the last parity bit is transmitted, the transmitter automatically generates IDLE_D pattern output (alternating 1 and 0). In MUX2, each new packet marked with SYNCD is automatically preceded by 16 IDLE_D bits in the first 16 D channel bits of the transmit frame containing SYNCD. 48 IDLE_D bits are also automatically inserted between packets during continuous transmission of the same fixed-length packet.

2.3.1.7.2 D Channel Receive Operation

D channel synchronization cannot be attained until frame timing has been established with the SYN channel. The device acquires D channel packet synchronization by seeking the SYNCD pattern at the beginning of each new packet when an RDATAC command is issued. The SYNCD pattern is 1100.0100.1101.0111, in chronological order. After recognizing a SYNCD pattern, the D channel receiver drives a CHM/SYNC interrupt to the interrupt controller and starts collecting the following 6 bytes of D channel data, which are the code word bytes. The cause of the interrupt is reported as SYNCD in CMSSRC[2] and is subject to masking in CMSMASK[2].

The 6 D channel bytes are loaded in the receive buffer. The following 16 bits of CRC and parity are routed to a CRC/parity check circuit, which generates a DRXERR interrupt in case of error. At the end of the check field reception, the DRXFULL interrupt notifies software that the receive buffer contains a code word. The check field is not loaded in the receive buffer. DRXERR and DRXFULL interrupts are reported in the DCHSTAT register and are forwarded to the MISRC0 register in the interrupt controller, masked by MIMSK0.

Two tasks must be completed at the end of each code word: the code word must be read from the buffer and the decision to resynchronize the D channel must be made. If the buffer is not read by the time the beginning of next code word arrives, the new code word will be

lost and an overflow interrupt will occur in the CRC/Parity Error indicator. Enabling the double buffers increases the real processing time available for the higher layer software of the receiver, extending the maximum processing time from 1 ms to approximately 7 ms in MUX2. Double buffers are enabled in DEVMODE[6].

The D channel must be resynchronized after every packet before a new packet can be received, but it must not be resynchronized between code words within a variable length packet. The decision to resynchronize the D channel can be done in either hardware or software. Hardware determines whether the code word just received is the last of the current packet, as defined by the *FT* and *endwrd* bit (bit 5) of the first byte. If the DEVMODE[6] is set, hardware will automatically issue an RDATAC command to begin a new search for SYNCD if the code word just received was the last of its packet and was received without CRC, parity, or overflow error. Error conditions require software intervention using the RDATAC command to clear D channel synchronization. The D channel synchronization clear function can be controlled completely by software by clearing DEVMODE[6] and using the RDATAC command. If this function is performed in software, the decision to issue RDATAC must be evaluated before reception of the next code word begins.

Note: *Software always has responsibility for issuing the first RDATAC to initiate D channel reception.*

2.3.1.7.3 Alternate Mux Mode (D Channel Training)

The default for the Training mode is disabled (DEVMODE[5]=0). Enable channel training by setting the register (DEVMODE[5] = 1).

To allow the demodulator and receiver to reacquire steady state after the transmit portion of the frame, MUX1.4 and MUX2 allow the initial D Channel field bits to be used as dummy bits. For the transmit frame, the first half frame's D Channel bits are zeroed. For the receive frame, the first half frame's D Channel bits are ignored. (In MUX1.4, the half frame D Channel is a 2-bit field; in MUX2, it is a 16-bit field.) This reduces the overall message rate to half of the normal rate.

2.3.1.8 B Channel Operation

The B channel handler aligns the 64 B channel ADPCM audio bits within the MUX1 transmit and receive frames and scrambles the data in order to ensure reasonably random output data sequences for timing recovery and spectral considerations. In the transmitter, bits 3, 4, 6, 9, 14, 16, 18, 19, 20, 22, 23, 27, 28, 29, 30, 31, 34, 35, 37, 40, 45, 47, 49, 50, 51, 53, 54, 58, 59, 60, 61, and 62 are inverted (scrambled). In the receiver, these bits are reinverted (descrambled). The B channel is inhibited until RXTMGR[1] indicates that the receiver is synchronized.

The B channel may be enabled by programming the BVALID register, allowing data flow between the air interface in MUX1 and the PhoX chip audio circuits. Before BVALID is asserted, transmit B channel data is forced to zero. The 8 kHz frame clock must be enabled in MECTR1[4] for a minimum of 1.25 ms before asserting BVALID. It is recommended that the B channel source and destination (i.e., audio mux, codec, B channel port, or encryption port) be initialized before setting BVALID.

The total round-trip B channel delay, including A/D conversion, radio transmission, radio reception, and D/A conversion, is approximately 1.94 ms.

The 8 kHz ADPCM frame synchronization clock, which may appear on the BDP2_OUT4 multifunction pin as the CLK8K signal, tracks the recovered timing and may jitter by as much as ±108 ns per 125 µs frame when the Formatter receive timing recovery is enabled in the CPP.

2.3.1.9 Setting Modem Delay

2.3.1.9.1 RF Delay Compensation

In a wireless system, there is an inherent delay between when a data stream leaves the baseband section of the transmitter and when it arrives at the baseband section of the receiver. The transmitted data experiences a delay $t_{TXMOD} + t_{TXRF}$ due to the modulator and the transmitter RF section, while in the receiver this data passes through the receiver RF circuitry and demodulator, thereby experiencing a time delay t_{RXRF}. This propagation delay (known as the modem, or RF delay) is therefore the *total* delay through each of the two transmit-receive paths between the handset and base station. The receive filters are typically the major cause of this delay. The modem delay is expressed by the term t_{MDM}:

$$t_{MDM} = t_{TXMOD} + t_{TXRF} + t_{RXRF}$$

There is a fixed timing relationship (time gap) between the receive and transmit subframes of the formatter protocol, which is represented by the following equation:

$$t_{CxP(RX) \rightarrow CxP(TX)} = t_{RXRF} + t_{ADJ} + t_{TXMOD} + t_{TXRF}$$

where the left side of the equation is the time gap between the last received bit of one frame and the first transmitted bit of the next frame for the CFP or CPP; that is, 4.5 bit periods in MUX1.4, and 6.5 bits in MUX1.2 or MUX2 (see Figure 2-12). The term t_{ADJ} is the adjustment that is necessary to compensate the right-hand side of the equation. Thus,

$$t_{CxP(RX) \rightarrow CxP(TX)} = t_{MDM} + t_{ADJ}$$

The PhoX device utilizes the Modem Delay register (MODDLY) for t_{MDM}, then determines the term t_{ADJ} to compensate for the RF delay. Thus, t_{MDM} is a static, user-defined value of propagation (or modem) delay. t_{ADJ} is a dynamic, automatic adjustment conducted by the PhoX device, which applies this value to the transmit controller to achieve consistent system timing.

Because every radio design has a unique propagation delay, this value must be determined for each. The delay value can be found manually with a digital storage oscilloscope, or the delay value can be determined automatically by software with a radio loopback configuration. The manual method is the most straightforward of the two techniques.

2.3.1.9.2 Manual Measurement

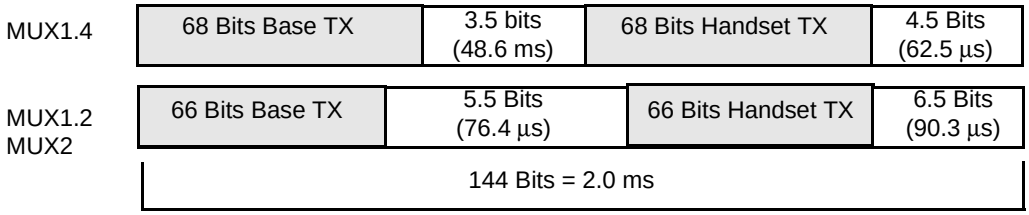
The manual method assumes that the same radio design is used for both the handset and base station, and that the transmit and receive delays are closely matched. The base station's independent receive timing should also be disabled (PLLCTRL = 00, and MODTMG = 00).

During system development, an initial value of t_{MDM} (modem delay) is determined by a laboratory measurement of propagation delay from the baseband transmit of one end to the baseband receive of the other. Convert this measurement (as outlined in Section 3.17.21) and write the resulting value in the MODDLY registers of both the handset and base station.

After a preliminary modem delay is determined and stored in the MODDLY registers, the system should be able to establish a link between that handset and base station. During initial development, establish this link from the base station such that both sides communicate in MUX2. If a voice link can be established, however, the system will communicate in MUX1.x. Establish the link and connect a 2-channel digital storage oscilloscope to the TXI pin on the PhoX devices of both the handset and base station. If the IQ Analog mode (MODTST[4]=0) is used, set BDMUX [6:5] = 11 and take measurements using the BDP1_OUT3 pin instead of TXI.

Verify the gap timing between the transmit frames for the appropriate MUX(1.x or 2). Simultaneously adjust both values of MODDLY such that the frame timing corresponds with Figure 2-12. The correct MODDLY is the same value for both the handset and base station.

Figure 2-12 Frame Timing of MUX1.x and MUX2



Observe the relationship between SHCTR and RX_DATA to finely adjust MODDLY. This measurement is made while the base station is linked with the handset in MUX1.x or MUX2.

First, observe SHCTR and RX_DATA at the handset. As the handset sample-and-hold window tracks the data, the falling edge of the last bit of data and the falling edge of SHCTR should be aligned. If not, the value of MODDLY programmed in the handset is incorrect and must be readjusted by measuring the propagation delay.

Next, observe SHCTR and RX_DATA at the base station. With the base receive tracking disabled, the SHCTR window depends only on the MODDLY setting. Verify that the next-to-last bit transition occurs 13.89 µs before the falling edge of SHCTR, shown in Figure 2-13. The two signals appear if the MODDLY settings are not optimal, shown in Figure 2-14.

Compensate for any deviation from this 13.89 µs value by equally adjusting the handset and base station MODDLY registers. For example, if the time between the next-to-last transition and the falling edge of SHCTR is 8.7 µs, the total modem delay should be increased by (13.89 – 8.7) = 5.19 µs, ~ 6/16 bit. Therefore, increase both handset and base MODDLY values by 3/16 bit.

Figure 2-13 Correct Timing Relationship between SHCTR and RX_DATA for MUX1.x or MUX2

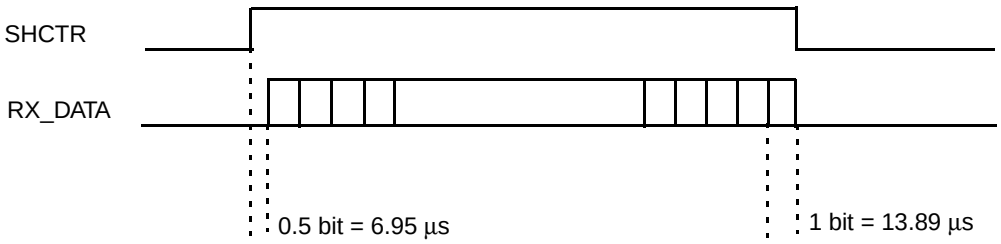
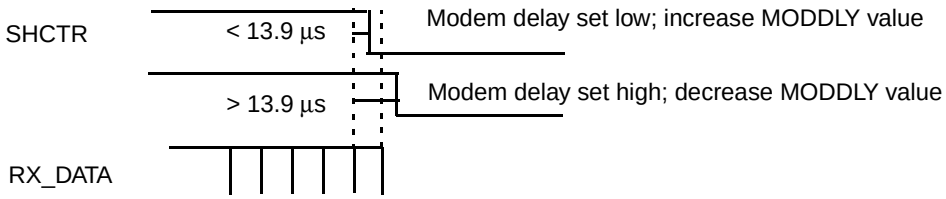


Figure 2-14 Fine Adjustment of MODDLY



2.3.1.9.3 Automatic Measurement

The automatic modem delay measurement has two requirements: the transmit and receive frequencies must be the same, and the radio section has the means to loop the transmitted radio signal at the antenna back to the receiver continuously during the procedure. The measurement operation (typically set to execute at power-up) is initiated by a software command in the MODTMG register. During the delay measurement, the transmitter and receiver are simultaneously enabled; that is, the TXEN and RXEN pins are both High, so that the transmit data goes through the transmitter to the antenna, loops back to the receiver, and returns to the PhoX device. The measurement circuit counts the delay between transmission and reception of CHM and returns the result, t_{MDM}, in the MODDLY register. The following equations show the relationships of the propagation delays:

$$t_{MDM} = t_{TXMOD} + t_{TXRF} + t_{RXRF}$$

$$t_{CxP(RX)} \rightarrow {}_{CxP(TX)} = t_{MDM} + t_{ADJ}$$

MODTMG[1] controls whether the measured delay t_{MDM} is used by the frame formatter and normally should remain cleared. If MODTMG[1] is set, however, t_{ADJ} works as if t_{MDM} is zero.

To measure delay, the following sequence must be included in the protocol software for execution upon power-up:

1. Initialize the transmitter mode: TXMUX = 02 for CFP, TXMUX = 03 for CPP
2. Initialize the receiver mode: RXMUX = 02 for CFP and for CPP
3. Load the D channel transmit buffer, TXBUF
4. Set the MEASURE DELAY bit in the MODTMG register: MODTMG = 01
5. Enable receive timing recovery: RXTMGR = 01
6. Enable transmission by clearing TXDISAB[1:0]
7. Poll the MEASURE DELAY bit, MODTMG[0], until it is cleared by hardware, indicating completion of the measurement. If the delay exceeds 6.9375 bits (96 μs), the measurement will fail and hardware will not clear the MEASURE DELAY bit, indicating an RF error. This requires a software timeout.

Note: *The radio control signals TXEN, RXEN, SHCTR, and ANTSW remain active High during the modem delay measurement procedure.*

The measured delay in MODDLY may be moved to nonvolatile memory, such as EEPROM, for use in future link initiation sequences. To force the modem delay compensation to any arbitrary value or to a previously determined value, software writes the value to MODDLY and clears MODTMG[1].

2.3.1.10 Radio Interface

Figure 2-15 shows the basic radio interface signals. These basic signals and others that are not shown in Figure 2-15 are described in Table 2-7.

Figure 2-15 Programmable Timing of RF Interface Controls

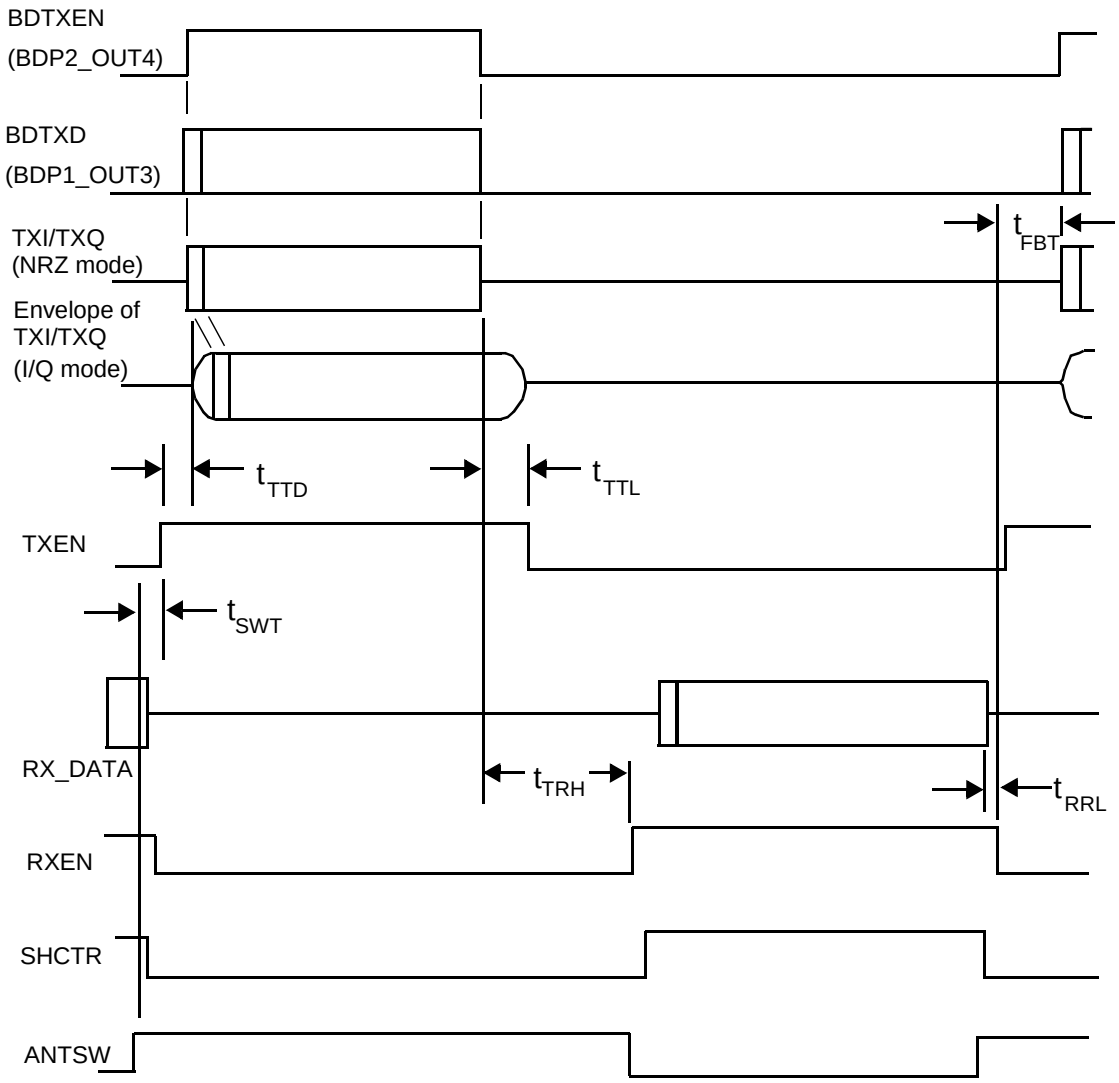


Table 2-7 Radio Interface Signals

Name	Signal	Description
Transmit Window	BDTXEN	Provided for utility in testing and development, the BDTXEN signal appears on the BDP2_OUT4 pin when appropriately programmed in BDMUX[6:5]. BDTXEN is High while transmit data BDTXD is active.
Transmit Data	BDTXD, TXI/TXQ	Transmit data appears in either NRZ (pseudo-digital) or analog I-Q form at the TXI and TXQ pins, as described in Section 2.3.3. It can also appear in true digital form as the BDTXD signal on the BDP1_OUT3 pin when that pin is appropriately configured in the BDMUX register. In this case it is also accompanied by a 72 kHz clock BDTXCLK on pin BDP0_OUT2 (not shown), which rises at the beginning of each new bit. Analog I-Q data lags its digital equivalent by approximately 15.1 µs.
Transmit Enable	TXEN	The programmability of the rising edge of TXEN with respect to unfiltered digital transmit data is 868 ns ≤ t_{TTD} ≤ 32.1 µs in 3.47 µs increments, programmed in TDELAY[7:4]. The programmability range of the falling edge of TXEN with respect to transmit data is 4.3 µs ≤ t_{TTL} ≤ 46 µs in 3.47 µs increments, programmed in TDELAY[3:0].
Receive Data	RX_DATA	The RX_DATA pin is the digital receive data input. The input is assumed to have been acted upon by an external FM discriminator followed by a slicer circuit, the purpose of which is to determine digital bit boundaries from the down-converted analog baseband signal by comparison to a varying reference voltage. The external slicer should include some amount of hysteresis for noise reduction and the RX_DATA signal should have a rise time on the order of 1 µs or less for optimal timing recovery response. Input to the slicer should be band-limited so that noisy radio conditions do not create numerous data transitions during the receive window, as this may also negatively impact timing recovery. The pulse widths of data presented to the PhoX chip on the RX_DATA pin influence timing recovery and will be affected by the external data slicer circuit. As the slicer level adjusts to balance the relative pulse widths of binary 1s and 0s, the nominal 13.88 µs pulse width will vary. In order to guarantee initial recognition of the first SYN channel pattern presented to the pin, the pulse widths of data bits input to the RX_DATA pin during the SYN channel must be within the range 13.88 ± 1.735 µs. In the absence of significant jitter, pulse widths as low as 7.3 µs will be accommodated, but synchronization will take longer on average, degrading proportionally to the slicer imbalance. Once synchronization is achieved, tolerance to pulse width variation improves. In the absence of jitter, pulse widths as low as 7.3 µs will be tolerated without error or loss of synchronization. Jitter will naturally degrade this performance, with tolerance being reduced proportional to the severity of the jitter.

Name	Signal	Description
Receive Enable	RXEN	The programmable delay from the end of digital transmit data to RXEN High is 11.3 µs ≤ t_{TRH} ≤ 87.6 µs with 3.47 µs resolution, programmed in RDELAY[4:0]. RXEN always falls t_{RRL} ≅ 6.9 µs after the last data bit is received on RX_DATA. If programmed in Independent Receiver mode (PLLCTRL[4] = 1), then RXEN falls to RXEN t_{FBT} prior to the next occurrence of transmitted data. The time of fall before transmit (t_{FBT}) delay is programmed in RXFALL[3:0] and defaults to 54.7 µs. RXEN can also be forced High regardless of the activity state of the Digital Formatter to enable the radio receiver for scanning, programmed in RDELAY[5].
Slicer Control	SHCTR	The sample/hold control (SHCTR) pin provides timing for an external sample/hold circuit that may be used to control DC offset in the receiver slicer.
Transmit Power Control	TXPWR*	The TXPWR pin is a control output synchronized to the frame timing and is controlled by software through the TPOWER register to accommodate two levels of RF power output. Depending on RF timing, TXPWR could be used alternatively for antenna diversity control.
Antenna Switch	ANTSW	Additionally, there is an output control called ANTSW (Antenna Switch), intended to switch the antenna between the receive and transmit functions. ANTSW always goes High t_{SWT} ≅ 6.9 µs before TXEN rises, and goes Low when RXEN goes High. The ANTSW signal is multiplexed on the XINT2 pin and is enabled for the ANTSW function under software control by programming RDELAY[6].

* *The signals are not shown in Figure 2-15.*

2.3.1.11 FDD Mode

Frequency Division Duplex (FDD) mode is a variation of the standard protocol in which TX and RX no longer utilize the usual Time Division Duplex (TDD) mode. This mode transmits and receives continuously at 36 kbits/s, and expects that the radio has separate frequency bands to carry the transmit and receive signals such that they do not collide. FDD mode is enabled by programming DEVMODE[3] = 1; Receive Independent Timing mode must be enabled by programming PLLCTRL[4] = 1.

In FDD mode, the RXEN pin for receive radio power is always on, and the TXEN pin is on whenever the transmitter is enabled. Receive data is expected on the RX_DATA pin as before, but transmit data must use the NRZ Output mode of the TXI and TXQ pins, shown in Figure 2-20.

FDD mode supports only MUX1.4 for audio transport. The other MUXs operate similarly to the TDD MUX modes in the ordering of the bits in time. Each bit lasts twice as long as the TDD bit period, and transmit and receive occur continuously at the same time.

MUX3 in FDD mode sends a data stream identical to a MUX2 stream, but allows the CPP to transmit when not synchronized to the base, as in TDD mode. When using the MUX modes in FDD, the sync patterns (CHMF, SYNC) are the same as in TDD mode, but the physical data stream occurs at one half of the data rate, and simultaneously transmits and receives.

2.3.2 RSSI

The RSSI (Receive Signal Strength Indicator) determines the signal level at the RSSI analog input pin. This circuit consists of a 5-bit successive approximation A/D converter requiring approximately 10 us for conversion time, during which the RSSI pin should be held constant, within 1LSB of resolution. The input is high impedance, allowing the RSSI level to be generated across an external resistance driven by a current source. The RSSI is enabled only when MECTR1[0] (address FFEC) is set; it operates in two modes (MODE1 and MODE2), as determined by RSSICFG[2] (address FF4C). The default mode is MODE1 to maintain compatibility with RSSI operation on the Am79C432.

2.3.2.1 MODE1

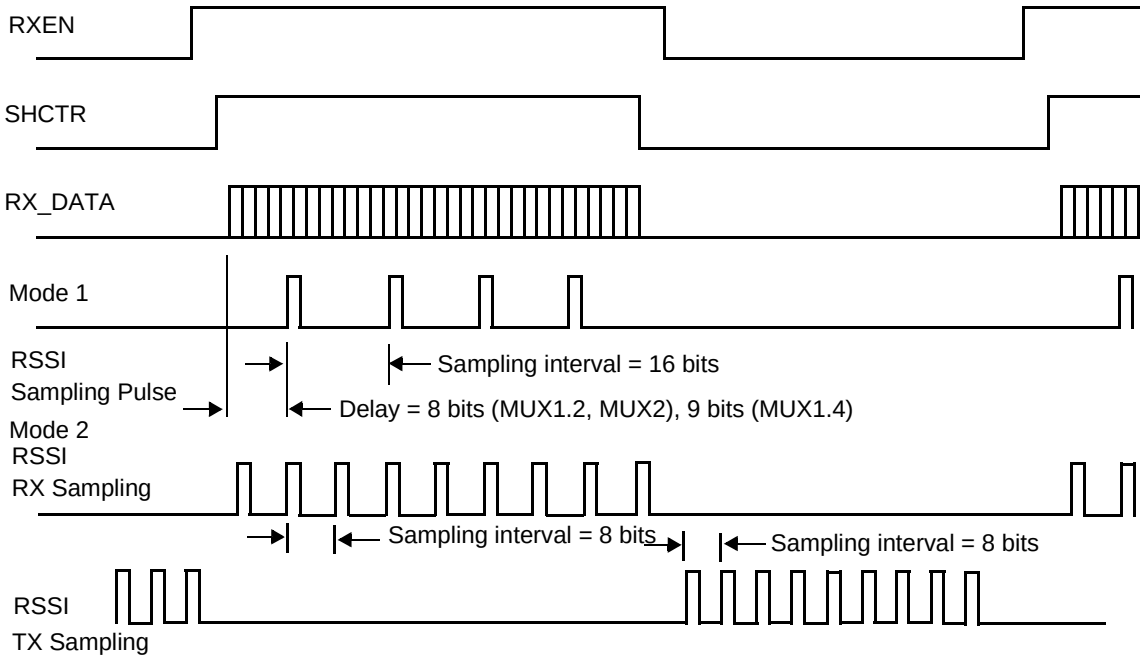
In MODE1 operation (RSSICFG[1] = 0, address FF4C), RSSI conversions are requested by setting RSSISTAT[7]. Upon completion, the hardware clears this bit and valid results are stored in RSSISTAT[4:0]. During asynchronous operation, the conversion is started immediately upon the setting of RSSISTAT[7]. During synchronous operation, the conversion is synchronized to the next timing signal, which occurs during the receive window every 16th bit (see Figure 2-16).

2.3.2.2 MODE2

MODE2 operation (RSSICFG[2] = 1, address FF4C) includes the capabilities of MODE1 and additional capabilities to allow PCI (Personal Communications Interface) interoperability, as defined by the TIA standards Committee. This standard is based upon the CT2 CAI specification with changes to comply with the use of the Unlicensed Personal Communications Services (U-PCS) frequency band. MODE2 allows the RSSI measurements during the transmit and receive windows of the transmission frame; thus, it is capable of detecting the Peak Signal Level in these windows. The software can determine the presence of another signal in the transmit window and select another channel if the interfering signal exceeds a predetermined threshold. MODE2 can make measurements synchronously, continuously, and asynchronously.

Receive and transmit RSSI conversions are initiated by setting RSSISTAT[7] and RSSISTAT[5], respectively. When an appropriate reading has been made, hardware will clear the respective request bit. If RSSICFG[0] is set, then conversions will continue until it is cleared, with the peak value held. The receive or transmit value is reported in RSSISTAT[4:0], depending on the state of RSSICFG[1]. During a Transmit window RSSI measurement, the TXENRF, RXENRF, and ANTSW pins remain in their respective receive states, and the TXI and TXQ pins are held at the reference voltage to prevent interference from the transmitter. However, ANTSW interrupts seen through the XINT2 pin are still generated even though the pin is not moving to maintain frame information to the microcontroller.

Figure 2-16 RSSI Timing in Synchronous Mode



2.3.3 Baseband Output Driver

The baseband output driver drives data in one of two modes, GMSK or NRZ, defined by the control bit MODTST[4]. There is also a test mode for RF development and test, described in Section 2.5.2.

2.3.3.1 I-Q Mode

The default mode is I-Q. In this mode, the modulator is a baseband Gaussian-filtered minimum shift key (GMSK) modulator. Serial transmit data from the Digital Formatter is digitally filtered and converted to two single-ended quadrature analog outputs, called TXI and TXQ. The outputs are intended to be externally mixed with the IF or RF carrier and summed to obtain the desired frequency-modulated signal.

The Gaussian filter response is approximated as a sixth-order Bessel filter with linear phase response and a 3 dB cut-off frequency of 57.6 kHz (i.e., the normalized 3 dB bandwidth $B_bT = 0.8$). The D/A conversion samples at 4.608 MHz with 7-bit precision over a ±0.5 V AC range, DC referenced to the MREF pin. *Net delay through the modulator, from digital input to analog output, is approximately 15.1 µs.*

The mathematical description of TXI and TXQ, depicted in Figure 2-17, is:

$$TXI = 0.5\ V \bullet I(t) + MREF$$

$$TXQ = 0.5\ V \bullet Q(t) + MREF$$

$$I(t) = \sin\left(\oint \omega_m(t)dt\right)$$

$$Q(t) = \cos\left(\oint \omega_m(t)dt\right)$$

where $\omega_m(t)$ is the instantaneous GMSK message frequency, which has a range of ±18.0 kHz, and the step response defined by the digital filter. Outputs are defined such that

when I and Q are subjected to a quadrature mixer and a carrier ω_c, as in Figure 2-18, the result y(t) is:

$$y(t) = I \bullet \cos(\omega_c t) + Q \bullet \sin(\omega_c t) = \sin\left(\omega_c t + \oint \omega_m(t) dt\right)$$

The instantaneous frequency of y(t) is then $\omega_c + \omega_m$ and there are no sidelobes. The frequency eye diagram of y(t) is shown in Figure 2-19.

Figure 2-17 Modulator Waveforms

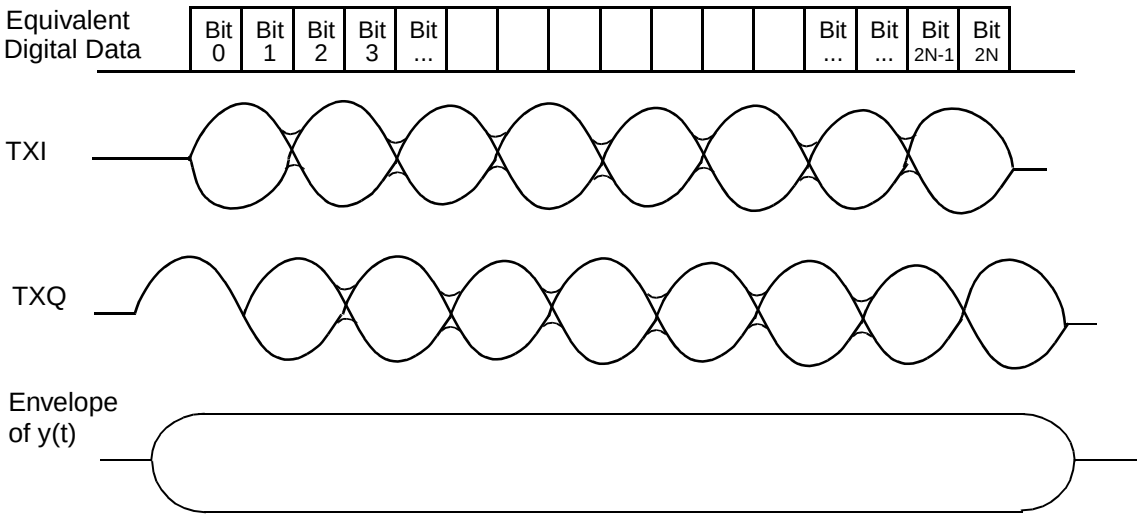


Figure 2-18 Modulator I/Q Mixer Block Diagram

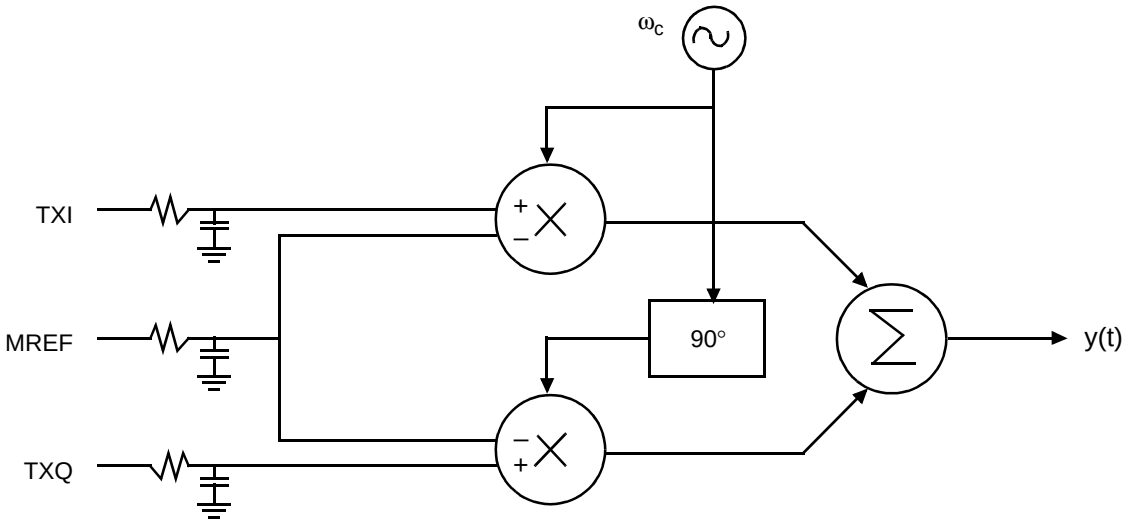
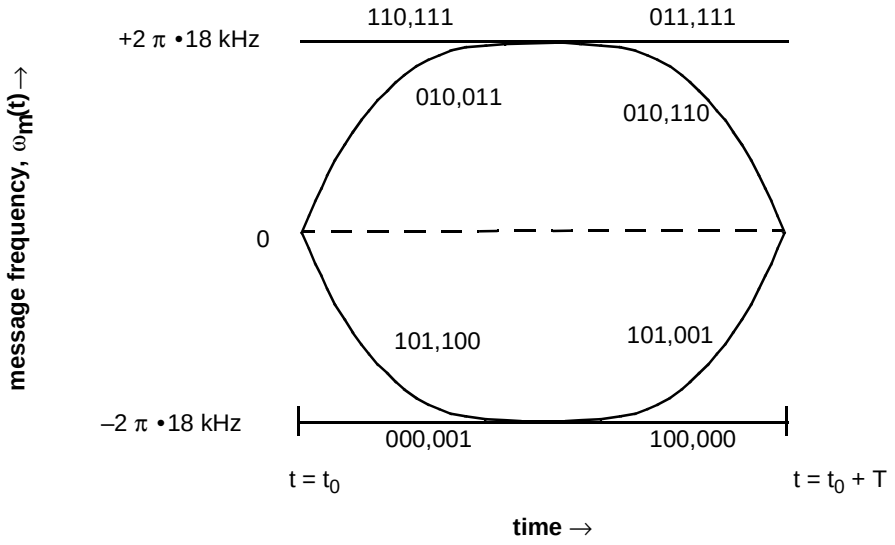


Figure 2-19 Modulator Eye Diagram for Three-Term Data Sequences



A passive single-pole low-pass filter with 3 dB frequency around 100 kHz is necessary at both TXI and TXQ outputs to remove sampling images at 4.608 MHz. The filter must have a minimum impedance of 1 kΩ. For stability, the maximum capacitance from pin to ground cannot exceed 100 pF.

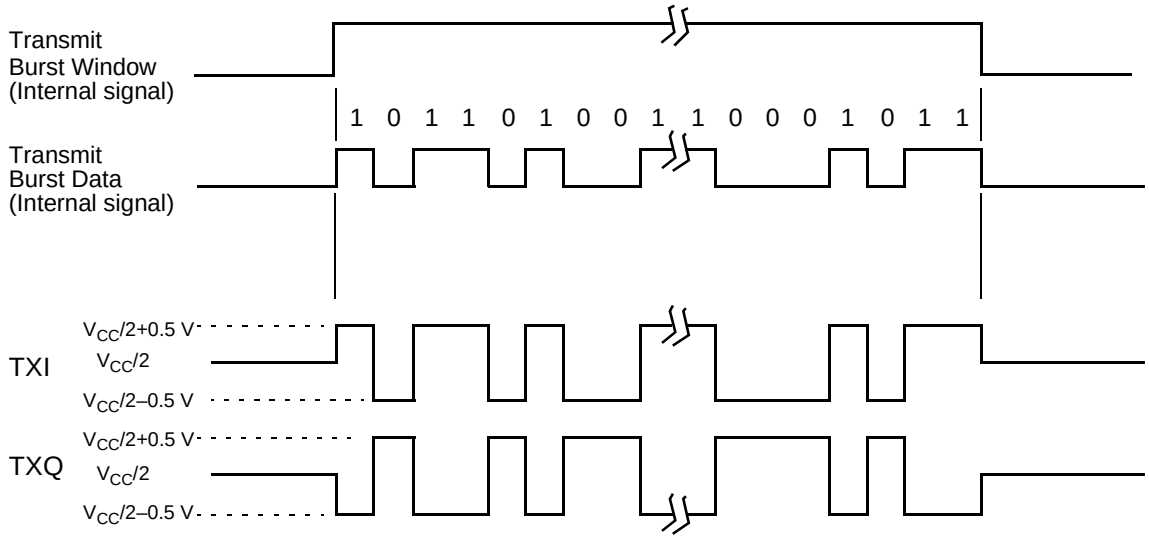
To reduce frequency spread, the modulator ramps up smoothly when transmit data is driven to it from the Digital Formatter. During the ramp-up period, I is zero and Q rises from zero to full scale so that the amplitude of y(t) increases smoothly from zero to full scale. Likewise, the modulator ramps down smoothly at the end of the transmission. Note that there remain two points of inflection at the beginning and ending points of the envelope of y(t) requiring external smoothing.

The modulator must be enabled in MECTR1[5] to function and respond to the transmit data without software intervention. The MODTST register provides test modes, enabling the modulator to send fixed or externally-generated data patterns for RF circuit evaluation.

2.3.3.2 NRZ Mode

NRZ (Non-Return to Zero) mode creates a pseudo-digital waveform and is enabled by setting MODTST[4]. The output appears at the TXI and TXQ pins as a square wave of ±0.5 V amplitude biased around $V_{CC}/2$, as shown in Figure 2-20.

Figure 2-20 NRZ-Format Output



2.3.4 Fade Management

The PhoX Controller offers many indicators allowing development of proprietary software algorithms to handle signal fades and interference conditions. These conditions can result in bit errors and even the loss of synchronization. Link quality indicators include the RSSI level, the D channel CRC and parity check, the SYN channel error check, the jitter indicator, the B channel noise indicator, and the 4-zero ADPCM detector. All of these factors can be considered in developing a comprehensive link maintenance algorithm. With the exception of the RSSI level, all indicators are available as interrupts.

2.3.4.1 Handling the Link

After software determines that a signal fade or interference condition exists, it may elect to program the CFP PLL timing recovery enable bit RXTMGR[0] to disable timing recovery. Disabling timing recovery forces receive data sampling instants to known locations relative to the CFP's own transmission timing. Radio control timing is unaffected. All of the link quality indicators remain operational so that they can be used to determine when the fade ends.

At the CPP, software can force the PLL into its Slow Response mode by programming RXTMGR[1]. This mode allows PLL adjustment for light fades, but limits the PLL response to adjustment by approximately 108 ns per 13.88 µs bit. The response of the PLL to random digital noise is to remain fairly stable around 0 ppm, relative to the CPP frequency reference. When the PLL is not forced into a slow response, it may be triggered by excessive jitter to reenter its Fast Acquisition mode.

At the physical layer, the receive data input (RX_DATA) pin should be preconditioned to minimize the number of erroneous data level transitions that may occur within one bit period under noisy conditions.

2.3.4.2 B Channel Noise Suppression

Bit errors or poor link quality adversely affect voice channel performance and in some cases can result in noise bursts at the earpiece. Noise suppression is an automatic feature enabled in DSPCTR[7] when the codec is in Normal mode, which immediately mutes the receiver under noisy conditions. Mutes may also be performed under software control.

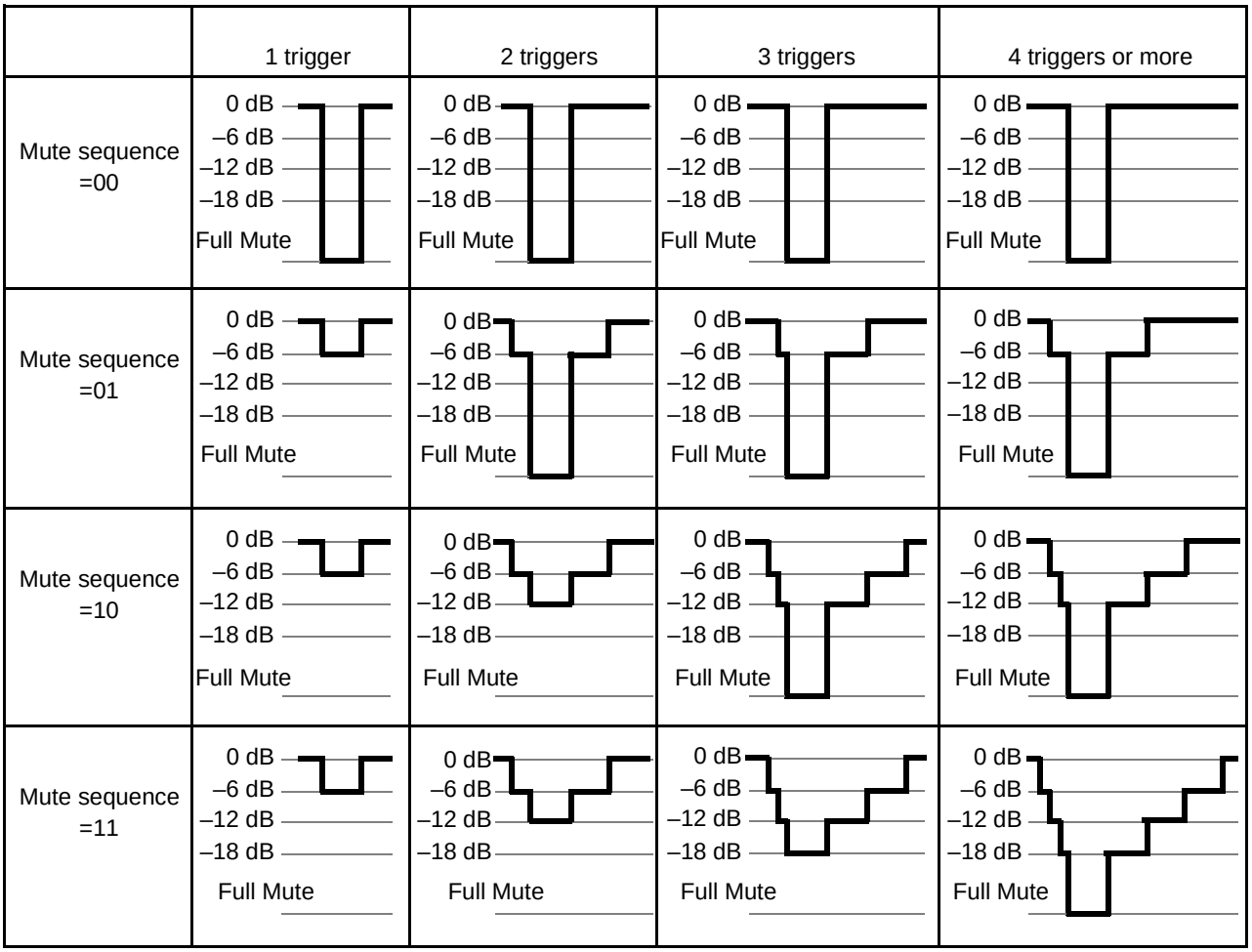
B channel noise is detected in two ways:

1. Non-speech B channel content, indicating bit errors
2. Jitter in the received data, indicating poor reception quality or likely loss of link synchronization

2.3.4.2.1 Automatic Noise Suppression

The NSCTR register, bits [3:2], select whether the noise suppression algorithm responds to bit errors or jitter. NSCTR[1:0] defines how the algorithm responds to noise indicators, as shown in Figure 2-21. The bits control the number and size of the attenuation steps applied to the receive data in the muting sequence. Noise generally arrives in bursts, so the four columns of Figure 2-21 show the response of the noise suppression algorithm to multiple consecutive noise events (triggers) as a function of the mute sequence, NSCTR[1:0]. Each new trigger causes increased muting until the maximum muting for a given programmed mute sequence is reached. The MUTE register controls the length of each attenuation step during the recovery. At each new trigger, the mute length counter is restarted, and if the counter reaches its programmed endpoint, one attenuation step is removed. Figure 2-21 assumes that the noise triggers occur near the beginning of the sequence, and that none occur during the recovery phase. If a trigger does occur during the recovery phase, muting again increases one step per event until the maximum muting is reached and the mute length counter is restarted.

Figure 2-21 Noise Suppression Muting Sequence



2.3.4.2.2 Software-Controlled Noise Suppression

Jitter and B channel noise trigger information is available in interrupt form to the processor, allowing proprietary noise suppression software algorithms by applying a loss at RXATTN in the codec. Both interrupts appear in MISRC0[5], with corresponding status bits in NSCTR[7:6].

2.3.4.2.3 Noise Suppression Triggers

Noise due to bit errors results in B channel waveforms outside normal human speech patterns. This type of noise is given the name DSP noise, because it is detected by analyzing the contents of the B channel in the codec digital signal processor. The noise detector calculates the ratio of the predicted received signal to the difference between the predicted and actual received signals, and generates a muting trigger when the ratio falls below the threshold programmed in the NSTHR register. Therefore, increasing NSTHR causes the trigger to be more sensitive to noise and more apt to falsely trigger on genuine non-noisy speech. Lowering it causes it to be more tolerant.

B channel noise triggers are reported in NSCTR[6], enabled by NSCTR[5], and cause an interrupt, shared with the jitter interrupt, in MISCR0[5].

The JITCTR register defines an integrating mechanism to count jitter occurrences and generate noise suppression triggers. The jitter phase threshold field of JITCTR determines

how large a jitter event must be, in degrees, relative to the expected ideal receive data transition time to be considered significant. The jitter event threshold field determines how many significant jitter events must occur within one frame period to merit a noise suppression muting response.

Jitter-based triggers cause the jitter interrupt (MISRC0[5], MISMK0[5]) and are reported in NSCTR[7], so that software may respond to excessive jitter, which might occur when a link fails.

2.3.4.2.4 4-Zero ADPCM Detect

The B Channel receiver can detect the presence of the 4-zero ADPCM word when in MUX1. The 4-zero code is not generated by the ADPCM transmitter and therefore represents a bit error, a disabled remote B Channel, or a loss of frame timing synchronization. When a 4-zero pattern is detected, the DSP Mute Algorithm is triggered and if unmasked, an interrupt occurs in MISRC0[5] and NSCTR[4] is set to 1 to report that a zero nibble in ADPCM caused an interrupt. The control bit DEVMODE[2] must be set to enable the feature.

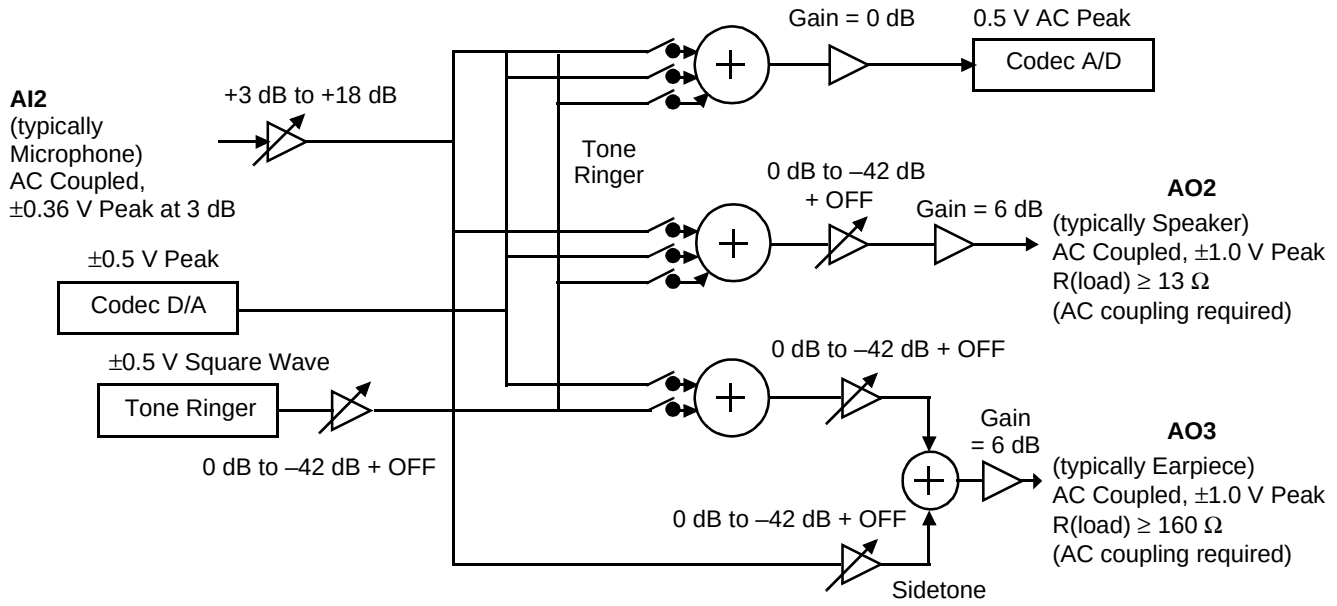
2.4 AUDIO FUNCTIONS

2.4.1 Audio Multiplexer

Figure 2-22 shows the audio multiplexer and interface. The audio mux allows flexibility in summing and applying gains to the various analog inputs and outputs. Since all internal nodes are limited to ±0.5 V swing, gain configuration should be carefully considered. It is possible to saturate a summing point by the addition of two or more large signals, resulting in clipping distortion.

The AI2 input is typically used for microphone input or PSTN input and is enabled by programming the AI2CTR register, bit [7]. The input must be AC-coupled and is followed by a gain stage that is programmable up to 18 dB in the AI2CTR register. The maximum internal signal level of the AI2 gain stage output is ±0.5 V; therefore, the maximum AI2 input level is 0.36 V at 3 dB gain.

Figure 2-22 Audio Multiplexer



Tone ringer and codec D/A inputs to the audio mux are internal signals that can be summed into any of the audio mux outputs.

The AO2 output drives an AC-coupled load of 13 Ω or greater to ±1.0 V and is intended for ringer applications. Capacitance from pin to ground should not exceed 100 pF. AO2 is enabled by setting AO2MUX[7] and is connected to the tone ringer, the analog inputs, or the codec D/A by programming AO2MUX[3:0]. The gain is programmable from 0 to –42 dB in the A23ATTN register.

AO3 is normally used for the handset earpiece driver. It drives an AC-coupled load of 160 Ω minimum to ±1.0 V. Capacitance to ground must not exceed 100 pF. AO3 is enabled by AO3MUX[7] and is connected to sidetone (AI2), tone ringer, or codec D/A in AO3MUX[4:0]. The gain is programmable from 0 to –42 dB in A23ATTN. Sidetone gain is independently controlled in the STCR register and is not affected by A23ATTN.

The codec digitizes the audio into data to be sent over the radio link. The analog input to the codec A/D is controlled by the ADMUX register. Analog data that can be summed and input to the A/D includes ringer tones, AI2, and codec D/A output. Looping the codec D/A output back into the codec A/D may be useful for system diagnostic purposes.

2.4.2 ADPCM Codec

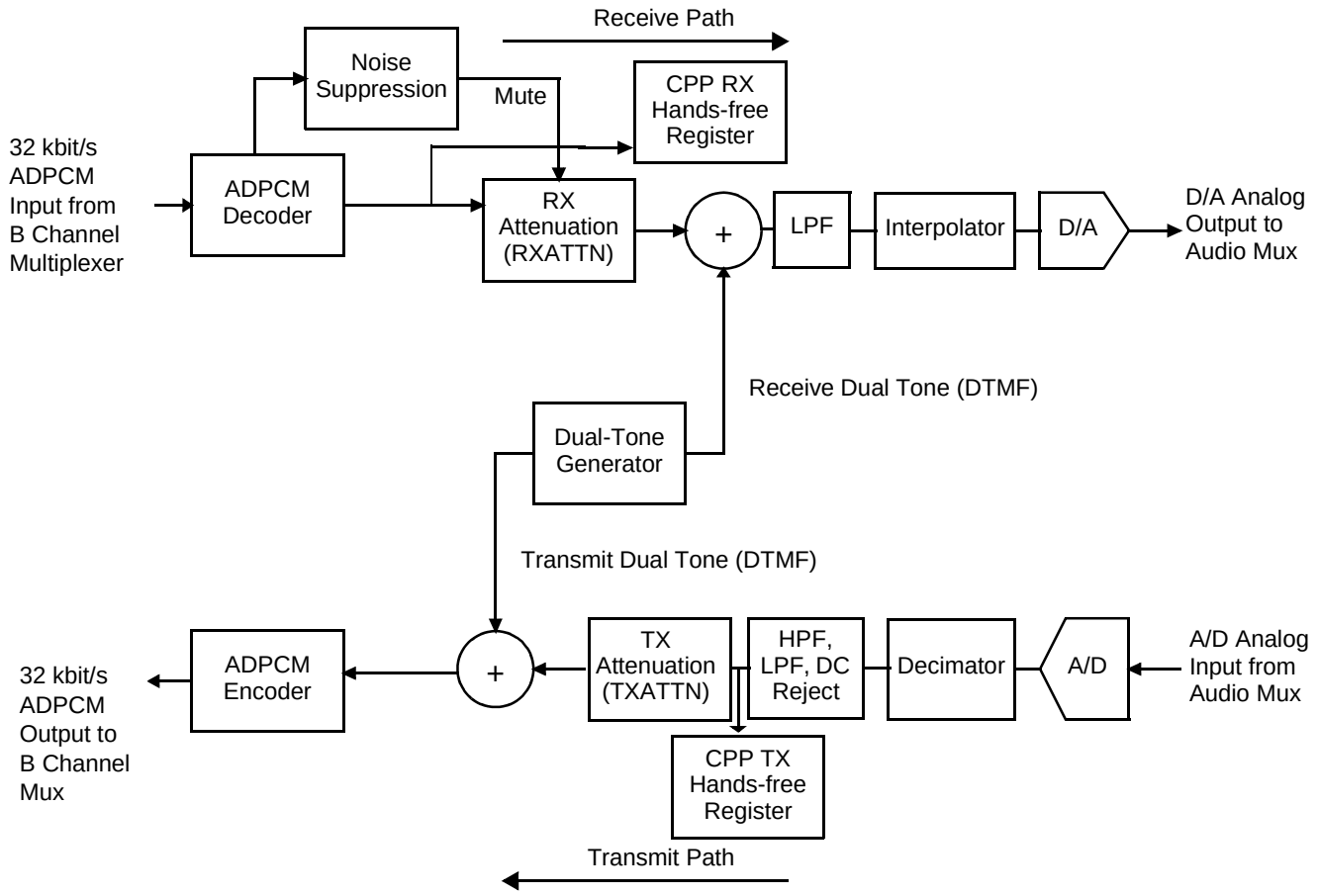
The Am79C432A codec, shown in Figure 2-23, performs 32 kbit/s ADPCM conversion in accordance with CCITT G.721. The codec is enabled by setting MECTR0[6] and is timed by an 8 kHz frame clock enabled by MECTR1[4]. The codec will not function if the frame clock is disabled. All codec and DTMF generator registers, except DSPCTR, default to unknown values and must be initialized before enabling the codec.

The transmit path is defined as the path from the A/D converter through the ADPCM encoder. Selection of input to the A/D is shown in Figure 2-22. The transmit path includes a decimator to reduce the effective sampling rate to 8 kHz and a series of filters to shape the input for minimal aliasing and rejection of DC and 50/60 Hz frequency content. The transmit attenuation TXATTN is a programmable gain. The dual-tone generator is

discussed separately in Section 2.4.3. The ADPCM encoder translates its input into a 32 kbit/s stream of ADPCM codes, which can be directed by the B Channel Multiplexer to the link or to a serial port, as described in Section 2.4.5.

The receive path begins with 32 kbit/s ADPCM data selected in the B Channel Multiplexer and ends with the D/A converter, the output of which may be connected to pins as shown in Figure 2-22. The noise suppression block applies a muting signal described in Section 2.3.4.2. The receive attenuation RXATTN is a programmable gain. The low-pass filter (LPF) and interpolator shape the signal and increase the effective sampling rate.

Figure 2-23 Codec Block Diagram for the Am79C432A



2.4.2.1 Hands-Free Support

Two peak-detect registers for the Receive and Transmit paths—RXLEVEL (FF48) and TXLEVEL (FF49)—allow the user to implement a hands-free CPP. Upon reading these registers, they reset to 0 with the exception of receiving an update while the register is being read. Under this condition, the updated data is buffered until the read goes inactive and then it is transferred to the register. Only under this condition is the new data coming in *not* compared to the data residing in the peak register. The contents of these registers are magnitude only, with the sign bit set to 0.

2.4.3 Dual-Tone Generator

The dual-tone generator is a codec feature for generating SF (single frequency), DTMF (dual-tone multi-frequency), or alert tones. It requires the codec to be enabled in MECTR0[6] and supplied with a frame clock in MECTR1[4]. Figure 2-24 is a block diagram of the dual-tone generator. The generator functions in the transmit and receive directions when the codec is in Normal mode, but only in the receive direction (i.e., output on AO2 or AO3) when the codec is programmed for DTMF-only mode in the DSPCTR register.

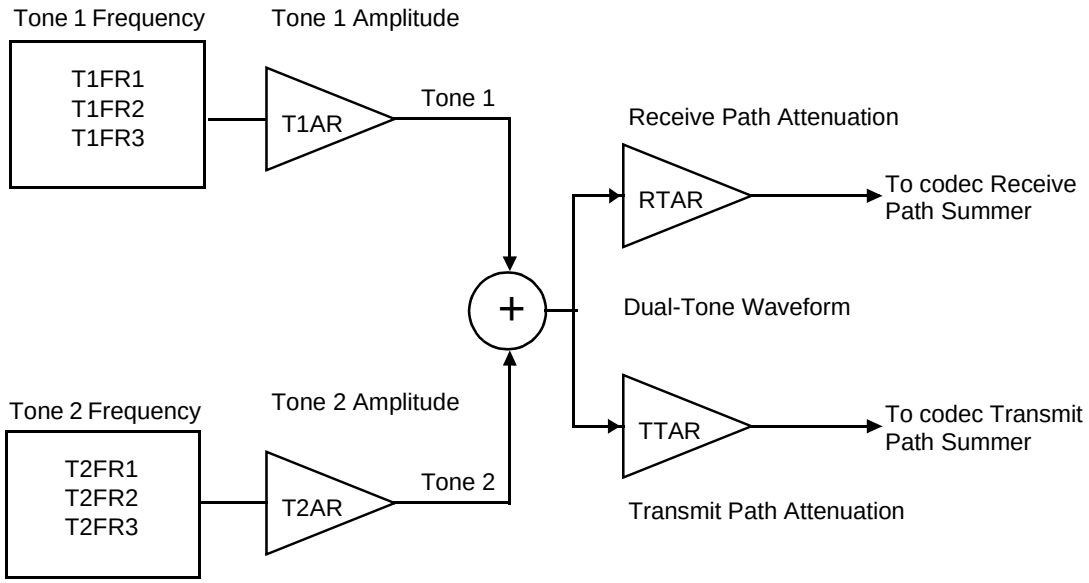
Each of the two tones has a programmable frequency and amplitude. Tone 1 frequency is programmed in T1FR1, T1FR2, and T1FR3 and its amplitude, relative to digital full scale, is programmed in T1AR. Likewise, tone 2 is defined by T2FR1, T2FR2, T2FR3, and T2AR. The two tones are summed to form the dual-tone signal. Care should be taken when programming amplitudes T1AR and T2AR to ensure that the summed signal does not overflow the digital full scale, resulting in clipping distortion. For example, if tone 1 has an amplitude of –6 dB (0.5 • full scale) and tone 2 has an amplitude of –3 dB (0.707 • full scale), the peak summed value is 1.207 • full scale, which will be clipped. Therefore, the amplitudes must be adjusted down to avoid distortion.

The tones are added to the transmit and receive paths of the codec, with independent gain adjustment in each path. Again, digital overflow should be avoided at the summing points by consideration of expected voice levels in the transmit and receive paths and the programmed transmit and receive tone levels. TTAR is the programmed loss applied to the summed dual-tone signal before it is added with the transmit audio data. RTAR is the loss applied to the summed dual-tone signal before it is added to the receive audio data.

2.4.4 Programming Notes

1. All 10 dual-tone generator registers must be initialized before the codec is enabled.
2. Writes to dual-tone generator registers are buffered such that it is possible to update all 10 locations simultaneously. Dual-tone registers loaded by software are not advanced into the digital signal processor until the RTAR address is written. Therefore, any write to any dual-tone register must be accompanied by a write to RTAR, which must occur at the end of the DTMF register write sequence.
3. In the low-power DTMF-only mode, the access speed of the codec registers is limited such that the 8032 clock speed, programmed in UCCCTR, may not exceed 2.304 MHz.

Figure 2-24 Dual-Tone Generator Block Diagram



2.4.5 B Channel Multiplexer and B Channel Port

The B channel multiplexer configures the B channel data paths, making connections between the codec, the Digital Formatter, and the 32 kbit/s serial ADPCM ports. Figure 2-25 is a block diagram of the B channel multiplexer, which is configured by programming the BDMUX register. In order to function, the B channel mux requires the 8 kHz frame clock to be enabled in MECTR1[4]. The four multifunction pins that make up the B channel port must be configured by programming BDMUX[6:5]. Figure 2-26 shows the timing of the B channel port. The 8 kHz frame clock will exhibit 108 ns jitter when the device is a timing slave to the radio link.

Figure 2-25 B Channel Multiplexer Diagram

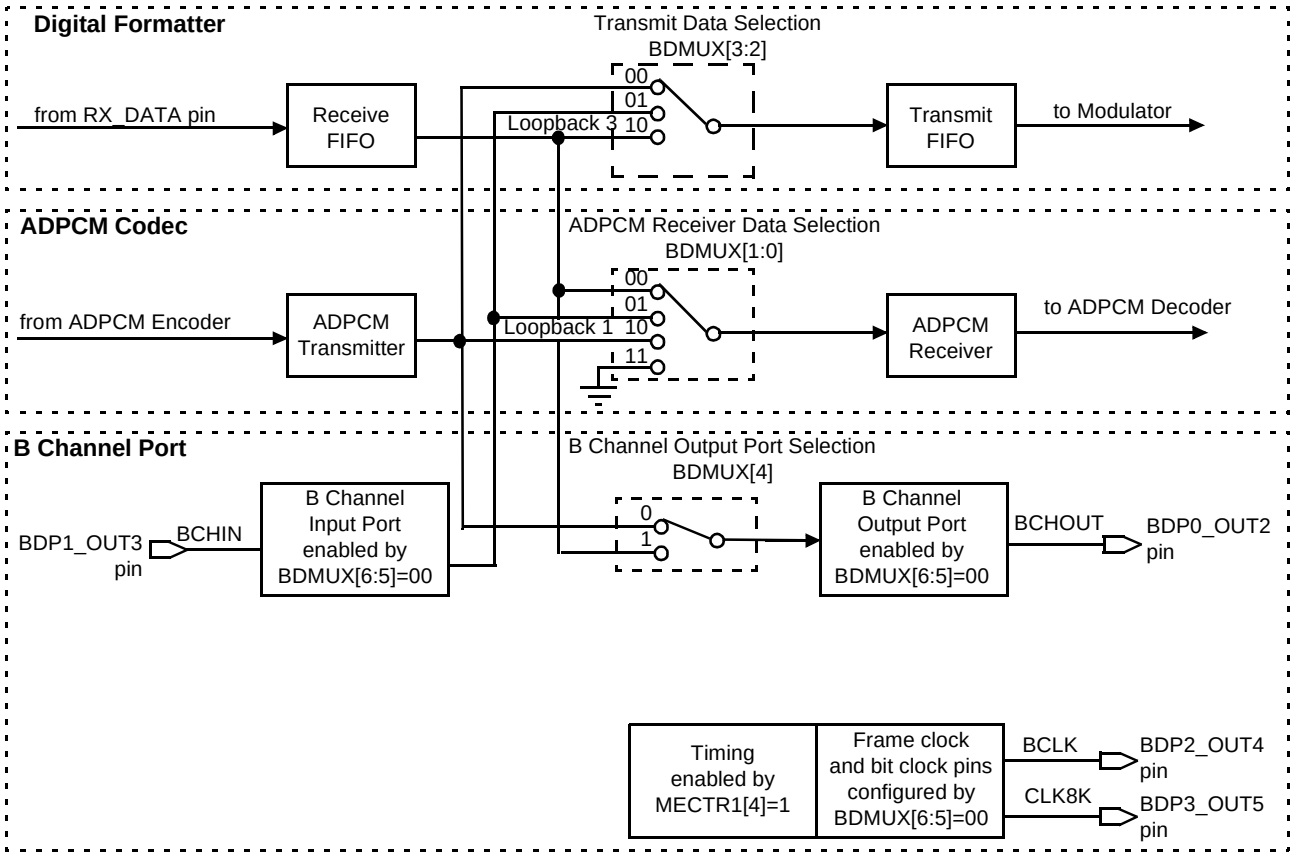
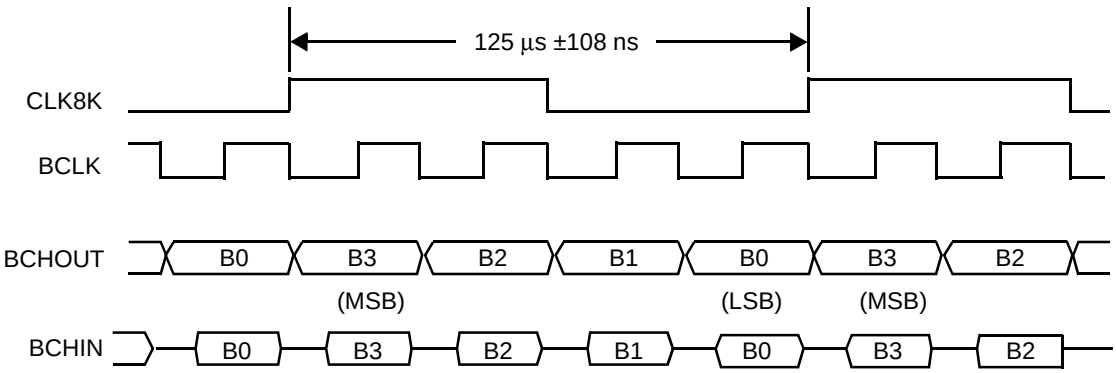


Figure 2-26 B Channel ADPCM Port Timing



2.4.6 Tone Ringer

The tone ringer generates a square wave of programmable frequency and amplitude. The ringer waveform is an input to the audio multiplexer and may appear at either of the analog outputs, AO2 or AO3, if appropriately configured. The ringer enable is MECTR0[3]. The frequency is programmed in the TRFR register, which must be initialized to a valid value before the ringer is enabled. The ringer smoothly switches from one programmed frequency to a newly programmed value with no irregular pulses.

The amplitude of the ringer waveform is programmed in the TRAMP register. Since an irregular pulse may occur when disabling the ringer, it is recommended that TRAMP be programmed for zero amplitude before clearing MECTR0[3].

2.4.7 Biasing

The biases of the various analog blocks are determined by an internal bandgap reference. IREF is the current reference that must be tied to analog ground through a 61.9 kΩ, 1% resistor. The IREF pin is high impedance when the device is in Shutdown mode. Because of its high input impedance, the IREF pin may be susceptible to noise. Therefore, external components connected to the pin should be located as close as possible to the IC and away from noisy signal traces.

The CFILT pin filters the internal analog reference voltage. Two capacitors, 10 µF low-frequency capacitor (e.g., electrolytic) in parallel with 1 µF high-frequency capacitor (e.g., ceramic), must be tied from the CFILT pin to analog ground. The bias network performs a 108 ms rapid charge acquisition procedure after reset to bring analog circuits to their approximate DC bias point, after which the CFILT pin provides 5 Hz, single-pole, low-pass filter for AC rejection, which is not affected by the Shutdown mode.

The internal references are automatically powered down when the device is in shutdown. Upon exit from shutdown, approximately 300 µs of stabilization time is required.

MECTR0[5] is a control bit that disables the internal analog references for all analog circuits, including the audio I/O, RSSI, Formatter Baseband output (TXI and TXQ), and the battery detector. The bit must be cleared in order to use any analog function. Setting MECTR0[5] powers down the internal references for minimal power consumption in Shutdown mode or when no analog circuits are necessary. Upon exit from the disabled state, references require approximately 300 µs to stabilize.

2.5 DEVELOPMENT SUPPORT

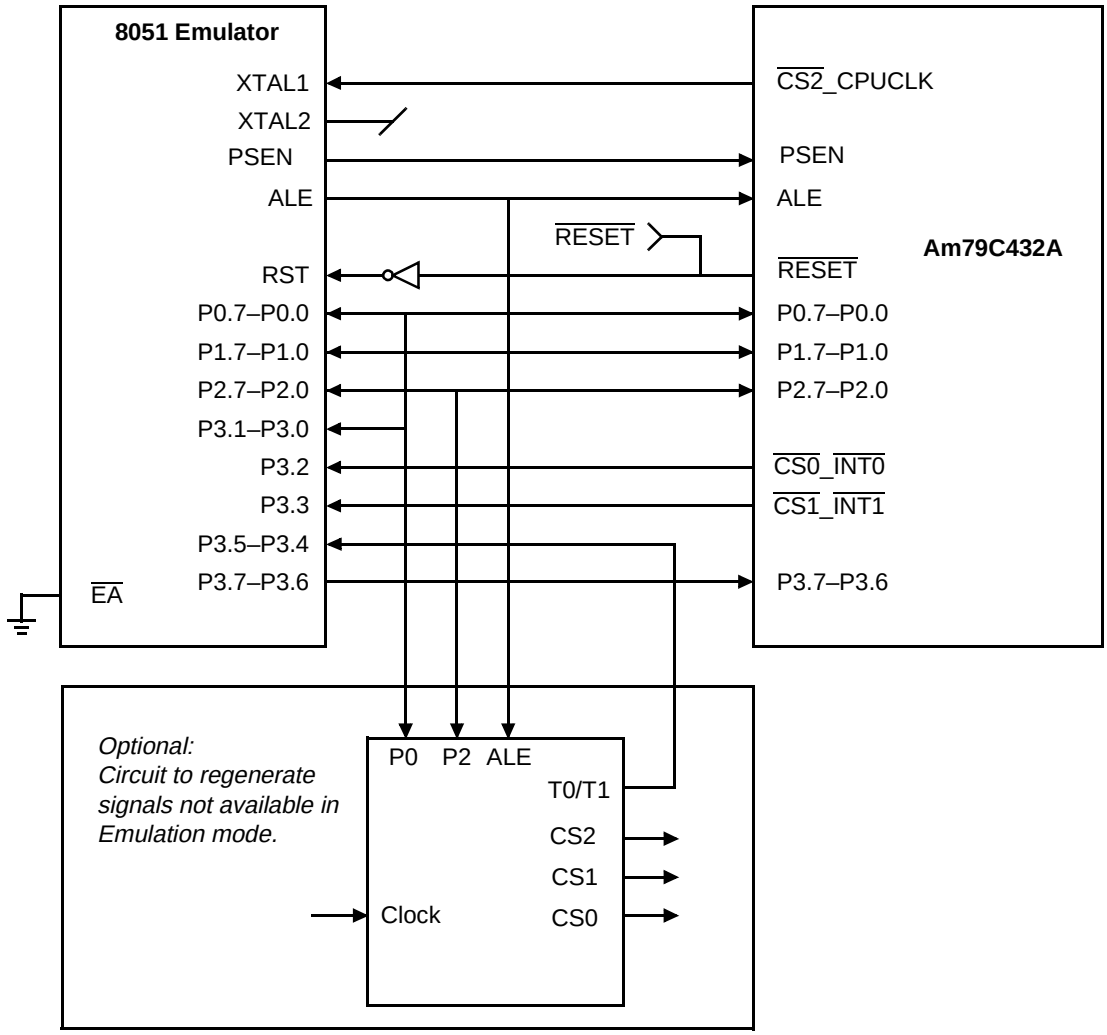
2.5.1 Emulation Mode

Emulation mode is for code development using an 8051-family emulator, and is entered by driving the TRI1 pin to ground while reset is active. Emulators provide the debug advantages of instruction stepping, breakpoints, visibility of internal microcontroller registers, and a convenient program download procedure. In Emulation mode, an external processor with 8051 bus timing, shown in Figure 2-27, drives the P0, P1, P2, P3, $\overline{\text{PSEN}}$, and ALE inputs of the PhoX IC, replacing the on-chip 8032.

The PhoX chip in Emulation mode behaves as in Normal mode, except as follows:

1. All of the on-chip 8032 ports go to the high impedance state, including $\overline{\text{PSEN}}$, ALE, P0, P1, P2, and P3 buffers.
2. The $\overline{\text{CS0}}$_$\overline{\text{INT0}}$ pin takes the $\overline{\text{INT0}}$ output function, which may be used to drive the $\overline{\text{INT0}}$ (P3.2) input of the emulator. The $\overline{\text{CS0}}$ function is not available.
3. The $\overline{\text{CS1}}$_$\overline{\text{INT}}$1 pin takes the $\overline{\text{INT1}}$ output function, which may be used to drive the $\overline{\text{INT1}}$ (P3.3) input of the emulator. The $\overline{\text{CS1}}$ function is not available.
4. The $\overline{\text{CS2}}$_CPUCLK pin takes the CPUCLK output function, which may be used to drive the clock input of the emulator. The $\overline{\text{CS2}}$ function is not available.
5. The watchdog timer is disabled and does not generate periodic resets.
6. The T0 and T1 (P3.4, P3.5) 18 kHz clock inputs are not available to the emulator.
7. The 256 byte RAM in 8032 internal data space is not available for use by the emulator.

Figure 2-27 Driving the Am79C432A with an 8051-Family In-Circuit Emulator



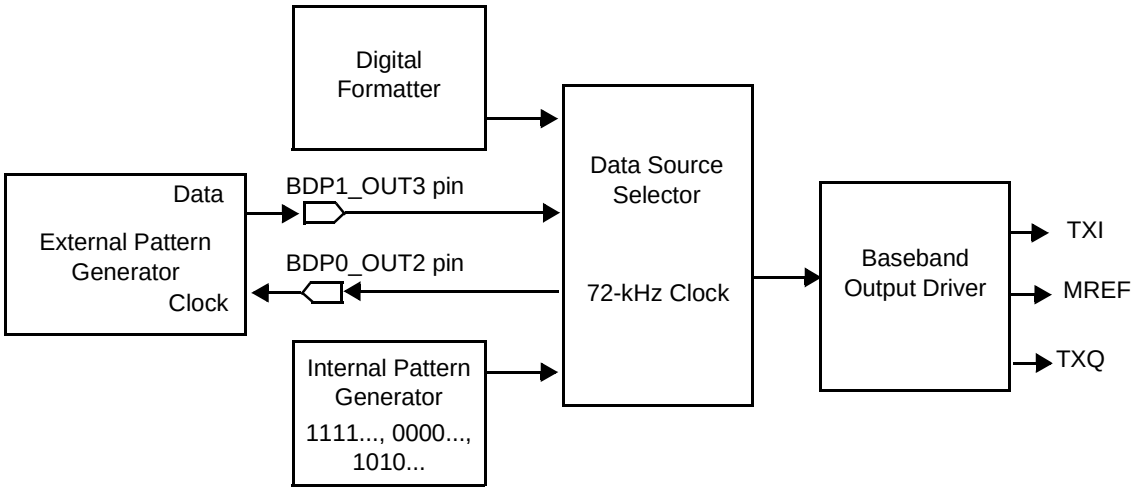
2.5.2 System Test Facilities

The PhoX IC provides test ports for the Digital Formatter and the modulator (transmit baseband driver) to ease system debug.

2.5.2.1 Modulator Test Mode

The Modulator Test mode allows RF development to proceed without functional system software by driving the modulator with either fixed patterns or externally generated arbitrary data. It operates with either I-Q or NRZ output data type and requires MECTR1[5] to be set. Figure 2-28 demonstrates the data sources for the modulator. The MODTST register bit [2] configures the modulator for the Test mode. MODTST[1:0] defines the data pattern to be modulated. The modulator provides three internally generated fixed patterns: all zeroes (i.e., $\omega_m(t) = -2\pi \bullet 18$ kHz), all ones (i.e., $+ 2\pi \bullet 18$ kHz), and alternating ones and zeroes ($\omega_m(t)$ varies over $\pm 2\pi \bullet 18$ kHz). In the externally generated Test Pattern mode, any arbitrary data pattern can be injected at the BDP1_OUT3 multifunction pin, with data transitions timed by the rising edges of the 72 kHz clock output at the BDP0_OUT2 pin. In Test mode, the modulator does not perform ramp-up or ramp-down sequences. In order to correctly configure the multifunction pin, BDMUX[6:5] must be programmed to 11 and MODTST[2] must be High.

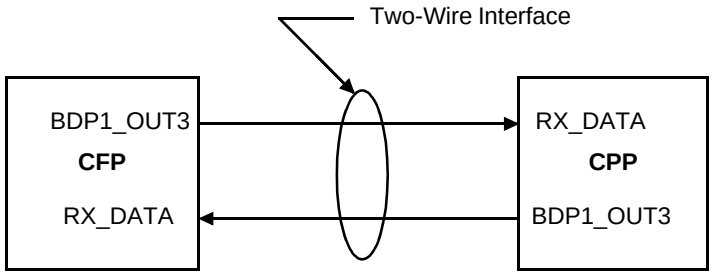
Figure 2-28 Data Source Selection for Modulator Test Mode



2.5.2.2 Transmitter Digital Output

The Digital Formatter transmit data output appears in true digital form at the BDP1_OUT3 pin when the BDMUX[6:5]=11 and MODTST[2]=0. Data changes on the rising edge of a 72 kHz clock that appears on the BDP0_OUT2 pin. The transmit data strobe, BDTXEN, appears on and is High during valid transmit data. The digital transmit data of one chip may be directly connected to the receive data of another, as shown in Figure 2-29, to eliminate the radio link during software development. The TXI pin, emitting transmit data in NRZ format, can be used rather than BDP1_OUT3 if the 1 Vpp pseudo-digital TXI output is externally modified to meet digital electrical specifications for V_{IH} and V_{IL}.

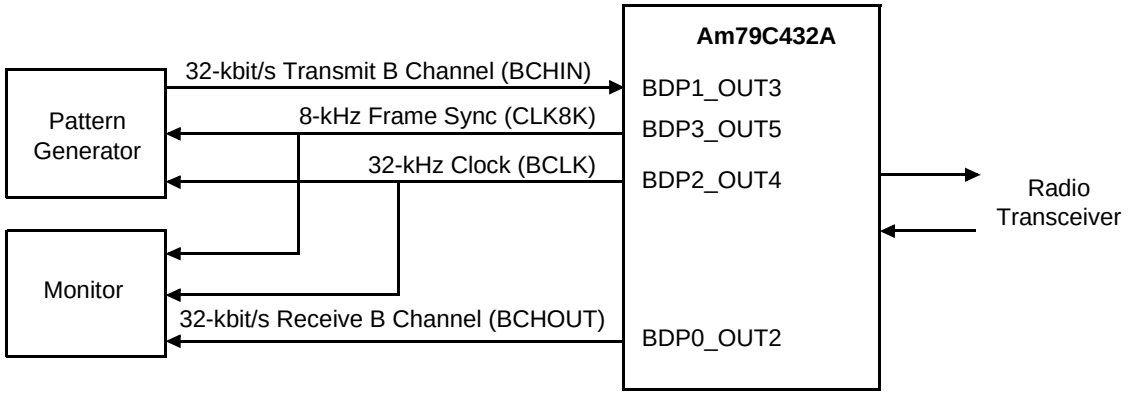
Figure 2-29 Eliminating the RF Front-End During Software Development



2.5.2.3 B Channel Injection/Monitoring

The B channel port and the B channel multiplexer are useful tools for validating B channel continuity and bit error rate. Connections are shown in Figure 2-30. The BDMUX register controls B channel routing. Multifunction pins are configured for B channel ports by programming BDMUX[6:5]=00. 8 kHz frame boundaries are determined by the CLK8K output on the BDP3_OUT5 pin and 32 kHz bit timing is the BCLK output on the BDP2_OUT5 pin. Data may be injected into the B channel by driving the BDP1_OUT3 pin. Input B channel data on BDP1_OUT3 is clocked into the PhoX device on rising edges of BCLK. B channel output received from the radio link is available in the BCHOUT signal on the BDP0_OUT2 pin.

Figure 2-30 B Channel Injection and Monitoring



2.5.2.4 D Channel and SYN Channel Injection/Monitoring

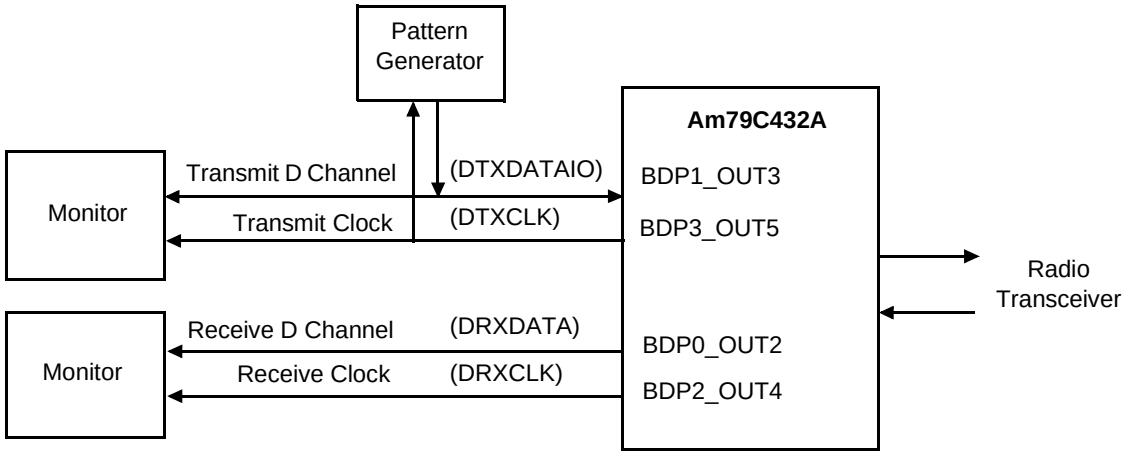
Normally, D channel transmit data is driven by the microcontroller through the transmit buffer. D channel injection, shown in Figure 2-31, allows an external circuit to drive the transmit D channel serially. The B/D channel multiplexer pins must be configured for the D channel function by programming BDMUX[6:5] to 10 and the DMONIT register, bit 1, must be programmed High to select injection. Input is sampled on rising edges of the transmit clock pulses, which appear on BDP3_OUT5. The correct number of clock pulses for a given multiplex occur during the D channel time slots. For example, in MUX1.4, two groups of two clock pulses occur per frame, corresponding to the beginning and the end of the transmit frame. Data is presented in the D channel in the order in which it is received. The external circuit is responsible for generating the IDLE_D and SYNCD patterns as necessary.

Setting DMONIT[0] enables SYN channel injection or monitoring. In this case, external circuitry is responsible for driving all data except for preambles, including CHM and SYNC patterns and the B channel. The clock output on BDP3_OUT5 drives pulses during each D, B, CHM or SYNC time slot, but not during preamble time slots.

Clearing DMONIT[1] puts the D channel port in Output (listen only) mode. In this case, transmit D channel activity, controlled by the microcontroller, may be monitored by an external circuit. The BDP1_OUT3 pin follows the D channel transmit data, and BDP3_OUT5 provides clocks. Data transitions are on falling clock edges. If DMONIT[0] is set, the output includes D and B channels and CHM and SYNC patterns.

The receiver has a listen-only output on the BDP0_OUT2 pin, driving either D channel data only (DMONIT[0] = 0 or D and B channels and SYNC and CHM patterns (DMONIT[0] = 1). The associated DRXCLK clock pulses are outputs of the BDP2_OUT4 pin. Data changes on falling clock edges.

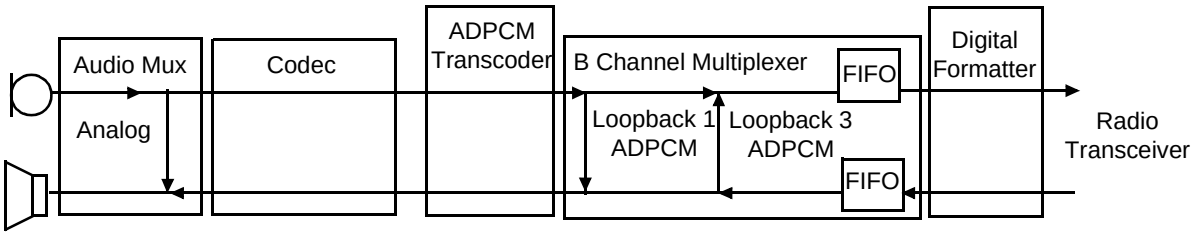
Figure 2-31 D/SYN Channel Injection and Monitoring



2.5.3 B Channel Loopbacks

Figure 2-32 shows the various B (voice) channel loopbacks in the Am79C432A chip. These loopbacks can be used to measure analog performance and isolate distortion sources. Loopback 3 allows a PhoX device to behave as a reference CFP for the handset round-trip delay measurement. When used as a reference CFP, the effective loopback delay is approximately 1.62 ms.

Figure 2-32 B Channel Loopbacks



CHAPTER

3 REGISTER SUMMARY

3.1 MEMORY MAP AND INDEX

The user registers and RAM reside in the 64 Kbyte external data space of the 8032, as shown in Table 3-1. The controller also has an internal data space that includes 256 bytes of RAM and special function registers, which are described in the *80C32T2 Appendices, PhoX™ Controller for Digital Cordless Telephones*. In Table 3-1, the following conventions apply:

* = register described out of numerical sequence in Table 3-1

x = default value of bit is unknown

x, 0, 1 = reserved or unused bit

N/A = not applicable

Table 3-1 External Data Space Address Map

Data Space	Register Mnemonic	Address	Access	Default	Description	Page
Data RAM		0000–03FF	R/W	xxxx xxxx	On-chip RAM, ADRDEC[7]=0	2-8
$\overline{CS1}$		0000–03FF	R/W	xxxx xxxx	Ext I/O, ADRDEC[7]=1, not Emulation mode	2-8
$\overline{CS1}$		0400–EFFF	R/W		Ext I/O, not Emulation mode	2-8
$\overline{CS0}$		F000–F3FF	R/W		Ext I/O, not Emulation mode	2-8
$\overline{CS2}$		F400–F7FF	R/W		Ext I/O, not Emulation mode	2-8
Address Decoder	Reserved	FF00–FF0E	—	—	—	—
	ADRDEC	FF0F	R/W	0x00 0001	Address decoder control/init and status	3-4
	Unused	FF10–FF1F	—	—	—	—
Parallel Port	P1SRC0	FF20	R	0000 0000	P1 interrupt source 0	3-5
	P1SRC1	FF21	R	0000 0000	P1 interrupt source 1	3-5
	P1SRC2	FF22	R	0000 0000	P1 interrupt source 2	3-6
	P1MASK	FF23	R/W	0000 0000	P1 interrupt mask	3-6
	P1TRIG	FF24	R/W	0000 0000	P1 int trigger control	3-7
	GPOCTR0	FF25	R/W	1111 11xx	Gen purpose output control 0	3-7
	GPOCTR1	FF26	R/W	0000 0100	Gen purpose output control 1	3-8
	XISTAT0	FF27	R	0xxx x00x	Ext interrupt 0 status	3-9
	XISTAT1	FF28	R	0000 000x	Ext interrupt 1 status	3-10
	XISTAT2	FF29	R	0000 000x	Ext interrupt 2 status	3-10
	Reserved	FF2A–FF2B	—	xxxx xxxx	—	—
Key Scanner	KPSTAT	FF2C	R	0000 0000	Keypad status	3-11
	Reserved	FF2D	—	xxxx xxxx	—	—
	*	FF2E	—	—	(see Noise Suppression)	—
B/D Mux	BDMUX	FF2F	R/W	0000 0000	B/D channel routing mux	3-12

Data Space	Register Mnemonic	Address	Access	Default	Description	Page
Serial Port	SIOMODE	FF30	R/W	xxx0 0000	Serial port mode	3-13
	SIOTB	FF31	W	N/A	Serial port transmit buffer	3-13
	SIORB	FF32	R	xxxx xxxx	Serial port receive buffer	3-14
	SIOTBL	FF33	R/W	xxxx x000	Serial port transmit length	3-15
	Reserved	FF34–FF36	—	xxxx xxxx	—	—
	SIOSTAT	FF37	R	0000 0010	Serial port status	3-15
	SIOMASK	FF38	R/W	0000 0000	Serial port interrupt mask	3-16
	SIOSRC	FF39	R	0000 0000	Serial port interrupt source	3-16
	Reserved	FF3A–FF3F	—	xxxx xxxx	—	—
	SPTMG	FFED	R/W	xxxx xx00	Serial port timing control	3-17
Audio Mux	Reserved	—	—	—	—	—
	AO2MUX	FF41	R/W	0xxx 0000	AO2 mux control	3-18
	AO3MUX	FF42	R/W	0xx0 0000	AO3 mux control	3-19
	ADMUX	FF43	R/W	xxxx 0000	A/D mux control	3-20
	AI2CTR	FF44	R/W	0xx0 0000	AI2 control	3-21
	STCR	FF45	R/W	xxx0 0000	Sidetone, Control	3-22
	*	FF46	—	—	(See Tone Ringer)	—
	A23ATTN	FF47	R/W	0000 0000	AO2, AO3 attenuation	3-23
Hands-Free Operations	RXLEVEL	FF48	R	0000 0000	Receive signal level	3-24
	TXLEVEL	FF49	R	0000 0000	Transmit signal level	3-24
	Reserved	FF4A	—	xxxx xxxx	—	—
Tone Ringer	TRAMP	FF46	R/W	xxxx 0000	Tone ringer amplitude	3-25
	TRFR	FF4B	R/W	xxxx xxxx	Tone ringer frequency	3-25
	*	FF4C	—	—	(See RSSI)	—
Modulator	MODTST	FF4D	R/W	xxx0 x000	Modulator test mode	3-28
Battery Detect	BATLEV	FF4E	R/W	00xx 0000	Battery-level register	3-29
RSSI	RSSICFG	FF4C	R/W	xxxx x000	RSSI configuration	3-30
	RSSISTAT	FF4F	R/W	0x0x xxxx	RSSI status	3-31
Dual-Tone Generator	T1FR1	FF50	R/W	xxxx xxxx	Tone 1 frequency	3-33
	T1FR2	FF51	R/W	xxxx xxxx	Tone 1 frequency	3-33
	T1FR3	FF52	R/W	xxxx xxxx	Tone 1 frequency	3-33
	T1AR	FF53	R/W	xxxx xxxx	Tone 1 amplitude	3-34
	TTAR	FF54	R/W	xxxx xxxx	Transmit tone attenuation	3-36
	T2FR1	FF55	R/W	xxxx xxxx	Tone 2 frequency	3-33
	T2FR2	FF56	R/W	xxxx xxxx	Tone 2 frequency	3-33
	T2FR3	FF57	R/W	xxxx xxxx	Tone 2 frequency	3-33
	T2AR	FF58	R/W	xxxx xxxx	Tone 2 amplitude	3-34
	RTAR	FF59	R/W	xxxx xxxx	Receive tone attenuation	3-36
Codec	TXATTN	FF5A	R/W	xxxx xxxx	Transmit attenuation	3-36
	RXATTN	FF5B	R/W	xxxx xxxx	Receive attenuation	3-36
	DSPCTR	FF5C	R/W	0000 0000	Codec mode control	3-37

Data Space	Register Mnemonic	Address	Access	Default	Description	Page
Noise Suppression	NSCTR	FF2E	R/W	0000 0000	Noise suppression control	3-38
	NSTHR	FF5D	R/W	xxxx xxxx	Noise suppression threshold	3-39
	MUTE	FF5E	R/W	xxxx xxxx	Noise suppress mute length	3-39
	Reserved	FF5F–FFBF	—	xxxx xxxx	—	—
	JITCTR	FFC7	R/W	0000 0000	Jitter detection control	3-40
Digital Formatter	RXBUF0–5	FFC0–FFC5	R	xxxx xxxx	Receive buffers 0–5	3-41
	TXBUF0–5	FFC0–FFC5	W	xxxx xxxx	Transmit buffers 0–5	3-41
	DEVMODE	FFC6	R/W	000x 0xxx	Device mode: CFP/CPP	3-42
	*	FFC7	R/W	—	(See Noise Suppression)	—
	RXTMGR	FFC8	R/W	000x 0000	Receive timing recovery	3-43
	TXMUX	FFC9	R/W	xxxx x011	Transmit frame control	3-44
	RXMUX	FFCA	R/W	xxxx 0011	Receive frame control	3-45
	TXDISAB	FFCB	W	xxxx xx01	Transmit disable	3-46
	SYNCDC	FFCC	R/W	xxxx xxx0	SYNCD control	3-46
	RDATAC	FFCD	W	N/A	Receive data control	3-47
	TPOWER	FFCE	R/W	00xx xxx0	Transmit power level control	3-47
	BVALID	FFCF	R/W	0xxx xxxx	Enable B channel	3-48
	SYNCTR	FFD0	W	N/A	Frame sync control	3-48
	DMONIT	FFD1	R/W	xxxx xx00	D channel monitor control	3-49
	DTXCTR	FFD2	R/W	xxxx xx00	Transmit control	3-50
	Reserved	FFD3	—	—	—	—
	TDELAY	FFD4	R/W	1000 1011	Transmit delay control	3-51
	RDELAY	FFD5	R/W	0000 1011	Receive delay control	3-52
	Reserved	FFD6–FFD7	—	xxxx xxxx	—	—
	RFINV	FFD8	R/W	xxxx 0000	RF polarity control	3-53
	RXFALL	FFD9	R/W	0000 0000	RX timing in CFP mode	3-54
	PLLCTRL	FFDA	R/W	0000 0000	Phase-locked loop control	3-55
	Reserved	FFDB–FFDC	—	xxxx xxxx	—	—
	MODTMG	FFDD	R/W	xxxx xx00	Modem timing adjustment	3-56
	MODDLY	FFDE	R/W	x000 0000	Modem delay register	3-57
	Reserved	FFDF	—	xxxx xxxx	—	—
	DCHSTAT	FFE4	R	0000 0100	D channel interrupt status	3-58
	CMSSRC	FFE5	R	0000 0000	CHM/SYNC interrupt source	3-60
	CMSMASK	FFE6	R/W	xxxx 0000	CHM/SYNC interrupt mask	3-61
Interrupt Controller	MISRC0	FFE0	R	0000 0000	Main interrupt source 0	3-62
	MISRC1	FFE1	R	0000 0000	Main interrupt source 1	3-63
	MIMSK0	FFE2	R/W	x000 0000	Main interrupt mask 0	3-65
	MIMSK1	FFE3	R/W	0000 0000	Main interrupt mask 1	3-65
	*	FFE4–FFE6	—	—	(See Digital Formatter)	—
	Reserved	FFE7–FFE8	R/W	xxxx xxxx	—	—
Clock Generator	UCCCTR	FFE9	R/W	000x 0000	Shutdown/µc clock control	3-66
	UCCCP	FFEA	W	N/A	Shutdown/µc clock control protect	3-67
	MECTR0	FFEB	R/W	0000 0x00	Module enable control 0	3-68
	MECTR1	FFEC	R/W	xx00 00x0	Module enable control 1	3-69
	*	FFED	—	—	(see Serial Port)	—
	Reserved	FFEE	—	xxxx xxxx	—	—
Watchdog Timer	WDTKEY	FFEF	W	N/A	WDT key register	
	Reserved	FFF0–FFFF	—	—	—	—

3.2 RESERVED REGISTER BITS

Many of the registers contain data fields that are reserved by AMD for feature enhancement in future silicon revisions, so writes to reserved data fields must be zeroes.

Except where noted, reads of reserved data fields return unknown values.

Read-modify-write operations may, in general, write back to the reserved field the value read. Exceptions are noted in the individual register descriptions.

3.3 ADDRESS DECODER

3.3.1 ADRDEC

Full name: Address Decoder Control/Initialization and Status

Address: FF0F

Default: 0x00 0001

Access: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data RAM Disable	Reserved			Quiet Mode	Reserved	$\overline{CS2}$_DISABLE	Reserved 1

Bit 7 Data RAM Disable

- 0: Enable on-chip 1024 byte RAM in address space 0000–03FF. The $\overline{CS1}$ output on the $\overline{CS1}$_$\overline{INT1}$ pin decodes address range 0400–EFFF.
- 1: Disable on-chip 1024 byte RAM. The $\overline{CS1}$_$\overline{INT1}$ output decodes address range 0000–EFFF.

Bits 6–4, 2 Reserved

Bit 3 Quiet Mode Enable (Noise reduction feature when operating from on-chip memory). User must program this bit Low before external memory can be accessed. Quiet mode is disabled (forced to 0) if the PhoX device is configured by the TRI1 pin during RESET to access external ROM.

- 0: Microcontroller I/O operates normally, even while accessing internal memory.
- 1: Disables the I/O for accessing external memory. The P0, P2, and P3.6 (WRn) and P3.7 (RDn) are held High and ALE is held Low.

Bit 1 $\overline{CS2}$_DISABLE

This bit controls the function of the $\overline{CS2}$_CPUCLK pin, depending on the device mode, according to Table 3-2.

Table 3-2 $\overline{CS2}$_CPUCLK Pin Function

$\overline{CS2}$_CPUCLK SELECT	Emulation Mode	$\overline{CS2}$_CPUCLK Pin Function	Description
0	No	$\overline{CS2}$	Address decode output (F400–F7FF)
0	Yes	CPUCLK	8032 clock output
1	X	CPUCLK	8032 clock output

Bit 0 Reserved Bit

Must be written to 1.

3.4 PARALLEL PORT

3.4.1 P1SRC0

Full name: P1 Interrupt Source Register 0

Address: FF20

Default: 0000 0000

Access: Read Only

P1SRC0 latches occurrences of unmasked transitions on port pins P1.0 and P1.1 and generates the P1 INT 0 interrupt reported in MISRC1[4]. Each bit is:

- Set by a P1 transition if the associated bit in P1MASK is set. The polarity of the transition is defined by the P1TRIG register.
- Cleared by reading P1SRC0 or by applying reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						P1.1 INTRUPT FLAG	P1.0 INTRUPT FLAG

Bits 7–2 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1 P1.1 Interrupt Flag

Bit 0 P1.0 Interrupt Flag

3.4.2 P1SRC1

Full name: P1 Interrupt Source Register 1

Address: FF21

Default: 0000 0000

Access: Read Only

P1SRC1 latches occurrences of unmasked transitions on port pins P1.2 and P1.3 and generates the P1 INT 1 interrupt reported in MISRC1[5]. Each bit is:

- Set by a P1 transition if the associated bit in P1MASK is set. The polarity of the transition is defined by the P1TRIG register.
- Cleared by reading P1SRC1 or by applying reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						P1.3 INTRUPT FLAG	P1.2 INTRUPT FLAG

Bits 7–2 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1 P1.3 Interrupt Flag

Bit 0 P1.2 Interrupt Flag

3.4.3 P1SRC2

Full name: P1 Interrupt Source Register 2

Address: FF22

Default: 0000 0000

Access: Read Only

P1SRC2 latches occurrences of unmasked transitions on port pins P1.7–P1.4 and generates the P1 INT 2 interrupt reported in MISRC1[6]. Each bit is:

- Set by a P1 transition if the associated bit in P1MASK is set. The polarity of the transition is defined by the P1TRIG register.
- Cleared by reading P1SRC2 or by applying reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				P1.7 INTRUPT FLAG	P1.6 INTRUPT FLAG	P1.5 INTRUPT FLAG	P1.4 INTRUPT FLAG

Bits 7–4 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 3 P1.7 Interrupt Flag

Bit 2 P1.6 Interrupt Flag

Bit 1 P1.5 Interrupt Flag

Bit 0 P1.4 Interrupt Flag

3.4.4 P1MASK

Full name: P1 Interrupt Mask Register

Address: FF23

Default: 0000 0000

Access: Read/Write

P1MASK individually masks transitions on P1 bits affecting P1SRC2–P1SRC0. For all bits:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1.7 INTRUPT MASK	P1.6 INTRUPT MASK	P1.5 INTRUPT MASK	P1.4 INTRUPT MASK	P1.3 INTRUPT MASK	P1.2 INTRUPT MASK	P1.1 INTRUPT MASK	P1.0 INTRUPT MASK

0: Disable interrupt source and clear corresponding source bit
1: Enable corresponding interrupt source

3.4.5 P1TRIG

Full name: P1 Interrupt Trigger Register

Address: FF24

Default: 0000 0000

Access: Read/Write

P1TRIG defines the polarity of transitions on individual P1 bits, causing interrupts to be latched in the P1SRC2–P1SRC0 registers.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1.7 TRIG SELECT	P1.6 TRIG SELECT	P1.5 TRIG SELECT	P1.4 TRIG SELECT	P1.3 TRIG SELECT	P1.2 TRIG SELECT	P1.1 TRIG SELECT	P1.0 TRIG SELECT

Bits 7–0 P1 Trigger Select

0: High-to-Low transitions cause interrupts
1: Low-to-High transitions cause interrupts

3.4.6 GPOCTR0

Full name: General Purpose Output Control Register 0

Address: FF25

Default: 1111 11xx

Access: Read/Write

GPOCTR0 controls the general-purpose outputs OUT2–OUT7, which are outputs on multifunction pins configured by the BDMUX register, bits [6:5], and by GPOCTR1[6:5]. Values written to GPOCTR0 are internally latched regardless of whether a pin is configured for OUT operation and are driven on the pin only when the pin is appropriately configured.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	Reserved	

Bit 7 OUT7

Enabled on the COL6_OUT7 pin if GPOCTR1[6,4]=1,0

0: OUT7 drives Low
1: OUT7 drives High

Bit 6 OUT6

Enabled on the COL5_OUT6 pin if GPOCTR1[5]=1

0: OUT6 drives Low
1: OUT6 drives High

Bit 5 OUT 5

Enabled on the BDP3_OUT5 pin if BDMUX[6:5]=01

0: OUT5 drives Low
1: OUT5 drives High

Bit 4 OUT 4

Enabled on the BDP2_OUT4 pin if BDMUX[6:5]=01

0: OUT4 drives Low

1: OUT4 drives High

Bit 3 OUT 3

Enabled on the BDP1_OUT3 pin if BDMUX[6:5]=01

0: OUT3 drives Low
1: OUT3 drives High

Bit 2 OUT 2

Enabled on the BDP0_OUT2 pin if BDMUX[6:5]=01

0: OUT2 drives Low
1: OUT2 drives High

Bits 1–0 Reserved

3.4.7 GPOCTR1

Full name: General Purpose Output Control Register 1

Address: FF26

Default: 0000 0100

Access: Read/Write

GPOCTR1 controls the general-purpose output OUT10, which is output on multifunction pins configured by the BDMUX register, bit 7, and by GPOCTR1[7]. Values written to GPOCTR1[3:0] are latched regardless of whether a pin is configured for OUT operation or not.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRI0_ OUT10 SELECT	COL6_ OUT7 SELECT	COL5_ OUT6 SELECT	OSCEN SELECT	Reserved	OUT10	Reserved	Reserved

Bit 7 TRI0_OUT10 Select

0: TRI0 input (tri-level input 0)
1: OUT10 output

Bit 6 COL6_OUT7 Select

0: Keypad COL6 input
1: OUT7 output

Bit 5 COL5_OUT6 Select

0: Keypad COL5 input
1: OUT6 output

Bit 4 OSCEN SELECT

0: Disables the OSCEN output function
1: Configures COL6_OUT7 pin to drive the OSCEN (oscillator enable, active High) signal which represents the Shutdown state of the PhoX device. Applies only if GPOCTR1[5] is set.

Bit 3 Reserved

Bit 2 OUT10

Enabled on the TRI0_OUT10 pin when GPOCTR1[7] is High
0: OUT10 drives Low
1: OUT10 drives High

Bit 1 Reserved

Bit 0 Reserved

3.4.8 XISTAT0

Full name: TRI0, TRI1, and External Interrupt 0 Status Register

Address: FF27

Default: 0xxx x00x

Access: Read Only

XISTAT0 reports the current logic levels of TRI0, TRI1, and XINT0 pins.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TRI1		TRI0		Reserved		XINT0

Bit 7 Reserved. The current silicon revision returns zeroes, subject to change in future revisions.

Bits 6–5 TRI1 Pin Level

00: Open or mid-supply (Basic mode = Internal ROM mode)
01: Low (Basic mode = Emulation mode)
10: High (Basic mode = External ROM mode)
11: Reserved, not used

Bits 4–3 TRI0 Pin Level

00: Open or mid-supply
01: Low
10: High
11: Reserved, not used

Bits 2–1 Reserved. The current silicon revision returns zeroes, subject to change in future revisions.

Bit 0 XINT0 Pin Level

0: XINT0 pin is Low
1: XINT0 pin is High

3.4.9 XISTAT1

Full name: External Interrupt 1 Status Register

Address: FF28

Default: 0000 000x

Access: Read Only

XISTAT1 reports the current logic level of the XINT1 pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							XINT1

Bits 7–1 Reserved. The current silicon revision returns zeroes, subject to change in future revisions.

Bit 0 XINT1 Pin Level

0: XINT1 pin is Low
1: XINT1 pin is High

3.4.10 XISTAT2

Full name: External Interrupt 2 Status Register

Address: FF29

Default: 0000 000x

Access: Read Only

XISTAT2 reports the current logic level of the XINT2 pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							XINT2

Bits 7–1 Reserved. The current silicon revision returns zeroes, subject to change in future revisions.

Bit 0 XINT2 Pin Level

0: XINT2 pin is Low
1: XINT2 pin is High

3.5 KEY SCANNER

3.5.1 KPSTAT

Full name: Keypad Status Register

Address: FF2C

Default: 0000 0000

Access: Read Only

KPSTAT reflects the status of the keypad matrix.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ROW			COL			MULTI KEY

Bit 7 Reserved. The current silicon revision returns zeroes, subject to change in future revisions.

Bits 6–4 Row Code

Binary encoding of the active key matrix row pin. If no row pins are active, the value is zero. The code is undefined when multiple keys are active, as detected in bit 0. If the scanner is disabled in MECTR0[7], the value is invalid.

Bits 3–1 Column Code

Binary encoding of the active key matrix column pin. If no column pins are active, the value is zero. The code is undefined when multiple keys are active, as detected in bit 0. If the scanner is disabled in MECTR0[7], the value is invalid.

Bit 0 Multiple Keys Down

0: No more than one key is depressed.
1: More than one key is active; therefore, bits 6–1 are invalid.

3.6 BDMUX

Full name: B/D Channel Port Multiplexer Control Register

Address: FF2F

Default: 0000 0000

Access: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	PIN SELECT		BCH PORT TXSRC	BCH TXSRC		ADPCM RXSRC	

Bit 7 Reserved

Bits 6–5 PIN SELECT[1:0]

Controls the configuration of four multifunction pins, described in Table 3-3.

Bit 4 BCH PORT TXSRC (B Channel Data Output Source)

0: 32 kbit/s B channel output (BCHOUT) on BDP0_OUT2 follows the codec transmit ADPCM output if BDMUX[6:5]=00.

1: BCHOUT follows the unscrambled received B channel if BDMUX[6:5]=00.

Bits 3–2 BCH TXSRC

Identifies the B channel data to be transmitted.

00: Codec transmit ADPCM output

01: BCHIN on the BDP1_OUT3 pin if BDMUX[6:5]=00. If BDMUX[6:5]≠00, operation is unpredictable.

10: Unscrambled received B channel (i.e., Loopback 3)

11: Reserved

Bits 1–0 ADPCM RXSRC (ADPCM Receiver Source)

00: Unscrambled receive B channel

01: BCHIN on the BDP1_OUT3 pin if BDMUX[6:5]=00. If BDMUX[6:5]≠00, operation is unpredictable.

10: Codec transmit ADPCM output (i.e., Loopback 1)

11: Hexadecimal 0

Table 3-3 Pin Select Multifunction Pin Configuration

BDMUX Bits 6–5	Name	BDP0_ OUT2 Pin	BDP1_ OUT3 Pin	BDP2_ OUT4 Pin	BDP3_ OUT5 Pin	Section Ref
00	B Channel	BCHOUT	BCHIN	BCLK	CLK8K	2.4.5, 2.5.2.3
01	Gen Purpose Output	OUT2	OUT3	OUT4	OUT5	2.2.9
10	D Channel	DRXDATA	DTXDATAIO	DRXCLK	DTXCLK	2.5.2.4
11	Formatter Transmit	BDTXCLK	BDTXD	BDTXEN	CLK8K	2.5.2.2

3.7 SERIAL PORT

3.7.1 SIOMODE

Full name: Serial Port Mode

Address: FF30

Default: xxx0 0000

Access: Read/Write

SIOMODE defines the serial port sequence and timing. Refer to Figures 2-3 through 2-7.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			SCLK INVERSION	CLOCK LEVEL SELECT	RX CLOCK EDGE	RX WORD LENGTH	READ/ WRITE

Bits 7–5 Reserved

Bit 4 SCLK Inversion

0: Normal SCLK
1: Inverted SCLK

Bit 3 Clock Active Level Select

0: Active Low clock (i.e., SCLK=1 when no transmission/reception is active).
1: Active High clock (i.e., SCLK=0 when no transmission/reception is active).

Bit 2 Receive Clock Edge

0: SDIN receive data latched on SCLK High-to-Low transition
1: SDIN receive data latched on SCLK Low-to-High transition

Bit 1 Receive Data Length Select

0: 16 bits
1: 8 bits

Bit 0 Write/Write-Read Selection

0: Write-only sequence
1: Write-then-read sequence

3.7.2 SIOTB

Full name: Serial Port Transmit Buffer

Address: FF31

Default: Not applicable

Access: Write Only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
SIOTB							

Writing SIOTB when the serial port is enabled (MECTR0[4]) starts a hardware write or write-read sequence and clears the transmit buffer empty interrupt. Software should allow no writes during transmission or reception.

The length of the data field is programmable from 1 to 8 bits and is defined in the SIOTBL (transmit buffer length) register. Data written to SIOTB is transmitted most significant bit first and must be right justified in the register.

3.7.3 SIORB

Full name: Serial Port Receive Buffer

Address: FF32

Default: xxxx xxxx

Access: Read Only

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIORB							

SIORB is the serial port receive buffer, which is 1 or 2 bytes deep, depending on SIOMODE[1]. The receive buffer is loaded during the second part of the write-read sequence, enabled by SIOMODE[0]. Data is valid only after the SIOSTAT[0] or SIOSRC[0] bits indicate that receive data is available. If a second read operation is initiated before the buffer has been read, the buffer contents are overwritten with the new receive data.

For 8-bit receive data:

- A read returns the receive data byte. The receiver places the first received bit in the most significant position.

For 16-bit receive data:

- 16-bit data operations require two reads, both subject to the requirement that the receive data available indicator is true. The first read returns the first byte received, MSB first, and may be read after the first 8 bits have been received. The second read operation returns the second byte received.

3.7.4 SIOTBL

Full name: Serial Port Transmit Buffer Length

Address: FF33

Default: xxxx x000

Access: Read/Write

SIOTBL defines the number of transmit buffer bits transmitted.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					TRANSMIT BUFFER LENGTH		

Bits 7–3 Reserved

Bits 2–0 Transmit Buffer Length

000: 8 bits
001: 1 bit
010: 2 bits
011: 3 bits
100: 4 bits
101: 5 bits
110: 6 bits
111: 7 bits

3.7.5 SIOSTAT

Full name: Serial Port Status

Address: FF37

Default: 0000 0010

Access: Read Only

SIOSTAT contains the unmasked status of the transmit buffer empty and receive data available indicators.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						TX BUFFER EMPTY	RX BUFFER FULL

Bits 7–2 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1 Transmit Buffer Empty Status

0: The transmit buffer is not empty.
1: The transmit buffer is empty (default state).

Bit 0 Receive Data Available Status

0: No valid data is in the receive buffer.
1: Valid data is in the receive buffer. For 16-bit reads, this bit becomes true when the first 8 bits are received and again when the 16th bit is received.

3.7.6 SIOMASK

Full name: Serial Port Interrupt Mask

Address: FF38

Default: 0000 0000

Access: Read/Write

The SIOMASK interrupt mask lies between the status and source registers. Status bits are logically ANDed with mask bits to yield source bits.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						TX BUFFER EMPTY MASK	RX BUFFER FULL MASK

Bits 7–2 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1 Transmit Buffer Empty Interrupt Mask

0: Transmit buffer empty interrupt disabled
1: Transmit buffer empty interrupt enabled

Note: *In most applications, the software sets Bit 1 only after transmission begins (i.e., after SIOTB is written).*

Bit 0 Receive Data Available Status

0: Receive data available interrupt disabled
1: Receive data available interrupt enabled

3.7.7 SIOSRC

Full name: Serial Port Interrupt Source

Address: FF39

Default: 0000 0000

Access: Read only

SIOSRC contains the masked status of the transmit buffer empty and receive data available indicators.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						TX BUFFER EMPTY FLAG	RX BUFFER FULL FLAG

Bits 7–2 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1 Transmit Buffer Empty Flag

0: The transmit buffer is not empty or SIOMASK[1]=0.
1: The transmit buffer is empty and SIOMASK[1]=1.

Bit 0 Receive Data Available Flag

0: No valid data is in the receive buffer or SIOMASK[0]=0.
1: Valid data is in the receive buffer and SIOMASK[0]=1.

3.7.8 SPTMG

Full name: Serial Port Timing Control Register

Address: FFED

Default: xxxx xx00

Access: Read/Write

SPTMG specifies the clock rate of the serial port enabled by MECTR0[4]. The serial port clock appears on the SCLK pin. To avoid unpredictable clock pulses, software should reprogram bits only when the serial port is disabled.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						SERIAL PORT CLOCK RATE CONTROL	

Bits 7–2 Reserved

Bits 1–0 Serial Port Clock Rate Control

00: Selected SCLK output rate is 36 kHz
01: Selected SCLK output rate is 72 kHz
10: Selected SCLK output rate is 144 kHz
11: Selected SCLK output rate is 288 kHz

3.8 AUDIO MUX

3.8.1 AO2MUX

Full name: AO2 MUX Control Register

Address: FF41

Default: 0xxx 0000

Access: Read/Write

AO2MUX specifies the inputs to be summed to the AO2 output pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AO2 ENABLE	Reserved			TONE RINGER	AI2	Reserved	CODEC D/A

Bit 7 AO2 Enable

0: Analog output AO2 is disabled and high impedance.
1: AO2 is enabled. When first enabled, a stabilization period of ≈200 µs is required.

Bits 6–4 Reserved

Bit 3 Tone Ringer Select

0: No connection of tone ringer to AO2.
1: Tone ringer output summed into AO2 with gain defined by TRAMP register. The tone ringer itself must also be enabled in MECTR0[3].

Bit 2 AI2 Select

0: No connection of AI2 analog input to AO2.
1: AI2 output summed into AO2 with gain defined by AI2CR register. AI2 must be enabled in AI2CTR[7].

Bit 1 Reserved

Bit 0 Codec D/A Select

0: No connection of codec D/A to AO2.
1: The codec D/A output is summed into AO2 with fixed 0 dB gain. The codec must be enabled by setting MECTR0[6] and MECTR1[4].

3.8.2 AO3MUX

Full name: AO3 MUX Control Register

Address: FF42

Default: 0xx0 0x00

Access: Read/Write

AO3MUX specifies the inputs to be summed to the AO3 output pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AO3 ENABLE	Reserved		SIDETONE	TONE RINGER	Reserved	Reserved	CODEC D/A

Bit 7 AO3 Enable

0: Analog output AO3 is disabled and high impedance.
1: AO3 is enabled. When first enabled, a stabilization period of ≈200 µs is required.

Bits 6–5 Reserved

Bit 4 Sidetone Select

0: No connection of sidetone through the AI2 analog input to AO3.
1: Sidetone through the AI2 input is summed into AO3 with gain defined by STCR register. AI2 must be enabled in AI2CTR[7].

Bit 3 Tone Ringer Select

0: No connection of tone ringer to AO3.
1: Tone ringer output summed into AO3 with gain defined by TRAMP register. The tone ringer itself must also be enabled in MECTR0[3].

Bit 2 Reserved

Bit 1 Reserved

Bit 0 Codec D/A Select

0: No connection of codec D/A to AO3.
1: The codec D/A output is summed into AO3 with fixed 0 dB gain. The codec must be enabled by setting MECTR0[6] and MECTR1[4].

3.8.3 ADMUX

Full name: Codec A/D Mux Control Register

Address: FF43

Default: xxxx 000

Access: Read/Write

ADMUX specifies the inputs to be summed into the codec A/D.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				TONE RINGER	AI2	Reserved	CODEC D/A

Bits 7–4 Reserved

Bit 3 Tone Ringer Select

0: No connection of tone ringer to the codec A/D.
1: Tone ringer output summed into the codec A/D with gain defined by TRAMP register. The ringer must also be enabled in MECTR0[3].

Bit 2 AI2 Select

0: No connection of AI2 analog input to the codec A/D.
1: The signal at AI2 is summed into the codec A/D with gain defined by the AI2CTR register. AI2 must be enabled in AI2CTR[7].

Bit 1 Reserved

Bit 0 Codec D/A Select

0: No connection of the codec D/A output to the codec A/D.
1: The codec D/A output is summed into the codec A/D with 0 dB gain. The codec must be enabled by setting MECTR0[6] and MECTR1[4].

3.8.4 AI2CTR

Full name: AI2 Control Register

Address: FF44

Default: 0xx0 0000

Access: Read/Write

AI2CR enables the AI2 analog input buffer and specifies its gain.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AI2 ENABLE	Reserved		AI2 GAIN				

Bit 7 AI2 Enable

0: Analog input AI2 is disabled.

1: AI2 is enabled. When enabled, a stabilization period of ≈ 200 µs is required.

Bits 6–5 Reserved

Bits 4–0 AI2 Gain

This field controls gain applied to the AI2 input signal, as listed in Table 3-4. The peak internal signal level is ±0.5 V.

Table 3-4 AI2 Gain Codes

Bits 4 3 2 1 0	Gain
0 0 0 0 0	3 dB
0 0 0 0 1	6 dB
0 0 0 1 0	9 dB
0 0 1 0 0	12 dB
0 1 0 0 0	15 dB
1 0 0 0 0	18 dB
All other codes	Reserved

3.8.5 STCR

Full name: Sidetone Control Register

Address: FF45

Default: xxx0 0000

Access: Read/Write

STCR enables the sidetone path and sets its amplitude.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				SIDETONE GAIN			

Bits 7–4 Reserved

Bits 3–0 Sidetone Gain

This field controls gain applied to the output of the sidetone path, as listed in Table 3-5 (applicable to SIDETONE GAIN, AO3GAIN, AO2GAIN, and TRAMP).

Table 3-5 Sidetone Gain Codes

Bits 3 2 1 0	Gain
0 0 0 0	Disabled
0 0 0 1	–42 dB
0 0 1 0	–39 dB
0 0 1 1	–36 dB
0 1 0 0	–33 dB
0 1 0 1	–30 dB
0 1 1 0	–27 dB
0 1 1 1	–24 dB
1 0 0 0	–21 dB
1 0 0 1	–18 dB
1 0 1 0	–15 dB
1 0 1 1	–12 dB
1 1 0 0	–9 dB
1 1 0 1	–6 dB
1 1 1 0	–3 dB
1 1 1 1	0 dB

3.8.6 A23ATTN

Full name: AO2, AO3 Attenuator Control Register

Address: FF47

Default: 0000 0000

Access: Read/Write

A23ATTN sets the output attenuation of the AO2 and AO3 output buffers.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AO3GAIN				AO2GAIN			

Bits 7–4 AO3 Gain

These 4 bits specify the gain (loss) from input to output of the AO3 buffer and do not affect the sidetone level. Table 3-5 applies.

Bits 3–0 AO2 Gain

These 4 bits specify the amount of gain (loss) from input to output of the AO2 buffer. Table 3-5 applies.

3.9 HANDS-FREE OPERATIONS

3.9.1 RXLEVEL

Full name: Receive Signal Level

Address: FF48

Default: 0000 0000

Access: Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIGN BIT 0	RXPEAK VALUE						

Bit 7 Sign Bit

Always 0

Bits 6–0 Peak Receive Signal Value

This represents the peak amplitude of the receive signal prior to the RXATTN attenuator; in rectified A-law format. Set to 000 0000 after read unless an update occurs during the read.

3.9.2 TXLEVEL

Full name: Transmit Signal Level

Address: FF49

Default: 0000 0000

Access: Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIGN BIT 0	TXPEAK VALUE						

Bit 7 Sign Bit

Always 0

Bits 6–0 Peak Transmit Signal Value

This represents the peak amplitude of the transmit signal prior to the TXATTN attenuator; in rectified A-law format. Set to 000 0000 after read unless an update occurs during the read.

Note: *The hands-free hooks apply to a device that has analog I/O at one end and digital I/O at the other, such as the CPP. It does not apply to the analog-analog path present between the PSTN and a base station-located hands-free microphone and loudspeaker, since this would imply two codecs back to back.*

3.10 TONE RINGER

3.10.1 TRAMP

Full name: Tone Ringer Amplitude Register

Address: FF46

Default: xxxx 0000

Access: Read/Write

TRAMP sets the amplitude for the tone ringer input to the audio multiplexer.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				TRAMP			

Bits 7–4 Reserved

Bits 3–0 Tone Ringer Amplitude

Relative to full scale, according to Table 3-5. The ringer must be enabled in MECTR0[3].

3.10.2 TRFR

Full name: Tone Ringer Frequency Register

Address: FF4B

Default: xxxx xxxx

Access: Read/Write

TRFR establishes the tone ringer frequency and must be initialized before the ringer is enabled in MECTR0[3].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRFR7–TRFR0							

Bits 7–0 Tone Ringer Frequency

Tabulated in Tables and 3.11.1 by frequency and by code value, respectively.

Note: *Do not program the following codes: 00, 1F, 3F, 7F. They are illegal.*

Table 3-6 Tone Ringer Frequency Codes, Ordered by Frequency

Freq (Hz)	TRFR	Freq (Hz)	TRFR	Freq (Hz)	TRFR	Freq (Hz)	TRFR	Freq (Hz)	TRFR
141.15	FF	175.65	99	232.28	B4	342.83	6F	654.53	26
141.75	FE	176.48	32	233.78	68	346.13	DF	666.68	4C
142.27	FC	177.38	65	235.28	D1	349.50	BE	679.28	98
142.88	F9	178.20	CB	236.85	A3	352.95	7C	692.32	30
143.40	F2	179.10	97	238.42	46	356.47	F8	705.90	60
144.00	E4	180.00	2F	240.00	8C	360.00	F0	720.00	C0
144.60	C8	180.90	5F	241.65	19	363.67	E1	734.70	81
145.20	90	181.80	BF	243.22	33	367.35	C3	750.00	03
145.73	21	182.77	7E	244.88	67	371.17	86	765.97	07
146.33	42	183.67	FD	246.60	CE	375.00	0D	782.63	0E
146.92	85	184.65	FB	248.25	9C	378.97	1A	800.02	1D
147.52	0A	185.55	F7	249.97	39	382.95	34	818.18	3A
148.13	14	186.52	EF	251.78	73	387.07	69	837.23	74
148.80	29	187.50	DE	253.50	E7	391.28	D3	857.18	E9
149.40	53	188.48	BC	255.30	CF	395.63	A6	878.02	D2
150.00	A7	189.45	79	257.17	9E	399.97	4D	900.00	A4
150.60	4F	190.50	F3	258.97	3C	404.47	9A	923.10	48
151.27	9F	191.48	E6	260.85	78	409.13	35	947.40	91
151.88	3E	192.53	CD	262.80	F1	413.78	6B	972.98	23
152.55	7D	193.58	9B	264.67	E3	418.57	D6	999.98	47
153.23	FA	194.63	37	266.70	C6	423.53	AD	1028.55	8E
153.83	F5	195.67	6E	268.65	8D	428.55	5B	1058.85	1C
154.50	EA	196.72	DD	270.67	1B	433.72	B6	1090.95	38
155.17	D5	197.78	BB	272.70	36	439.05	6D	1125.00	71
155.85	AA	198.90	77	274.80	6C	444.45	DA	1161.30	E2
156.52	55	200.03	EE	276.90	D8	450.00	B5	1200.00	C4
157.20	AB	201.15	DC	279.08	B0	455.70	6A	1241.40	88
157.88	57	202.28	B9	281.25	61	461.55	D4	1285.73	10
158.63	AE	203.40	72	283.50	C2	467.55	A8	1333.35	20
159.30	5C	204.53	E5	285.75	84	473.70	50	1440.00	80
159.98	B8	205.72	CA	288.00	08	480.00	A0	1500.00	01
160.73	70	206.92	95	290.33	11	486.53	41	1565.25	02
161.48	E0	208.13	2A	292.65	22	493.13	82	1636.35	05
162.15	C1	209.33	54	295.05	45	500.03	04	1714.27	0B
162.90	83	210.53	A9	297.53	8B	507.07	09	1800.00	16
163.65	06	211.80	52	300.00	17	514.28	13	1894.73	2C
164.40	0C	213.00	A5	302.55	2E	521.78	27	2000.02	58
165.15	18	214.28	4A	305.10	5D	529.43	4E	2117.63	B1
165.90	31	215.55	94	307.72	BA	537.30	9D	2250.00	63
166.65	62	216.90	28	310.35	75	545.47	3B	2400.00	C7
167.48	C5	218.17	51	313.05	EB	553.88	76	2571.45	8F
168.23	8A	219.53	A2	315.83	D7	562.50	EC	2769.23	1E
169.05	15	220.88	44	318.60	AF	571.43	D9	3000.00	3D
169.80	2B	222.22	89	321.45	5E	580.65	B2	3272.70	7A
170.63	56	223.58	12	324.30	BD	590.18	64	3600.00	F4
171.45	AC	225.00	25	327.30	7B	600.00	C9	3999.97	E8
172.27	59	226.42	4B	330.30	F6	610.20	92	4500.00	D0
173.10	B3	227.85	96	333.30	ED	620.70	24	5142.83	A1
173.92	66	229.28	2D	336.45	DB	631.57	49	6000.00	43
174.75	CC	230.78	5A	339.60	B7	642.82	93	7200.00	87

Table 3-7 Tone Ringer Frequency Codes, Ordered by Code

Code	TRFR	Code	TRFR	Code	TRFR	Code	TRFR	Code	TRFR
00	Reserved	37	194.63	6E	195.67	A5	213.00	DA	444.45
01	1500.00	38	1090.95	6F	342.83	A6	395.63	DB	336.45
02	1565.25	39	249.97	70	160.73	A7	150.00	DC	201.15
03	750.00	3A	818.18	71	1125.00	A8	467.55	DD	264.67
04	500.03	3B	545.47	72	203.40	A9	210.53	DE	196.72
05	1636.35	3C	258.97	73	251.78	AA	155.85	DF	346.13
06	163.65	3D	3000.00	74	837.23	AB	157.20	E0	161.48
07	765.97	3E	151.88	75	310.35	AC	171.45	E1	363.67
08	288.00	3F	Reserved	76	553.88	AD	423.53	E2	1161.30
09	507.07	40	1384.65	77	198.90	AE	158.63	E3	264.67
0A	147.52	41	486.53	78	260.85	AF	318.60	E4	144.00
0B	1714.27	42	146.33	79	189.40	B0	279.08	E5	204.53
0C	164.40	43	6000.00	7A	3272.70	B1	2117.63	E6	191.48
0D	375.00	44	220.88	7B	327.30	B2	580.65	E7	253.50
0E	782.63	45	295.05	7C	352.95	B3	173.10	E8	3999.97
0F	9000.00	46	238.42	7D	152.55	B4	232.28	E9	857.18
10	1285.73	47	999.98	7E	182.77	B5	450.00	EA	154.50
11	290.33	48	923.10	7F	Reserved	B6	433.72	EB	313.05
12	223.58	49	631.57	80	1440.00	AF	318.60	EC	562.50
13	514.28	4A	214.28	81	734.70	B0	279.08	ED	333.30
14	148.13	4B	226.42	82	493.13	B7	339.60	EE	200.03
15	169.05	4C	666.68	83	162.90	B8	159.98	EF	186.52
16	1800.00	4D	399.97	84	285.75	B9	202.28	F0	360.00
17	300.00	4E	529.43	85	146.92	BA	307.72	F1	262.80
18	165.15	4F	150.60	86	371.17	BB	197.78	F2	143.40
19	241.65	50	473.70	87	7200.00	BC	188.48	F3	190.50
1A	378.97	51	218.17	88	1241.40	BD	324.30	F4	3600.00
1B	270.67	52	211.80	89	222.22	BE	349.50	F5	153.83
1C	1058.85	53	149.40	8A	168.23	BF	181.80	F6	330.30
1D	800.02	54	209.33	8B	297.53	C0	720.00	F7	185.55
1E	2769.23	55	156.52	8C	240.00	C1	162.15	F8	356.47
1F	Reserved	56	170.63	8D	268.65	C2	283.50	F9	142.88
20	1333.35	57	157.88	8E	1028.55	C3	367.35	FA	153.23
21	145.73	58	2000.02	8F	2571.45	C4	1200.00	FB	184.65
22	292.65	59	167.27	90	145.20	C5	167.48	FC	142.27
23	972.98	5A	230.78	91	947.40	C6	266.70	FD	183.67
24	620.70	5B	428.55	92	610.20	C7	2400.00	FE	141.75
25	225.00	5C	159.30	93	642.82	C8	144.60	FF	141.15
26	654.53	5D	305.10	94	215.55	C9	600.00		
27	521.78	5E	321.45	95	206.92	CA	205.72		
28	216.90	5F	180.90	96	227.85	CB	178.20		
29	148.80	60	705.90	97	179.10	CC	174.75		
2A	208.13	61	281.25	98	679.28	CD	192.53		
2B	169.80	62	166.65	99	175.65	CE	246.60		
2C	1894.73	63	2250.00	9A	404.47	CF	255.30		
2D	229.28	64	590.18	9B	193.58	D0	4500.00		
2E	302.55	65	177.38	9C	248.25	D1	235.28		
2F	180.00	66	173.92	9D	537.30	D2	878.02		
30	692.32	67	244.88	9E	257.17	D3	391.28		
31	165.90	68	233.78	9F	151.27	D4	461.55		
32	167.48	69	387.07	A0	480.00	D5	155.17		
33	243.22	6A	455.70	A1	5142.83	D6	418.57		
34	382.95	6B	413.78	A2	219.53	D7	315.83		
35	409.13	6C	274.80	A3	236.85	D8	276.90		
36	272.70	6D	439.05	A4	900.00	D9	571.43		

3.11 MODULATOR

3.11.1 MODTST

Full name: Modulator Test Mode Register

Address: FF4D

Default: xxx0 x000

Access: Read/Write

MODTST enables constant transmission modes for the Baseband Output Driver for the purpose of spectral measurement. When in Test mode, the modulator ignores the Digital Formatter data and transmits instead either an internally generated fixed pattern or arbitrary data from an external source. To use the external source, BDMUX[6:5] must be programmed to 11. The external source drives data on the BDP1_OUT3 pin, clocked by rising edges of the 72 kHz clock output on the BDP0_OUT2 pin. The modulator must be enabled in MECTR1[5] in order to function.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			NRZ/IQ	Reserved	MOD TEST ENABLE	TEST MODE	

Bits 7–5 Reserved

Bit 4 I-Q/NRZ Data Output Format

- 0: I-Q analog output
- 1: NRZ quasi-digital output

Bit 3 Reserved

Bit 2 Modulator Test Enable

- 0: Disable Test mode, (i.e., Normal mode)
- 1: Enable Test mode

Bits 1–0 Modulator Test Mode

- 00: Transmit all 0s (i.e., $\omega_m(t) = \omega_{min} = -2\pi \bullet 18$ kHz for I-Q format)
- 01: Transmit data from external source
- 10: Transmit alternating 1s and 0s (i.e., $\omega_m(t) = \pm 2\pi \bullet 18$ kHz for I-Q format)
- 11: Transmit all 1s (i.e., $\omega_m(t) = \omega_{max} = +2\pi \bullet 18$ kHz for I-Q format)

3.12 BATTERY DETECT

3.12.1 BATLEV

Full name: Battery-Level Register

Address: FF4E

Default: 00xx 0000

Access: Read/Write

BATLEV returns the result of a comparison between a written value and the main power supply voltage. The values returned are absolute voltages, referenced to ground.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BATTERY OK	SOURCE SELECT	Reserved		THRESH			

Bit 7 Battery OK is the read-only comparison result.

0: V_{CC} < value programmed in bits [3:0]

1: V_{CC} > value programmed in bits [3:0]

Bit 6 Battery Source Selection
Controls which signal is presented to the A/D for conversion.

0: Chip V_{CC}. Internally-scaled version of the device power supply.

1: Pin ROW1. Internal pull-downs are disabled. Useful for voltage-regulated systems.

Bits 5–4 Reserved

Bits 3–0 THRESH is the battery comparison threshold code, detailed in Table 3-8.

Table 3-8 Battery-Level Comparison Threshold Codes

Bits 3 2 1 0	Bit 6 = 0 Nominal Threshold Voltage at Vcc Pin (V)	Bit 6 = 1 Nominal Threshold Voltage at ROW1 Pin (V)
0 0 0 0	2.688	0.645
0 0 0 1	2.856	0.685
0 0 1 0	3.024	0.726
0 0 1 1	3.192	0.766
0 1 0 0	3.360	0.806
0 1 0 1	3.528	0.847
0 1 1 0	N/A	0.887
0 1 1 1	N/A	0.927
1 0 0 0	N/A	0.968
1 0 0 1	N/A	1.008
1 0 1 0	N/A	1.048
1 0 1 1	N/A	1.089
1 1 0 0	N/A	1.129
1 1 0 1	N/A	1.169
1 1 1 0	N/A	1.210
1 1 1 1	N/A	1.250

3.13 RSSI

3.13.1 RSSICFG

Full name: RSSI Configuration/Status Register

Address: FF4C

Default: xxxx x000

Access: Read/Write

RSSICFG enables the PCI mode features not available on earlier versions of the PhoX device.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					ENABLE NEW FEATURES	RX/TX WINDOW SELECT	CONVERSION TYPE

Bits 7–3 Reserved

Bit 2 Enable New Features (Modifies operation of RSSISTAT Register FF4F)

- 0: RSSISTAT register operates as in earlier PhoX revisions. RSSICFG register is disabled.
- 1: RSSISTAT and RSSICFG registers have a superset of functions enabled for PCI-required functionality.

Bit 1 Report Receive or Transmit RSSI value and conversion status

- 0: Receive window RSSI measurements are reported in RSSISTAT[4:0].
- 1: Transmit window RSSI measurements are reported in RSSISTAT[4:0].

Bit 0 Conversion Type (Window determined by RSSISTAT[7] and/or RSSISTAT[5])

- 0: Single conversion
- 1: Continuous conversion

3.13.2 RSSISTAT

Full name: RSSI Status Register

Address: FF4F

Default: 0x0x xxxx

Access: Read/Write

RSSISTAT operation can be modified by RSSICFG[2]. The RSSISTAT register reports the result of the RSSI A/D conversion of the voltage at the RSSI pin. The register description below is in two parts as determined by RSSICFG[2].

3.13.2.1 RSSICFG[2] = 0 Normal Operation

Setting bit 7 requests a conversion. Software polls RSSISTAT until bit 7 is cleared by hardware, indicating that the conversion is complete and bits 4–0 have a valid code. Bit 6 reports the status of microcontroller port pin P1.7, allowing a simultaneous read of the RSSI level and some arbitrary digital input, such as reporting channel status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSSI REQUEST	P1.7 STATUS	Reserved	RSSI VALUE				

Bit 7 RSSI Request

0: Read conversion complete
1: Write conversion request, read conversion not complete

Bit 6 Microcontroller Port Pin P1.7 Status (read only)

Pin P1.7 may be used to monitor the free channel status signal.

0: P1.7 is 0
1: P1.7 is 1

Bit 5 Reserved. Software must write zero. Reads return zeroes, subject to change in future silicon revisions.

Bits 4–0 RSSI Value

These bits report the result of the A/D conversion listed in Table 3-9.

3.13.2.2 RSSICFG[2] = 1 Enhanced RSSI Feature Set Enabled

Setting bit 7 requests an RX Window conversion that is either a single or continuous conversion as defined by RSSICFG[0].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSSI RX REQUEST	RSSI SYNC	RSSI TX REQUEST	RSSI VALUE				

Bit 7 RSSI RX Conversion Request

0: Initial read conversion complete
1: Write conversion request, clears RSSISTAT[4:0], read conversion not complete

Bit 6 RSSISYNC Mode Indicator

0: RSSI operating in Synchronous mode, RSSISTAT[4:0] operation determined by RSSICFG[1]
1: RSSI operating in Asynchronous mode, RSSISTAT[4:0] indicates RX Peak Value

Bit 5 RSSI TX Request

0: Initial read conversion complete

1: Write initiates conversion, clears the TX Peak Detect register. When returned from a read, this defines the conversion as incomplete.

Bits 4–0 RSSI Value

These five bits report the result of the A/D conversion, listed in Table 3-9.

Table 3-9 RSSI Codes

RSSISTAT Bits 4 3 2 1 0	Nominal Center Voltage	RSSISTAT Bits 4 3 2 1 0	Nominal Center Voltage
0 0 0 0 0	0.220	1 0 0 0 0	0.760
0 0 0 0 1	0.253	1 0 0 0 1	0.794
0 0 0 1 0	0.287	1 0 0 1 0	0.828
0 0 0 1 1	0.321	1 0 0 1 1	0.861
0 0 1 0 0	0.355	1 0 1 0 0	0.895
0 0 1 0 1	0.389	1 0 1 0 1	0.929
0 0 1 1 0	0.422	1 0 1 1 0	0.963
0 0 1 1 1	0.456	1 0 1 1 1	0.997
0 1 0 0 0	0.490	1 1 0 0 0	1.030
0 1 0 0 1	0.524	1 1 0 0 1	1.064
0 1 0 1 0	0.557	1 1 0 1 0	1.098
0 1 0 1 1	0.591	1 1 0 1 1	1.132
0 1 1 0 0	0.625	1 1 1 0 0	1.166
0 1 1 0 1	0.659	1 1 1 0 1	1.199
0 1 1 1 0	0.693	1 1 1 1 0	1.233
0 1 1 1 1	0.726	1 1 1 1 1	1.267

3.14 DUAL-TONE GENERATOR

3.14.1 T1FR1–3, T2FR1–3 (Dual-Tone Frequency)

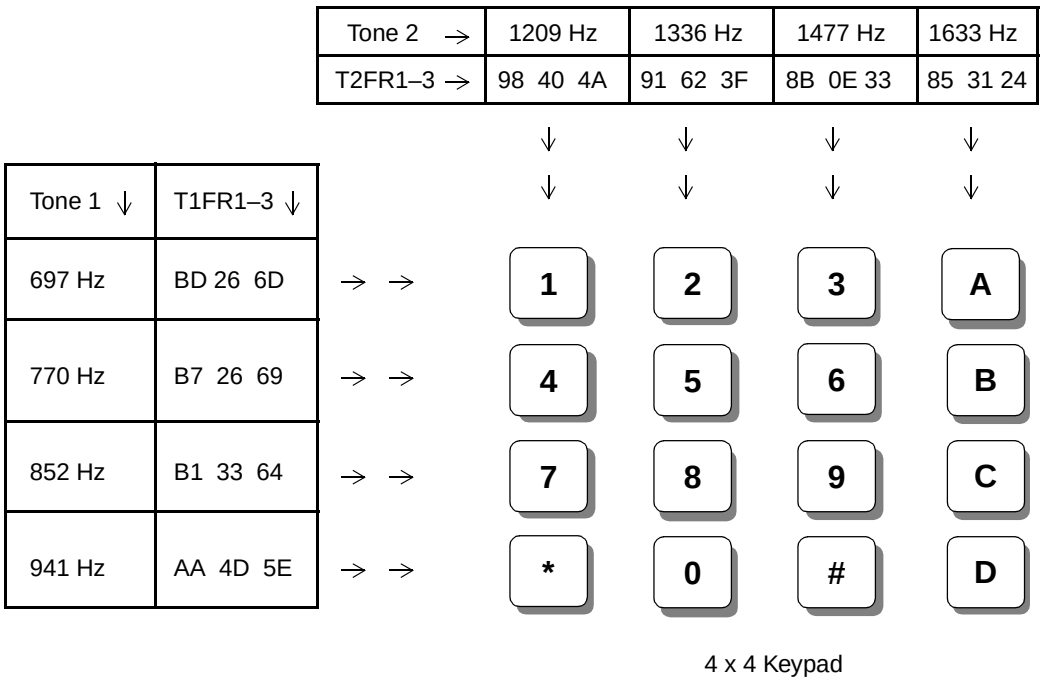
T1FR1–T1FR3 (Tone 1 Frequency Registers 1 through 3) and T2FR1–T2FR3 control the frequency of the first and second tones, respectively, from the dual-tone generator. They are actually RAM locations that reset to indeterminate states and therefore must be initialized before the codec block is enabled.

All dual-tone generator values (i.e., data space FF50–FF59) are double-buffered and progress to the coefficient RAM simultaneously, keyed by a write to the RTAR location (address FF59). Therefore, if a change in any DTMF-related value is required, the write sequence must conclude with a write to RTAR.

Figure 3-1 is a short-form listing of standard DTMF tones. Appendix A is a full list of valid values, in order of increasing frequency.

Mnemonic	Address
T1FR1	FF50
T1FR2	FF51
T1FR3	FF52
T2FR1	FF55
T2FR2	FF56
T2FR3	FF57

Figure 3-1 DTMF Frequency Short-Form Reference



3.14.2 T1AR, T2AR (Dual-Tone Amplitude)

T1AR (Tone 1 Amplitude Register) and T2AR control the amplitudes of the first and second tones, respectively, from the dual-tone generator. After application of the programmed gains, the two tones are summed; therefore, gains should be programmed such that the sum of the two tones does not cause the digital signal processor accumulator to overflow, resulting in clipping. T1AR and T2AR are RAM locations that reset to indeterminate states and therefore must be initialized before the codec block is enabled.

All dual-tone generator values (i.e., data space FF50–FF59) are double-buffered and progress to the digital signal processor simultaneously, keyed by a write to the RTAR location (address FF59). Therefore, if a change in any dual-tone generator value is required, the write sequence must conclude with a write to RTAR.

Note: *All tones in the receive path are subject to the codec low-pass filter transfer function, which rolls-off high frequencies according to the frequency response template specified in Table 6-3. The amplitude error column in* Appendix A*,* 80C32T2 Appendices, PhoX™ Controller for Digital Cordless Telephones *does not reflect this low-pass characteristic. The actual output level includes the T1AR/T2AR, RTAR, amplitude error (Appendix A), and frequency response template gain terms. When the codec is programmed for DTMF-only operation, out-of-bound tones (i.e., > 3.4 kHz) are subject to a different Frequency Response Template, which is not guaranteed or characterized in this document.*

Table 3-10 lists valid values.

Mnemonic	Address
T1AR	FF53
T2AR	FF58

Table 3-10 Attenuation Codes—Valid for T1AR, T2AR, RTAR, TTAR, RXATTN, and TXATTN

Code	Attenuation (dB)	Code	Attenuation (dB)	Code	Attenuation (dB)
00	No Output	30	–8.52	60	–3.50
01	–42.14	31	–8.34	61	–2.41
02	–36.12	32	–8.16	62	–2.32
03	–32.60	33	–7.99	63	–2.23
04	–30.10	34	–7.82	64	–2.14
05	–28.16	35	–7.66	65	–2.06
06	–26.58	36	–7.50	66	–1.97
07	–25.24	37	–7.34	67	–1.89
08	–24.08	38	–7.18	68	–1.80
09	–23.06	39	–7.03	69	–1.72
0a	–22.14	3a	–6.88	6a	–1.64
0b	–21.32	3b	–6.73	6b	–1.56
0c	–20.56	3c	–6.58	6c	–1.48
0d	–19.87	3d	–6.44	6d	–1.40
0e	–19.22	3e	–6.30	6e	–1.32
0f	–18.62	3f	–6.16	6f	–1.24
10	–18.06	40	–6.02	70	–1.16
11	–17.54	41	–5.89	71	–1.08
12	–17.04	42	–5.75	72	–1.01
13	–16.57	43	–5.62	73	–0.93
14	–16.12	44	–5.49	74	–0.86
15	–15.70	45	–5.37	75	–0.78
16	–15.30	46	–5.24	76	–0.71
17	–14.91	47	–5.12	77	–0.63
18	–14.54	48	–5.00	78	–0.56
19	–14.19	49	–4.88	79	–0.49
1a	–13.84	4a	–4.76	7a	–0.42
1b	–13.52	4b	–4.64	7b	–0.35
1c	–13.20	4c	–4.53	7c	–0.28
1d	–12.90	4d	–4.41	7d	–0.21
1e	–12.60	4e	–4.30	7e	–0.14
1f	–12.32	4f	–4.19	7f	–0.07
20	–12.04	50	–4.08		
21	–11.77	51	–3.97		
22	–11.51	52	–3.87		
23	–11.26	53	–3.76		
24	–11.02	54	–3.66		
25	–10.78	55	–3.56		
26	–10.35	56	–3.45		
27	–10.32	57	–3.35		
28	–10.10	58	–3.25		
29	–9.89	59	–3.16		
2a	–9.68	5a	–3.06		
2b	–9.47	5b	–2.96		
2c	–9.28	5c	–2.87		
2d	–9.08	5d	–2.77		
2e	–8.89	5e	–2.68		
2f	–8.70	5f	–2.59		

3.14.3 TTAR, RTAR (Dual-Tone Path Attenuation)

TTAR (Transmit Tone Attenuation Register) and RTAR (Receive Tone Attenuation Register) control the level of the dual-tone signal in the transmit and receive data paths, respectively. After application of the programmed attenuation, the dual-tone signal is summed with audio data; therefore, attenuations should be programmed such that the sum of the dual-tone signal and audio data does not cause the codec accumulator to overflow, resulting in clipping. TTAR and RTAR are RAM locations that reset to indeterminate states and therefore must be initialized before the codec block is enabled.

All dual-tone generator values (i.e., data space FF50–FF59) are double-buffered and progress to the digital signal processor simultaneously, keyed by a write to the RTAR location (address FF59). Therefore, if a change in any dual-tone generator value is required, the write sequence must conclude with a write to RTAR.

Table 3-10 lists valid values.

Mnemonic	Address
TTAR	FF54
RTAR	FF59

3.15 CODEC

3.15.1 TXATTN

Full name: Transmit Attenuation

Address: FF5A

Default: xxxx xxxx

Access: Read/Write

The TXATTN byte controls the attenuation applied to the transmitted B channel data. It is a RAM location that must be initialized before the codec is enabled. Codes are tabulated in Table 3-10.

3.15.2 RXATTN

Full name: Receive Attenuation

Address: FF5B

Default: xxxx xxxx

Access: Read/Write

The RXATTN byte controls the attenuation applied to the received B channel data. It is a RAM location that must be initialized before the codec is enabled. Codes are tabulated in Table 3-10.

3.15.3 DSPCTR

Full name: Digital Signal Processor Control Register

Address: FF5C

Default: 0000 0000

Access: Read/Write

DSPCTR controls the codec operating mode when it is enabled by MECTR0[6]. For valid results, software must disable the codec by clearing MECTR0[6] before changing DSPCTR.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		NOISE SUPPR ENABLE	Reserved				

Bit 7, 6 Reserved

Bit 5 Noise Suppression Enable

- 0: Noise suppression algorithm is disabled
- 1: Enable noise suppression, further controlled in NSCTR, NSTHR, MUTE, and JITCTR registers

Bits 4–0 Reserved

3.16 NOISE SUPPRESSION

3.16.1 NSCTR

Full name: Noise Suppression Control Register

Address: FF2E

Default: 0000 0000

Access: Read/Write

NSCTR controls the behavior of the noise suppression algorithm.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
JITTER STATUS	DSP NOISE STATUS	DSPINT EN	ADPCM = 0 STATUS	MUTE MODE		MUTE STEP	

Bit 7 Jitter Status (read only)

Set by a jitter detection trigger. Cleared by reading the register.

0: No jitter has occurred since the last read of this register.
1: Jitter has occurred on the radio link, as defined by the JITTER register, since this register was last read.

Bit 6 DSP Noise Status (read only)

Active High if enabled in bit 5 and set by a DSP-based noise detection trigger. Cleared by reading the register.

0: No DSP-based noise trigger occurred since NSCTR was last read.
1: A DSP-based noise trigger occurred in the codec receiver since last read of NSCTR.

Bit 5 DSP Noise Interrupt Enable

0: Noise interrupt and status indicator disabled.
1: Enable the DSP Noise Status Bit (bit 6) and a corresponding interrupt (jitter) reported in MISRC0[5] to indicate that a codec DSP-based noise trigger occurred, regardless of whether actual muting is enabled to occur.

Bit 4 ADPCM = 0 Status (read only)

Set by reception of ADPCM nibble = 0000. Cleared by reading the register. The 4-zero ADPCM pattern is an illegal code and indicates an error and possible signal loss/fade condition.

0: No 4-zero ADPCM nibble is detected
1: 4-zero ADPCM nibble is detected

Bits 3–2 Mute mode

Applicable when noise suppression is enabled in DSPCTR[5].

00: Trigger mute sequence on DSP noise or jitter detection
01: Trigger mute sequence on DSP noise detection only
10: Trigger mute sequence on jitter detection only
11: Trigger mute sequence on concurrent DSP noise and jitter detection

Bits 1–0 Mute Sequence

Applicable when noise suppression or 4-zero ADPCM detection is enabled. See Figure 2-21. A mute sequence is initiated when noise is detected,

according to the Mute mode bits above. Each attenuation step lasts a duration specified in the MUTE register.

00: Full mute, 0 dB
01: Full mute, –6 dB, 0 dB
10: Full mute, –12 dB, –6 dB, 0 dB
11: Full mute, –18 dB, –12 dB, –6 dB, 0 dB

3.16.2 NSTHR

Full name: Noise Threshold

Address: FF5D

Default: xxxx xxxx

Access: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	THR [3]	THR [2]	THR [1]	THR [0]	THR [-1]	THR [-2]	THR [-3]

Bit 7 Reserved. Must be written to 0. Reads back the value written.

Bits 6–0 Threshold

The THR field sets the trigger level, in dB, for noise detected in the B channel. The noise detector calculates the ratio of predicted received signal to the difference between predicted and actual received signal, and generates a muting trigger when the ratio falls below the programmed threshold. Therefore, increasing THR makes the mute mechanism more sensitive to noise but more likely to trigger on genuine non-noisy speech. Low values allow more tolerance.

THR is a binary representation, in the form 3 2 1 0. –1 –2 –3. THR[3:0] is a whole number and THR[–1, –2, –3] forms the fractional part.

For example, 9.75 dB is represented as NSTHR = 0 1001 110 (9 + 0.5 + 0.25). The maximum is 15.875 dB.

3.16.3 MUTE

Full name: Noise Suppression Mute Length

Address: FF5E

Default: xxxx xxxx

Access: Read/Write

MUTE defines the length of muting steps (defined in NSCTR[1:0]) in the noise suppression algorithm. It is a RAM location and therefore must be initialized before noise suppression is enabled. Muting is caused by DSP noise or jitter enabled in NSCTR[3:2], or 4-zero ADPCM enabled in DEVMODE[2].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	MUTE						

Bit 7 Reserved. Must be written to 0. Reads back the value written.

Bits 6–0 MUTE[6:0]

Binary representation, from 0 to 127, of the duration of the noise suppression attenuation steps, in units of 125 μs frame periods.

3.16.4 JITCTR

Full name: Jitter Detection Control Register

Address: FFC7

Default: 0000 0000

Access: Read/Write

JITCTR determines the threshold for detecting jitter in the radio link for the purposes of link maintenance and B channel noise suppression.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EVENT THRSH				PHASE THRSH			

Bits 7–4 EVENT THRSH (Event Threshold)

The event threshold specifies the minimum number of jitter events that must occur during a frame to cause the noise suppression jitter trigger to become active, according to Table 3-11.

Bits 3–0 PHASE THRSH (Phase Threshold)

The phase threshold specifies in degrees, relative to the expected receive bit boundary, the amount of phase error that causes a jitter error event to be counted, listed in Table 3-12.

Table 3-11 Jitter Event Threshold Codes

Event THRSH 3 2 1 0	Jitter Events per 2 ms Frame
0 0 0 0	4
0 0 0 1	8
0 0 1 0	12
0 0 1 1	16
0 1 0 0	20
0 1 0 1	24
0 1 1 0	28
0 1 1 1	32
1 0 0 0	36
1 0 0 1	40
1 0 1 0	44
1 0 1 1	48
1 1 0 0	52
1 1 0 1	56
1 1 1 0	60
1 1 1 1	64

Table 3-12 Jitter Phase Threshold Codes

Phase THRSH 3 2 1 0	Phase Error (degrees)
0 0 0 0	None reported
0 0 0 1	168.75
0 0 1 0	157.5
0 0 1 1	146.25
0 1 0 0	135.00
0 1 0 1	123.75
0 1 1 0	112.50
0 1 1 1	101.25
1 0 0 0	90.00
1 0 0 1	78.75
1 0 1 0	67.50
1 0 1 1	56.25
1 1 0 0	45.00
1 1 0 1	33.75
1 1 1 0	22.50
1 1 1 1	11.25

3.17 DIGITAL FORMATTER

3.17.1 RXBUF0–5

Full name: D Channel Receive Buffer (Six Bytes)

Address: RXBUF0 FFC0
RXBUF1 FFC1
RXBUF2 FFC2
RXBUF3 FFC3
RXBUF4 FFC4
RXBUF5 FFC5

Default: xxxx xxxx

Access: Read Only

Received D channel data is stored in the receive buffer, starting with RXBUF0 bit 0 (corresponding to bit 1 of byte 1, in the received code word) and ending with RXBUF5 bit 7 (bit 8 of byte 6). The receive buffer full flag is set by hardware when the last bit of the code word is received. The flag is cleared by reading the most significant byte of the buffer (FFC5).

The receive buffer can retain either one or two complete code words, depending on DEVMODE[6].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXBUFx							

3.17.2 TXBUF0–5

Full name: D Channel Transmit Buffer (six bytes)

Address: TXBUF0 FFC0
TXBUF1 FFC1
TXBUF2 FFC2
TXBUF3 FFC3
TXBUF4 FFC4
TXBUF5 FFC5

Default: xxxx xxxx

Access: Write Only

The 6 transmit buffer bytes are transmitted serially in the D channel, starting with TXBUF0 bit 0 (corresponding to bit 1 of byte 1 in the transmitted code word) and ending with TXBUF5 bit 7 (bit 8 of byte 6). When the buffer is empty, as defined by the D Channel Transmit Control Register, the transmit buffer empty flag is set. Writing the last byte, TXBUF5, clears the flag.

The transmit buffer can be loaded with either one or two complete code words, depending on DEVMODE[6].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXBUFx							

3.17.3 DEVMODE

Full name: Device Mode Select Register

Address: FFC6

Default: 0000 00xx

Access: Read/Write

This register defines the operation of the PhoX device, as either a CFP or a CPP. The Formatter must be in Clear mode (program TXMUX[1:0]=11 and RXMUX[1:0]=11) to change the contents of this register with predictable results.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPP/CFP	DOUBLE BUFFER	D Channel Training	Reserved	FDD Mode Enable	4-ZERO ADPCM DETECT	Reserved	

Bit 7 CPP/CFP Mode Selection

0: The PhoX device operates as a Cordless Fixed Part (CFP).

1: The device operates as a Cordless Portable Part (CPP). The Formatter must be in Clear mode (program TX MUX = 3 and RX MUX = 3) to change the device mode.

Bit 6 Double Buffer Enable

0: Transmit and Receive Buffers are one code word deep only. In the transmitter, software control of the SYNCDC register determines insertion of SYNCDC. In the receiver, the RDATAC command controls the location of a new packet by searching for the SYNCD pattern.

1: Transmit and Receive Buffers are two code words deep. In the transmitter, insertion of SYNCD automatically occurs when the code word is an address code word, determined by bit 0 of TXBUF0. In the receiver, hardware determines the end boundary of the packet and automatically issues an RDATAC command when the packet is complete and the last code word is error-free. The receiver is responsive to software-generated RDATAC commands to force receiver D Channel resynchronization. Setting bit 6 High also redefines the DCHSTAT register bits to reflect the double buffer status.

Bit 5 D Channel Training

0: Normal operation

1: First D-field is ignored for MUX1.4 and MUX2 modes.

Bit 3 FDD Mode Enable

0: Disable FDD mode

1: Enable FDD mode

The FDD mode allows simultaneous transmits/receives on different radio channels at 36 kbits/s, inhibiting time division burst of Formatter. FDD mode is available in MUX1.4 and MUX2. Enable RX independent timing in both the CFP and CPP, in PLLCTRL[4].

Bit 2 4-Zero ADPCM Detect

0: Detection of 4-zero ADPCM nibble (error condition) disabled

1: Detection of 4-zero ADPCM nibble (error condition) enabled and triggers mute algorithm. Mute steps set in NSCTR[1:0] and the mute duration set in MUTE. Detection is reported in NSCTR[4] and can cause an interrupt enabled by NSCTR[5].

Bits 4,1–0 Reserved

3.17.4 RXTMGR

Full name: Receive Timing Recovery Register

Address: FFC8

Default: 000x 0000

Access: Read/Write

RXTMGR enables timing recovery, specifies the timing recovery speed, and reports link synchronization status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC STATUS	PLL SPEED STATUS	SYNC RELEASE STATUS	Reserved	HOLD ADJ	MULTI SAMPLE	RECOVERY SPEED CONTROL	RX TIMING RECOVERY ENABLE

Bit 7 Synchronization Status (read only)

0: The receiver has not obtained frame (SYN Channel) synchronization.

1: The receiver has obtained frame (SYN Channel) synchronization.

Bit 6 Phase-Locked Loop Speed Status (read only)

0: The receiver phase-locked loop is in High-speed or Low-speed mode, according to the value in bit 1.

1: The receiver has detected a SYN channel marker; therefore, the PLL response is automatically forced to low speed, regardless of bit 1.

Bit 5 Synchronization Release Status (read only)

0: Default. A zero also indicates that frame synchronization is cleared, due to a write to SYNCTR.

1: SYNCTR has been written to initiate the clearing of the frame synchronization, but it is not yet cleared.

Bit 4 Reserved

Bit 3 Hold PLL Adjustments

Setting this bit stops adjustment of the receiver clock recovery PLL and keeps the receive data sampling point fixed relative to the locally derived 72 kHz frequency, with a phase offset determined by the last PLL adjustment.

0: Enable PLL adjustments if enabled in bit 0.

1: Hold PLL adjustments and the data sampling point, regardless of bit 0.

Bit 2 Receiver Multisampling

When disabled, the receiver samples data once in the middle of the bit period. When enabled, receive data is calculated as the value occurring at least twice among three samples, taken symmetrically about the center of the bit period and separated by 1.7 µs. Multiple sampling functions only when timing recovery is enabled in bit 0; if bit 0 is cleared, the receiver samples singly, regardless of bit 2.

0: Single receive sampling

1: Multiple receive sampling

Bit 1 Phase-Locked Loop Timing Recovery Speed Control

0: High-speed phase-locked loop response, changing to low speed automatically
1: Forced low-speed phase-locked loop response

Bit 0 Receiver Timing Recovery Enable

When set, this control enables the clock recovery PLL and allows it to adjust the receive data sampling window, ±¼ of a bit relative to the overall receiver window. Additional flexibility is provided by the independent RX timing option enabled in PLLCTRL[4], which enables the RX window to adjust with respect to the TX window.

0: Disable
1: Enable

3.17.5 TXMUX

Full name: Transmit Frame Control Register

Address: FFC9

Default: xxxx x011

Access: Read/Write

TXMUX controls the Multiplex mode of the transmitter and selects the SYNC or CHM pattern for the SYN channel.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					TX SYN SELECT	TX MUX	

Bits 7–3 Reserved

Bit 2 Transmit SYN Channel Pattern Select

0: CHMP or CHMF, depending on the DEVMODE register
1: SYNCF or SYNCP, depending on the DEVMODE register

Bits 1–0 Transmit Multiplex Selection

The formatter is cleared if TXMUX and RXMUX are both programmed for MUX3.

00: MUX1.2
01: MUX1.4
10: MUX2
11: MUX3

3.17.6 RXMUX

Full name: Receive Frame Control Register

Address: FFCA

Default: xxxx 0011

Access: Read/Write

RXMUX controls the Multiplex mode of the receiver and selects the SYNC or CHM pattern for the receive SYN channel.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				SYNTOL	RX SYN SELECT	RX MUX	

Bits 7–4 Reserved

Bit 3 SYN Channel Error Tolerance Enable

0: Accept a SYN channel pattern only if all 24 bits are correct.
1: Accept a SYN channel pattern if at least 23 of 24 bits are correct.

The error tolerance function is intended to improve initial frame timing recovery in noisy or intermittent transmissions. No SYN channel error will be reported if the pattern is accepted.

Bit 2 Receive SYN Channel Pattern Select

0: CHMP or CHMF, depending on the DEVMODE register
1: SYNCF or SYNCP, depending on the DEVMODE register

Bits 1–0 Receive Multiplex Selection

The formatter is cleared if RXMUX and TXMUX are both programmed for MUX3.

00: MUX1.2
01: MUX1.4
10: MUX2
11: MUX3

3.17.7 TXDISAB

Full name: Transmit Disable Register

Address: FFCB

Default: xxxx xx01

Access: Write Only

TXDISAB aborts a transmission or disables the transmitter, but does not clear frame synchronization.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						TX ABORT	TX DISABLE

Bits 7–2 Reserved

Bit 1 Transmit Abort

0: Default (transmission not aborted)
1: Immediately stop transmission at the end of the current frame, regardless of bit 0.

Note: *Writing 03H also causes an immediate disable and 00H restarts transmission.*

Bit 0 Transmit Disable

Transmission will start when data is loaded in the transmit buffer AND this bit is cleared. Setting this bit disables the transmission at the end of the current transmit code word if data is still present in the transmit buffer. If the transmit buffer is empty, transmission stops at the end of the current frame. If the bit is set and then cleared prior to the end of a transmission, the write is ignored and transmission is not terminated.

0: Enable transmission
1: Disable transmission at the end of the code word

3.17.8 SYNCDC

Full name: Sync D Control Register

Address: FFCC

Default: xxxx xxx0

Access: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							SYNCD CONTROL

Bits 7–1 Reserved

Bit 0 SYNCD Control

SYNCDC controls insertion of the SYNCD pattern. The control bit is ignored if double buffering is enabled in DEVMODE[6].

0: The SYNCD pattern is not inserted prior to the next code word transmission.
1: The SYNCD pattern is inserted in the D channel before the next transmit code word, indicating the beginning of a new packet.

3.17.9 RDATAC

Full name: Receive D Channel Data Control Register

Address: FFCD

Default: N/A

Access: Write Only

RDATAC is a command (address decode) with no associated data field that locates the beginning of the next receive D Channel packet by seeking the SYNCD pattern. Once software writes RDATAC, all D channel data is ignored by hardware until the SYNCD pattern is received, after which time the D channel code word will be loaded into the receive buffer RXBUF0–5.

Software must issue the RDATAC command to initiate D channel reception. It must also be issued to locate the beginning of each new D channel packet. If double buffering is enabled, RDATAC is issued automatically by hardware if the packet is received without error. Under error conditions, software is responsible for issuing the command. If single buffering is used, software is always responsible for determining whether to issue RDATAC after each received code word.

3.17.10 TPOWER

Full name: Transmit Power Control Register

Address: FFCE

Default: 00xx xxx0

Access: Read/Write

TPOWER controls the TXPWR and ALE pins.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXPWR MODE		Reserved					

Bits 7–6 TXPWR Pin Mode Selection

- 00: TXPWR goes High and stays High after the transmit portion of the current Formatter frame.
- 01: TXPWR is High during the transmit portion of the frame and Low during the receive portion, with timing the same as that of the TXEN pin.
- 1x: TXPWR goes Low and stays Low after the end of the transmit portion of the current Formatter frame.

Bits 5–0 Reserved

3.17.11 BVALID

Full name: B Channel Valid Register

Address: FFCF

Default: 0xxx xxxx

Access: Read/Write

BVALID enables the B channel.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B CH ON/OFF	Reserved						

Bit 7 B Channel On/Off

0: Transmit and receive paths between the B channel and the 32 kbit/s ADPCM data stream at the B Channel Multiplexer are disabled. The B Channel Multiplexer output goes to zero in both the transmit (to radio link) and receive (from radio link) directions.

1: Transmit and receive B channel paths are enabled, that is, the B channel is connected to the 32 kbit/s ADPCM stream of the B Channel Multiplexer. There is a restriction that MECTR1[4] be enabled at least 1.25 ms before this bit is asserted to guarantee that embedded FIFO storage is appropriately loaded for operation.

Bits 6–0 Reserved

3.17.12 SYNCTR

Full name: Frame Sync Control Command

Address: FFD0

Default: N/A

Access: Write Only

SYNCTR is a command (address decode) with no associated data field. Writing SYNCTR causes the frame synchronization to be cleared.

If synchronization has not been achieved, writing SYNCTR immediately clears any state machines attempting to synchronize to the SYN channel.

If synchronization has already been achieved, it will be cleared at the end of the transmit portion of the current Formatter frame, approximately 14 µs before the next rising edge of the RXEN pin.

Note: *When resynchronizing during a transmission, TXDISAB must be written before SYNCTR in order to disable transmission cleanly. Otherwise, unexpected transmit frame timing may result.*

3.17.13 DMONIT

Full name: D Channel Monitor Control Register

Address: FFD1

Default: xxxx xx00

Access: Read/Write

DMONIT defines the test mode configuration applicable when the BDMUX register is programmed for D channel input/output (BDMUX[6:5]=10).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						TX D CH I/O MODE	MONITOR MODE

Bits 7–2 Reserved

Bit 1 TX D Channel Data I/O Selection

- 0: The DTXDATAIO signal on the BDP1_OUT3 multifunction pin is an output and is a copy of what is being transmitted on the radio link.
- 1: The DTXDATAIO signal on the BDP1_OUT3 multifunction pin is an input, which will be transmitted on the radio link.

Bit 0 Monitor Mode

- 0: The DTXDATAIO signal on BDP1_OUT3 includes only D channel data. The DRXDATA signal on BDP0_OUT2 is an output that includes only D channel data.
- 1: The DTXDATAIO signal includes D channel, B channel, and SYN channel (except for preamble) data. The DRXDATA signal is an output, which includes D, B, and SYN channel data (except for preamble).

3.17.14 DTXCTR

Full name: D Channel Transmit Control Register

Address: FFD2

Default: xxxx xx00

Access: Read/Write

DTXCTR specifies when the D channel transmit buffer empty interrupt is generated as well as specifying a Continuous D Channel Transmit mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						TX BUFFER EMPTY CONTROL	CONTIN TX

Bits 7–2 Reserved

Bit 1 D Channel Transmit Buffer Empty Interrupt Control

0: The transmit buffer empty (or half-empty) interrupt is generated when the last byte of the code word is loaded from the buffer into a serializing shift register.

1: The transmit buffer empty interrupt is generated when the last bit of the code word (i.e., the parity bit) is transmitted.

Bit 0 D Channel Continuous Transmit Mode Select

0: Normal mode. After the transmit buffer is empty, D channel bits are filled with the IDLE_D pattern until the next code word is initiated. Emptying the buffer causes the transmit buffer empty interrupt.

1: Continuous Transmission mode. Code words including the same 6 bytes of the transmit buffer are transmitted repeatedly. The transmit buffer empty interrupt is not generated. If the Transmit Multiplex mode is set to 2, then the 48-bit IDLE_D pattern is also transmitted between code words.

3.17.15 TDELAY

Full name: Transmit RF Delay Control

Address: FFD4

Default: 1000 1011

Access: Read/Write

TDELAY controls the timing of the TXEN RF control pin relative to data transmission. Refer to Figure 2-15 for definition of timing parameters.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TTD DELAY				TTL DELAY			

Bits 7–4 Programmed delay t_{TTD}. 868 ns ≤ t_{TTD} ≤ 32.1 µs in 3.47 µs increments.

Default = 4.3 µs. Unspecified codes are invalid.

Bits 7 6 5 4	Delay
0 0 0 0	32.1 µs
0 0 0 1	28.6 µs
0 0 1 0	25.2 µs
0 0 1 1	21.7 µs
0 1 0 0	18.2 µs
0 1 0 1	14.8 µs
0 1 1 0	11.3 µs
0 1 1 1	7.8 µs
1 0 0 0	4.3 µs
1 0 0 1	0.87 µs

Bits 3–0 Programmed delay $t_{TTL.}$ 4.3 µs ≤ t_{TTL} ≤ 46 µs in 3.47 µs increments.

Default = 42.5 µs. Unspecified codes are not valid.

Bits 3 2 1 0	Delay
0 0 0 0	4.3 µs
0 0 0 1	7.8 µs
0 0 1 0	11.3 µs
0 0 1 1	14.8 µs
0 1 0 0	18.2 µs
0 1 0 1	21.7 µs
0 1 1 0	25.2 µs
0 1 1 1	28.6 µs
1 0 0 0	32.1 µs
1 0 0 1	35.6 µs
1 0 1 0	39.0 µs
1 0 1 1	42.5 µs
1 1 0 0	46.0 µs

3.17.16 RDELAY

Full name: Receive RF Timing Control

Address: FFD5

Default: 0000 1011

Access: Read/Write

RDELAY controls the timing of the RXEN RF control pin relative to data reception and configures the XINT2 pin to provide the ANTSW output timing signal. Refer to Figure 2-15 for definition of timing parameters.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLICER PIN ENABLE	ANTSW/ XINT2 SEL	FORCERXEN	TRH DELAY				

Bit 7 Slicer Control

0: OUT10 pin operates as standard I/O
1: Enables OUT10 pin for external slicer control

Bit 6 ANTSW/XINT2 Select

0: XINT2 pin performs XINT2 input function.
1: XINT2 pin performs ANTSW output function.

Bit 5 Force RXEN pin High, regardless of the activity state of the Digital Formatter. Allows receive-level scanning without activating the Digital Formatter.

0: Default operation of RXEN
1: Force RXEN High

Bits 4–0 Programmed delay t_{TRH}. 11.3 µs ≤ t_{TRH} ≤ 87.6 µs in 3.47 µs increments. Default = 49.5 µs. Unspecified codes are invalid.

Bits 4 3 2 1 0	Delay (µs)
0 0 0 0 0	11.3
0 0 0 0 1	14.8
0 0 0 1 0	18.2
0 0 0 1 1	21.7
0 0 1 0 0	25.2
0 0 1 0 1	28.6
0 0 1 1 0	32.1
0 0 1 1 1	35.6
0 1 0 0 0	39.0
0 1 0 0 1	42.5
0 1 0 1 0	46.0
0 1 0 1 1	49.5
0 1 1 0 0	52.9
0 1 1 0 1	56.4
0 1 1 1 0	59.9
0 1 1 1 1	63.4
1 0 0 0 0	66.8
1 0 0 0 1	70.3
1 0 0 1 0	73.8
1 0 0 1 1	77.2
1 0 1 0 0	80.7
1 0 1 0 1	84.2
1 0 1 1 0	87.6

3.17.17 RFINV

Full name: RF Polarity Control

Address: FFD8

Default: xxxx 0000

Access: Read/Write

RFINV is used to set the active polarity for the RF control signals TXEN, RXEN, SHCTR, and ANTSW.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				TXEN POLARITY CONTROL	RXEN POLARITY CONTROL	SHCTR POLARITY CONTROL	ANTSW POLARITY CONTROL

Bits 7–4 Reserved

Bit 3 TXEN Polarity Control

0: Normally Low; active High
1: Normally High, active Low

Bit 2 RXEN Polarity Control

0: Normally Low; active High
1: Normally High, active Low

Bit 1 SHCTR Polarity Control

0: Normally Low; active High
1: Normally High, active Low

Bit 0 ANTSW Polarity Control

0: Normally Low; active High
1: Normally High, active Low

3.17.18 RXFALL

Full name: RX Off, in Independent Timing Mode

Address: FFD9

Default: 0000 0000

Access: Read/Write

The Independent RX Timing mode, enabled in PLLCTRL[4], allows the RX timing to be established independently from the TX timing. This register is used to program the fixed time relationship between the falling edge of RXEN and the first bit in the transmitted frame. RXFALL, combined with TDELAY, produces a fixed relationship between the falling edge of RXEN and the rising edge of TXEN.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				TRL			

Bits 7–4 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bits 3–0 TRL

Time from when RXEN falls to the first MUX1.4 TX bit; default = 54.7 µs.

Bits 3–0	Delay Time (t_{FBT})	Bits 3–0	Delay Time (t_{FBT})
0000	54.7 µs	1000	26.9 µs
0001	51.2 µs	1001	23.4 µs
0010	47.7 µs	1010	20.0 µs
0011	44.3 µs	1011	16.5 µs
0100	40.8 µs	1100	13.0 µs
0101	37.3 µs	1101	9.5 µs
0110	33.9 µs	1110	6.9 µs
0111	30.4 µs	1111	2.6 µs

3.17.19 PLLCTRL

Full name: Phase-Locked Loop Control Register

Address: FFDA

Default: 0000 0000

Access: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EN_LT	PLL MODE	EN_FADE DETECT	RX INDEP TIMING	SLOW TAU		FAST TAU	

Bit 7 Enable Long-Term Timing Recovery

This control bit applies to the CPP only; it is gated off in the CFP. The long-term timing recovery circuit measures the frequency offset between the remote CFP and the local crystal over a 64 ms period after initial synchronization of the link and continuously adds this offset to the PLL. This bit can be used in conjunction with the PLLHOLD bit in the RXTMGR register as detailed below.

0: Disable
1: Enable

EN_LT	PLLHOLD (RXTMGR Register)	Function
0	0	Track recovered clock
0	1	Hold PLL steady with respect to local crystal
1	0	Allow PLL to hold steady with measured receive frequency when fades are detected
1	1	Force PLL to hold steady with measured receive frequency regardless of detection fades

Bit 6 PLL Mode

Switch between previous generation edge-triggered PLL with fixed, time constant and new generation energy-triggered PLL with programmable time constants. When Energy Triggered mode is enabled, an additional one-half bit delay must be added to the MODDLY register value to compensate for the additional internal delay.

0: Edge-triggered, fixed time constant
1: Energy-triggered, programmable time constant

Bit 5 Enable Hardware Fade Detection and Response

This control bit enables hardware to respond to detected fades by halting evaluation of the data for PLL timing information. The JITCTR register contains the threshold used by the fade detection circuit to differentiate between a good signal and a fade.

0: Disable
1: Enable

Bit 4 RX Independent Timing

When set to Mode 0, the CFP receiver frame timing is locked to the transmitter frame timing. When set to Mode 1, the CFP receiver frame timing is allowed

to float with recovered clocks from the CPP, allowing greater tolerance for the temporary condition of CPP losing timing lock during a fade. This bit is a CFP-only bit unless FDD mode is selected. DEVMODE[3] is set, in which case this bit must be set to 1 for both CPP and CFP.

0: Fixed relationship to transmit frame
1: Receiver timing independent of TX frame

Bits 3–2 PLL Tracking Mode Loop Filter Constant

00: = 1/2 (fastest); response time constant τ = 13 µs
01: = 1/4; response time constant τ = 48 µs
10: = 1/12; response time constant τ = 104 µs
11: = 1/16 (slowest); response time constant τ = 159 µs

Bits 1–0 PLL Acquisition Mode Loop Filter Constant

00: = 1/4 (fastest); response time constant τ = 48 µs
01: = 1/12; response time constant τ = 159 µs
10: = 1/20; response time constant τ = 270 µs
11: = 1/28 (slowest); response time constant τ = 381 µs

3.17.20 MODTMG

Full name: Modem Timing Adjustment Register

Address: FFDD

Default: xxxx xx00

Access: Read/Write

MODTMG specifies whether delay is to be added to the transmit frame and initiates a delay measurement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						NO DELAY	MEASURE DELAY

Bits 7–2 Reserved

Bit 1 No Delay

0: The delay value in the MODDLY register determines the relative timing of the transmit and receive portions of the Formatter frame.
1: The transmit and receive portions of the Formatter frame are fixed as if the external RF delay were zero. That is, digital transmit and receive data signals at the chip meet the necessary antenna timing constraints.

Bit 0 Delay Measurement Command

Writing 1 initiates a modem delay measurement, which returns a value to the MODDLY register. Hardware clears the bit to indicate the end of the measurement. A software timer is recommended to time the measurement out in case of RF circuit failure.

0: No action (write); measurement complete (read)
1: Initiate measurement (write); measurement incomplete (read)

3.17.21 MODDLY

Full name: Modem Delay Register

Address: FFDE

Default: x000 0000

Access: Read/Write

MODDLY reports the measured delay (read) and programs the desired delay (write). The total delay value, in 72 kHz bit periods, is:

Total Delay = BIT DELAY + 1/16 • PHASE DELAY

The measured data can be read anytime after MEASURE DELAY (MODTMG[0]) is cleared after completion of a measurement, even after writing new values to this register. Reading the register always returns the measured value. Written values cannot be read. If MEASURE DELAY has never been set, the default value is returned.

Writes to this register should not take place while the MEASURE DELAY bit is set.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	PHASE DELAY				BIT DELAY		

Bit 7 Reserved

Bits 6–3 Phase Delay

These bits report in binary form the measured phase delay when read, and specify the desired phase delay when written. Each phase increment is 1/16th of one bit, or 868 ns.

Bits 2–0 Bit Delay

These bits report in binary form the measured bit delay when read, and specify the desired bit delay when written. Each increment represents a delay of one bit, or 13.89 µs.

Note: *The maximum modem delay value is* $6\frac{15}{16}$ *bits or 96 µs.*

3.17.22 DCHSTAT

Full name: D Channel Status Register

Address: FFE4

Default: 0000 0100

Access: Read Only

DCHSTAT reports the channel transceiver status. DCHSTAT bits have no individual mask bits, but appear in MISRC0[2:0] subject to mask bits MIMSK0[2:0].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					DTX EMPTY	DRX ERR	DRX FULL

The following definitions apply when DEVMODE[6]=0, Single Buffering

Bits 7–3 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 2 D Channel Transmit Buffer Empty. Note that the DTX EMPTY interrupt defaults to ACTIVE, and that it remains active until the buffer is filled. Therefore, software should mask the interrupt until after the buffer is written. This bit is cleared by writing to the transmit buffer, TXBUF0–TXBUF5.

0: The channel transmit buffer TXBUF is not empty.
1: TXBUF is empty (default). Empty is defined by the DTXCTR register, bit 1.

Bit 1 D Channel Receive CRC, Parity Error, or Overflow

This bit is cleared when the DCHSTAT register is read.

0: There is no CRC, parity, or overflow error.
1: A CRC, parity, or overflow error occurred in the D channel receiver

Bit 0 D Channel Receive Buffer Full

This bit is set when the buffer is full and cleared when RXBUF5 is read.

0: The receive buffer has not been filled since RXBUF5 was last read.
1: The D channel receive buffer, RXBUF0–RXBUF5, contains 6 bytes.

The following definitions apply when DEVMODE[6]=1, Double Buffering

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	DRX OVF	DTX UF	DTX HALF EMPTY	DRX FULL	DTX EMPTY	DRX ERR	DRX HALF FULL

Bit 7 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 6 RX Overflow Status (read only)

Active High if the D Channel Receive Buffer has overflowed, indicating possible erroneous buffer contents. This bit should be evaluated each time the receive buffer is read to validate buffer contents.

0: No overflow (default)
1: Overflow

Bit 5 TX Underflow (read only)

Active High if the D Channel Transmit Buffer has underflowed, indicating that the D channel may have been stuffed with IDLE_D bits. Cleared by reading the register. This bit should be evaluated each time the transmit buffer is loaded to validate the contents of the actual transmitted D channel stream.

0: No underflow (default)
1: Underflow

Bit 4 TX Buffer Half-Empty (read only)

Active High if the D Channel Transmit Buffer contains one code word or less, indicating that software should load another code word into the D channel buffer. Cleared when software loads the buffer.

0: Buffer contains two code words.
1: Transmit buffer half-full (i.e., contains one code word or less) (default)

Bit 3 RX Buffer Full (read only)

Active High if the D Channel Receive Buffer contains two code words (12 bytes), indicating that software should read a code word from the D channel buffer to avoid overflow. Cleared when software reads a code word from the buffer, RXBUF.

0: Buffer does not contain two code words (default)
1: Buffer full (i.e., contains two code words)

Bit 2 TX Buffer Empty (read only)

Active High if the D Channel Transmit Buffer contains no code words, indicating that software should load another code word into the D channel buffer to avoid underflow. Note that the DTX EMPTY interrupt defaults to ACTIVE, and that it remains active until the buffer is filled. Therefore, software should mask the interrupt until after the buffer is written. Cleared when software loads the buffer.

0: Buffer contains at least one code word.
1: Buffer empty (i.e., contains no data) (default)

Bit 1 RX Error (read only)

Active High if the D Channel Receive Buffer code word accessible by software contains a CRC or parity error. This bit should be evaluated before the actual buffer contents are read, because the act of reading one part of the double buffer switches the software access to the second part.

0: No parity or CRC error detected in the accessible code word (default)
1: Accessible code word in the receive buffer contains a parity or CRC error

Bit 0 RX Buffer Half-Full (read only)

Active High if the D Channel Receive Buffer contains at least one code word (6 bytes), indicating that software should read a code word from the D channel buffer. Cleared when software reads a code word from the buffer.

0: Buffer contains less than one code word (default)
1: Buffer half full (i.e., contains at least one code word)

3.17.23 CMSSRC

Full name: CHM/SYNC Interrupt Source Register

Address: FFE5

Default: 0000 0000

Access: Read Only

CMSSRC reports SYN channel interrupt sources. Bits are latched to 1 only when an interrupt event occurs while the associated mask bit in CMSMASK is set. All bits are cleared by reading the register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				SYNC ERR	SYNCD	SYNC	CHM

Bits 7–4 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 3 Sync Error

The SYNC ERROR interrupt occurs if the appropriate SYN channel pattern (SYNCF, SYNCP, CHMF, or CHMP), as determined by the DEVMODE and RXMUX registers, is not received at the expected time during the receive frame.

0: There has been no synchronization error or CMSMASK[3]=0.
1: The SYNC channel pattern was not received correctly and CMSMASK[3]=1.

Bit 2 Sync in D Channel

The SYNCD interrupt occurs when a SYNCD pattern is received in the D channel.

0: No SYNCD has been received or CMSMASK[2]=0.
1: A SYNCD pattern has been received and CMSMASK[2]=1.

Bit 1 SYNC

The SYNC interrupt occurs when the SYN channel receiver correctly receives either a SYNCF or a SYNCP pattern, depending on whether the device is programmed as a CFP or a CPP in the DEVMODE register.

0: No SYNC has been received or CMSMASK[1]=0.
1: A SYNC pattern has been received and CMSMASK[1]=1.

Bit 0 CHM

The CHM interrupt occurs when the SYN channel receiver correctly receives either a CHMF or a CHMP pattern, depending on whether the device is programmed as a CFP or a CPP in the DEVMODE register.

0: No CHM has been received or CMSMASK[0]=0.
1: A CHM pattern has been received and CMSMASK[0]=1.

3.17.24 CMSMASK

Full name: CHM/SYNC Mask Register

Address: FFE6

Default: xxxx 0000

Access: Read/Write

CMSMASK provides individual enables for each interrupt source in CMSSRC.

0: Disable interrupt
1: Enable interrupt

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				SYNC ERR	SYNCD	SYNC	CHM

Bits 7–4 Reserved

Bit 3 SYNC Error Interrupt Mask

Bit 2 SYNCD Interrupt Mask

Bit 1 SYNC Interrupt Mask

Bit 0 Channel Marker Interrupt Mask

3.18 INTERRUPT CONTROLLER

3.18.1 MISRC0

Full name: Main Interrupt Source Register 0

Address: FFE0

Default: 0000 0000

Access: Read Only

A 1 in any bit of MISRC0 causes an active (Low) level at the 8032 $\overline{\text{INT0}}$ input. Bits are individually enabled in MIMSK0.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		NOISE	EXTINT2	EXTINT1	DTX EMPTY	DRX ERR	DRX FULL

Bits 7–6 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 5 Noise Condition (Jitter, DSP Noise, 4-Zero Detect)

An error or noise condition interrupt is generated by the “or” of the following three mechanisms: JITTER, NOISE DETECTION, and 4-ZERO ADPCM DETECT. JITTER indicates that the noise suppression jitter detector has detected jitter in the radio link in excess of the threshold programmed in the JITCTR register. NOISE DETECTION is indicated in register NSCTR[6], and the 4-ZERO ADPCM DETECT interrupt is indicated in register NSCTR[4].

0: The JITTER, NOISE DETECTION, and 4-ZERO ADPCM DETECT interrupts are inactive or MIMSK0[5] = 0.
1: The JITTER, NOISE DETECTION, or 4-ZERO ADPCM DETECT interrupts are active and MIMSK0[5] = 1.

Bit 4 EXTINT2

External interrupt 2 is generated by a change of state of the XINT2 pin and is cleared by reading XISTAT2.

0: There is no EXTINT2 interrupt active or MIMSK0[4]=0.
1: The EXTINT2 interrupt is active and MIMSK0[4]=1.

Bit 3 EXTINT1

External interrupt 1 is generated by a change of state of the XINT1 pin and is cleared by reading XISTAT1.

0: There is no EXTINT1 interrupt active or MIMSK0[3]=0.
1: The EXTINT1 interrupt is active and MIMSK0[3]=1.

Bit 2 DTXEMPTY is the D channel transmit buffer empty status, DCHSTAT[2], subject to MIMSK0[2].

0: The D channel transmit buffer is full or MIMSK0[2]=0.
1: The D channel transmit buffer is empty (default) and MIMSK0[2]=1.

Bit 1 DRXERR is the D channel receive error status, DCHSTAT[1], subject to MIMSK0[1].

0: No D channel receive parity or CRC error has been detected or MIMSK0[1]=0.
1: A D channel receive error has been detected and MIMSK0[1]=1.

Bit 0 DRXFULL is the D channel receive buffer full status, DCHSTAT[0], subject to MIMSK0[0].

0: The D channel receive buffer, RXBUF0–RXBUF5, does not contain a complete code word or MIMSK0[0]=0.

1: RXBUF contains either one or two complete code words, as determined by DCHSTAT[3,1], and MIMSK0[0]=1. The receive buffer can contain two code words only if double buffering is enabled in DEVMODE[6].

3.18.2 MISRC1

Full name: Main Interrupt Source Register 1

Address: FFE1

Default: 0000 0000

Access: Read Only

A 1 in any bit of MISRC1 causes an active (Low) level at the 8032 $\overline{\text{INT1}}$ input. Bits are individually masked in MIMSK1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	P1 INT 2	P1 INT 1	P1 INT 0	CHM/ SYNC	SIO	KEY PAD	EXTINT0

Bit 7 Reserved

Bit 6 P1 INT 2

Port 1 Interrupt 2 is active when an interrupt at pins P1.7–P1.4 has occurred, enabled by P1MASK, and is cleared by reading P1SRC2.

0: No interrupts on pins P1.7–P1.4 have occurred or MIMSK1[6]=0.

1: An interrupt on pins P1.7–P1.4 has occurred and MIMSK1[6]=1.

Bit 5 P1 INT 1

Port 1 Interrupt 1 is active when an interrupt at pins P1.3 or P1.2 has occurred, enabled by P1MASK, and is cleared by reading P1SRC1.

0: No interrupts on pins P1.3 or P1.2 have occurred or MIMSK1[5]=0.

1: An interrupt on pins P1.3 or P1.2 has occurred and MIMSK1[5]=1.

Bit 4 P1 INT 0

Port 1 Interrupt 0 is active when an interrupt at pins P1.1 or P1.0 has occurred, enabled by P1MASK, and is cleared by reading P1SRC0.

0: No interrupts on pins P1.1 or P1.0 have occurred or MIMSK1[4]=0.

1: An interrupt on pins P1.1 or P1.0 has occurred and MIMSK1[4]=1.

Bit 3 CHM/SYNC

The channel marker/SYNC interrupt is active if any of the four interrupt sources reported in CMSSRC is true, subject to MIMSK1[3], and is cleared by reading CMSSRC.

0: No CMSSRC bit is set or MIMSK1[3]=0.
1: A CMSSRC bit is set and MIMSK1[3]=1.

Bit 2 SIO

The serial port interrupt is active when either of the two interrupt sources reported in SIOSRC is true, and is cleared when SIOSRC is read.

0: There is no serial port interrupt or MIMSK1[2]=0.
1: There is a serial port interrupt and MIMSK1[2]=1.

Bit 1 KEYPAD

The keypad interrupt occurs every time the keypad status changes, regardless of whether the key scanner is enabled or not in MECTR0[7]. The mask bit MIMSK1[1] is automatically bypassed during shutdown, so that keypad activity will always wake the chip out of Shutdown mode. The interrupt is cleared by reading KPSTAT.

0: There is no keypad interrupt or MIMSK1[1]=0.
1: There is a keypad interrupt and MIMSK1[1]=1.

Bit 0 EXTINT0

External interrupt 0 is generated by a change of state of the XINT0 pin and is cleared by reading XISTAT0.

0: There is no EXTINT0 interrupt active or MIMSK0[0]=0.
1: The EXTINT0 interrupt is active and MIMSK0[0]=1.

3.18.3 MIMSK0

Full name: Main Interrupt Mask Register 0

Address: FFE2

Default: x000 0000

Access: Read/Write

MIMSK0 provides individual enables for each interrupt source in MISRC0.
0: Disable interrupt
1: Enable interrupt

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		JITTER	EXTINT2	EXTINT1	DTX EMPTY	DRX ERR	DRX FULL

Bits 7–6 Reserved, unused. Reads return 0s, subject to change in future silicon revisions.

Bit 5 Jitter Interrupt Mask

Bit 4 External Interrupt 2 Mask

Bit 3 External Interrupt 1 Mask

Bit 2 D Channel Transmit Buffer Empty Interrupt Mask

Bit 1 D Channel Receive Error Interrupt Mask

Bit 0 D Channel Receive Buffer Full Interrupt Mask

3.18.4 MIMSK1

Full name: Main Interrupt Mask Register 1

Address: FFE3

Default: 0000 0000

Access: Read/Write

MIMSK1 provides individual enables for each interrupt source in MISRC1.
0: Disable interrupt
1: Enable interrupt

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	P1 INT 2	P1 INT 1	P1 INT 0	CHM/SYNC	SIO	KEY PAD	EXTINT0

Bit 7 Reserved

Bit 6 Port 1 Interrupt 2 Mask

Bit 5 Port 1 Interrupt 1 Mask

Bit 4 Port 1 Interrupt 0 Mask

Bit 3 CHM/SYNC Interrupt Mask

Bit 2 Serial Port Interrupt Mask

Bit 1 Keypad Interrupt Mask

Bypassed during shutdown; any keypad activity activates the 8032 $\overline{\text{INT1}}$ interrupt. After IC wake-up and MISRC1 is read, the mask returns to normal operation. Defeat mask bypass using hold function, enabled in UCCCTR[5].

Bit 0 External Interrupt 0 Mask

3.19 CLOCK GENERATOR (POWER MANAGEMENT)

3.19.1 UCCCTR

Full name: Shutdown/Microcontroller Clock Control Register

Address: FFE9

Default: 000x 0000

Access: Read/Write

UCCCTR controls the low-power Shutdown mode and the 8032 clock rate. Write access to UCCCTR is restricted by the UCCCP address decode protection mechanism, but UCCCTR read access is unrestricted.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHUT DOWN	AUTO SPEED UP	ENHOLD	Reserved	CLK DOUBLE	CPU CLK RATE		

Bit 7 Shutdown

Setting the SHUTDOWN bit starts a timer that places the chip in Shutdown mode in 3.56 ms (min) to 7.12 ms (max). Any unmasked interrupt ($\overline{INT0}$ or $\overline{INT1}$) aborts the sequence and clears the bit. The bit is automatically cleared when the device exits shutdown.

0: Disable shutdown sequence or halt shutdown sequence
1: Initiate shutdown sequence if none running or restart the sequence if already running.

Bit 6 Automatic Speed-up

Setting the CPU clock Automatic Speed-Up mode allows the CPU clock generator to increase the CPU clock rate to 9.216 MHz when any unmasked interrupt ($\overline{INT0}$ or $\overline{INT1}$) occurs.

0: Disable auto speed-up
1: Enable auto speed-up

Bit 5 Enable the hold function, allowing the XINT1 pin to be HOLD input.

0: Disable hold function
1: Enable hold function, driven by the HOLD signal on the XINT1 pin. Interrupt functionality of the XINT1 pin is unmodified

Bit 4 Reserved

Bit 3 CLK Double

Bypasses the divide by two in the clock generator for the microcontroller and, if set, CPUCLK RATE [2:0] are inoperative. Setting this bit causes the CPUCLK to operate at 18.432 MHz.

0: Does not bypass the divide by two
1: Bypasses the divide by two

Bits 2–0 CPU CLK RATE

Determines the rate of the 8032 clock, CPUCLK, which may be configured as an output on the $\overline{CS2}$_CPUCLK pin. Table 3-13 lists codes for CPUCLK rate. The bits are cleared by software or by the automatic speed-up mechanism.

Table 3-13 8051 CPUCLK Speed Codes

CLK Double	CPUCLK Rate 2 1 0	CPUCLK Rate
0	0 0 0	9.216 MHz
0	0 0 1	4.608 MHz
0	0 1 0	2.304 MHz
0	0 1 1	1.152 MHz
0	1 0 0	576 kHz
0	1 0 1	288 kHz
0	1 1 0	144 kHz
0	1 1 1	72 kHz
1	x x x	18.432 MHz

3.19.2 UCCCP

Full name: Shutdown/Microcontroller Clock Control Protection

Address: FFEA

Default: N/A

Access: Write Only

This write-only address decode is part of the mechanism to protect the shutdown/microcontroller clock control register (UCCCTR) against inadvertent writes. There is no data field associated with the UCCCP address.

Software must perform the following sequence of events consecutively, without interruption, to change the contents of UCCCTR.

1. Write arbitrary data to UCCCP
2. Write arbitrary data to UCCCTR
3. Write arbitrary data to UCCCP
4. Write desired immediate data to UCCCTR

If any other reads or writes occur during the sequence, the sequence is aborted. This implies that all loading of the UCCCTR must be done with data stored either as immediate data in program space or else stored in 8032 internal data space (e.g., auxiliary registers, internal 256 byte RAM, etc.).

3.19.3 MECTR0

Full name: Module Enable Control Register 0

Address: FFEB

Default: 0000 0x00

Access: Read/Write

MECTR0 enables power management functions within the chip. Each enable bit is gated with the Shutdown mode indicator so that all blocks are automatically disabled when the chip is in shutdown and restored to their programmed state after the chip wakes up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KEY SCAN ENABLE	CODEC ENABLE	REF POWER DOWN	SIO ENABLE	TONE RINGER ENABLE	Reserved	T0/T1 ENABLE	T0/T1 FORCE

Bit 7 Key Scanner Enable

0: Disable. The scanner continues to generate interrupts regardless of whether it is enabled, but the key value read from the KPSTAT register will not be correct.
1: Enable

Bit 6 Codec and DTMF Enable

0: Disable
1: Enable. Enable MECTR1[4] to provide frame timing.

Bit 5 Analog Reference Power Down

Disables the analog reference circuits, including audio I/O, RSSI, battery detector, and TXI/TXQ baseband output driver. This bit must remain cleared for any of these blocks to function. After clearing the bit, approximately 300 µs are required to stabilize the reference. The reference is automatically powered down when the device is in Shutdown mode, without affecting this bit.

0: Enable the analog reference when not in the Shutdown mode
1: Power down the analog reference

Bit 4 Serial Port Enable

0: Disable
1: Enable the synchronous serial port block using the SDIN, SDOUT, and SCLK pins. This bit must be set to use the serial port.

Bit 3 Tone Ringer Clock Enable

0: Disable
1: Enable

Bit 2 Reserved

Bit 1 T0/T1 ENABLE

8032 T0 and T1 signals (P3.5 and P3.4) are internally connected to a common 18 kHz clock, enabled by this bit.

0: Disable. T0 and T1 signals are held at a level determined by MECTR0[0].
1: Enable

Bit 0 T0/T1 FORCE (applicable only when MECTR0[1]=0)

0: 8032 T0 and T1 signals are held Low.
1: 8032 T0 and T1 signals are held High.

3.19.4 MECTR1

Full name: Module Enable Control Register 1

Address: FFEC

Default: xx00 00x0

Access: Read/Write

MECTR1 enables specific functions within the chip for power management reasons. Each enable bit is gated with the Shutdown mode indicator so that all blocks are automatically disabled when the chip is in Shutdown and restored to their programmed state after the chip wakes up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		TX MOD ENABLE	FIFO/ FRAME SYNC ENABLE	FORMAT ENABLE1	FORMAT ENABLE2	Reserved	RSSI ENABLE

Bits 7–6 Reserved

Bit 5 Transmit Modulator Enable

0: Disable
1: Enable

Bit 4 FIFO and Frame Sync Enable

0: Disable the FIFO, the 8 kHz codec frame sync that times the 32 kbit/s B channel port.
1: Enable the FIFO and the 8 kHz codec frame sync, CLK8K.

Bits 3–2 Digital Formatter Enables 1 and 2

00: Disable the Digital Formatter
11: Enable the Digital Formatter. Both bits must be set High to enable the formatter.

Bit 1 Reserved

Bit 0 RSSI Enable

0: Disable
1: Enable. Allow 300 µs for settling after the RSSI is enabled.

3.20 WATCHDOG TIMER

3.20.1 WDTKEY

Full name: Watchdog Timer Key Register

Address: FFEF

Default: N/A

Access: Write Only

WDTKEY must be accessed in a certain sequence at least once every 1.82 seconds, or the watchdog timer will generate a reset pulse, returning the chip to its default state. The key sequence is:

write WDTKEY = A5 hex
write WDTKEY = 5A hex

The sequence must be written *without interruption* in consecutive write cycles.

Do not write the key sequence within the first 120 ms after reset is released. Timing information drawn from the watchdog timer after reset initializes some analog circuits, and writing the key sequence during this period may interrupt this initialization.

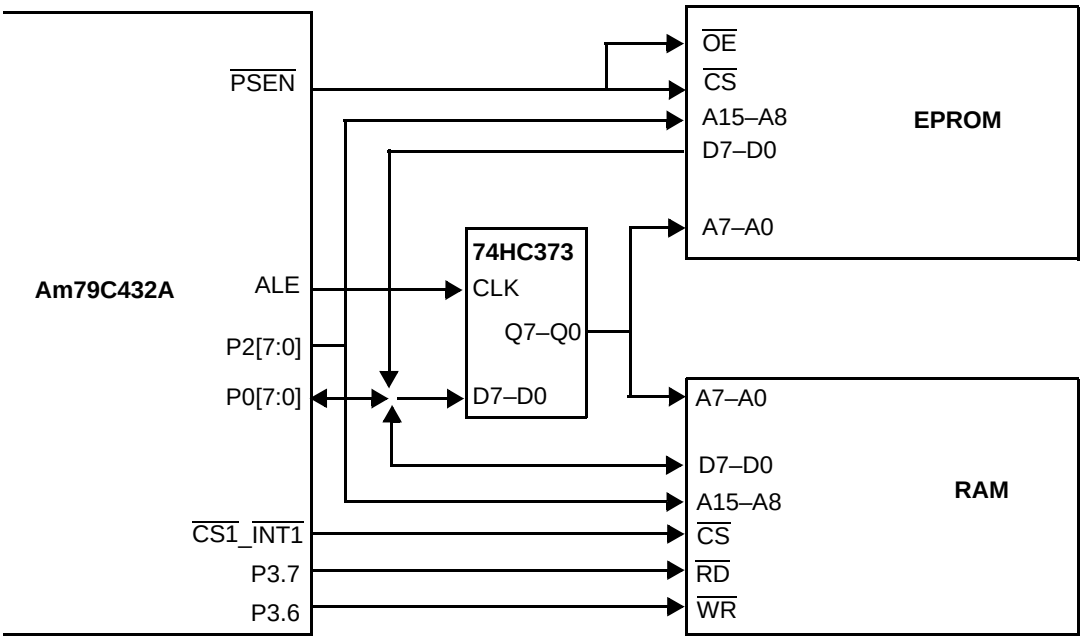
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTKEY							

CHAPTER

4 HARDWARE APPLICATIONS

4.1 ROM AND RAM INTERFACE

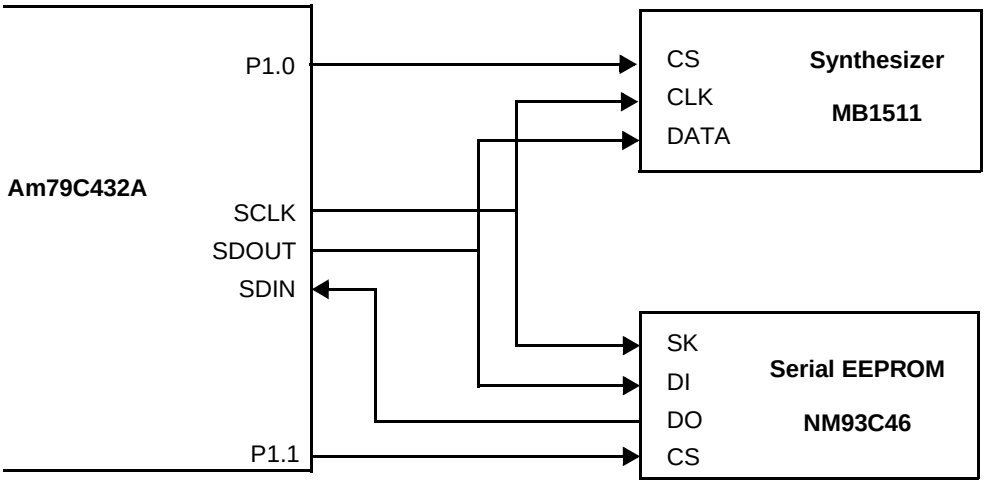
Figure 4-1 Interface to Program ROM and External Data RAM



4.2 EEPROM INTERFACE

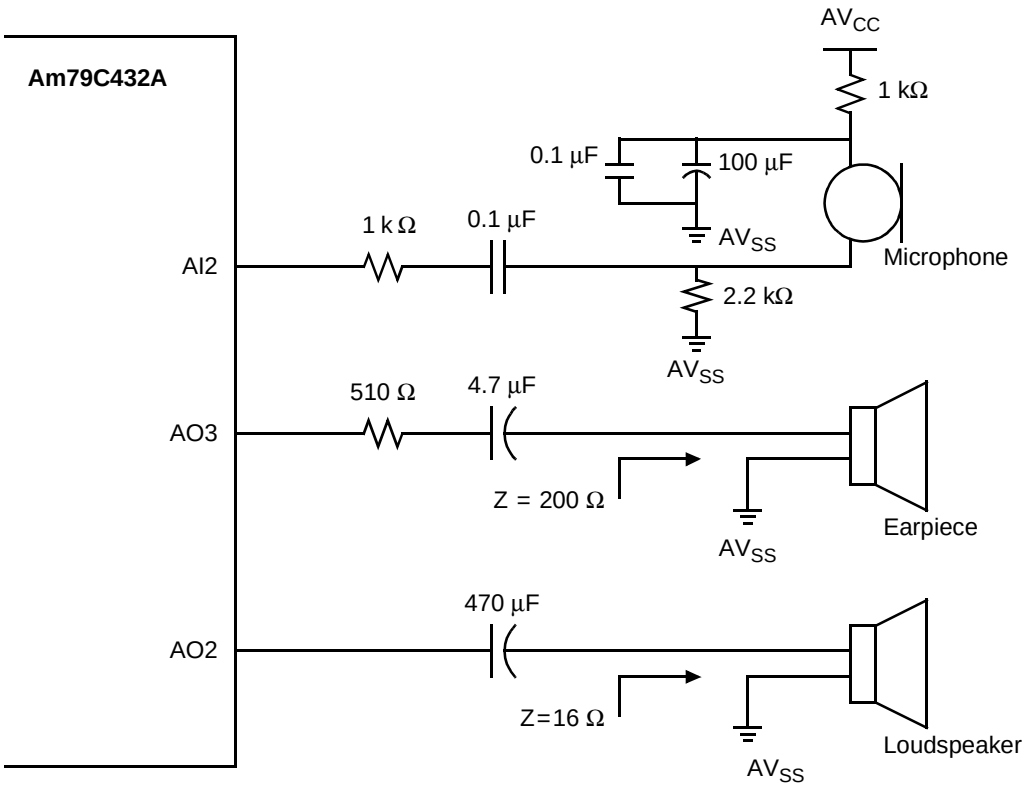
The synchronous serial interface can connect to several serial devices at once, provided the chip select signals of each are controlled by software. In the example of Figure 4-2, ports P1.0 and P1.1 are used as chip selects.

Figure 4-2 Interface to a Synthesizer and Serial Access EEPROM



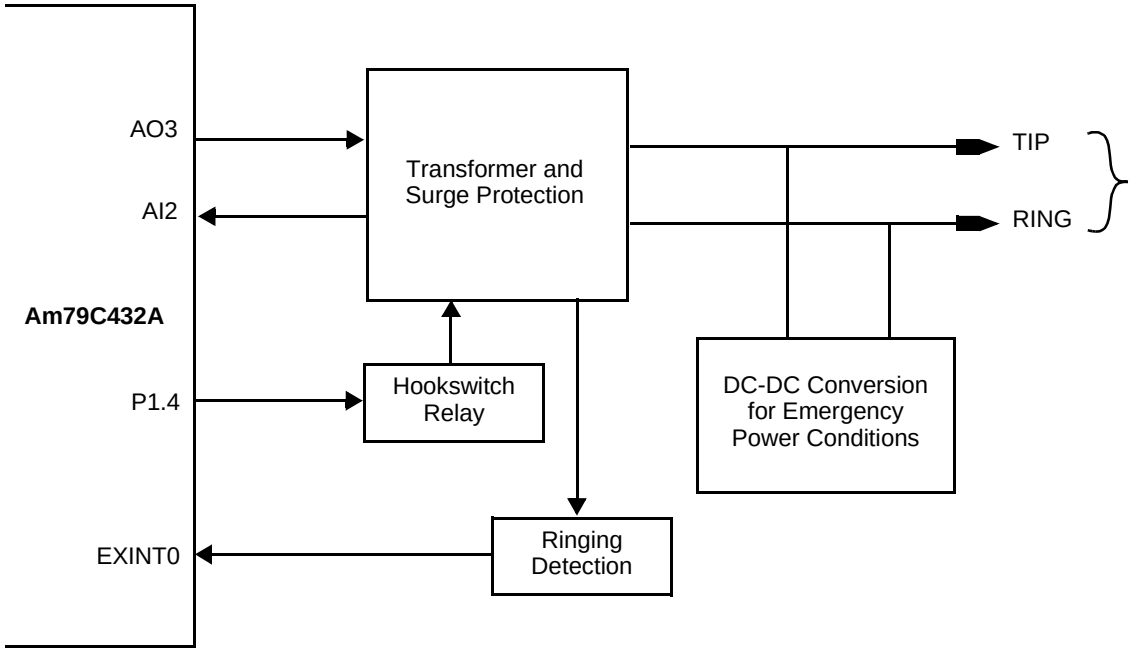
4.3 HANDSET AND LOUDSPEAKER INTERFACE

Figure 4-3 Interface to Handset and Loudspeaker



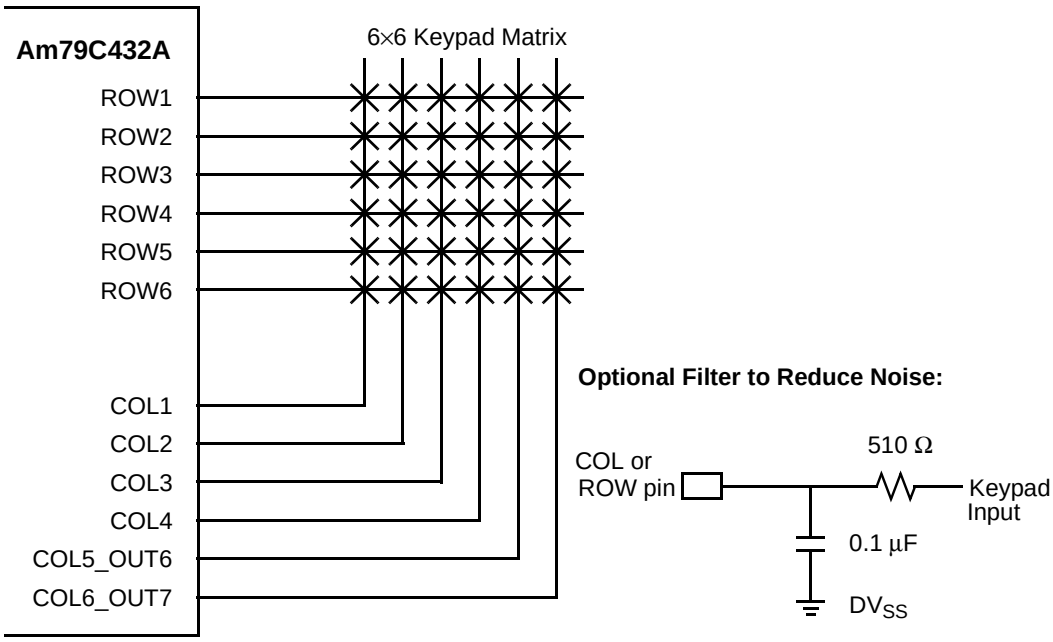
4.4 PSTN INTERFACE

Figure 4-4 Interface to Public Switched Telephone Network



4.5 KEY SCANNER INTERFACE

Figure 4-5 Interface to a 6 x 6 Keypad Matrix



4.6 BATTERY

The battery-level detector can be used to monitor the slow decline of main battery voltage in the handset. Software can poll the BATLEV register and send some warning to the user, such as a flashing LED, when the battery level falls below a programmed threshold. In this case, some sacrifice in battery life is made to guarantee that the chip is able to successfully provide the warning.

Once the main battery level falls below the 2.7 V operating voltage limit, the microprocessor is no longer able to poll the BATLEV register, and therefore cannot continue to provide any warning. Microcontroller behavior below 2.7 V is unpredictable, and as it begins to fail it may corrupt the Digital Formatter registers and static RAM (RAM1K). Likewise, since the Digital Formatter is not specified to operate below 2.7 V, it may change the radio interface signals unpredictably, causing spurious radio emissions. This condition may occur if the main battery is suddenly removed, for example, when it is being replaced.

In order to guarantee a well-behaved transition as the main battery falls below 2.7 V, an external power management device is recommended. This external device must accurately measure supply voltage and may assert an active Low HOLD signal on the XINT1 pin of the PhoX chip when the power supply falls below 2.7 V. When the hold function is enabled in UCCCTR[5], it has the desired effect of stopping all clocks within the PhoX chip, not only inhibiting spurious radio emission and protecting RAM contents, but also stopping further drainage of the battery, so that the handset can continue in this very low-power, safe, inactive state for extended periods of time.

The battery-level detector can be used to avoid an external power management device. When the threshold is crossed, the software can cause a PhoX chip port externally connected to the XINT1 pin to drive a Low level on the HOLD signal, thereby stopping all activity until a hardware reset is applied to the device.

Many handsets use a regulated power supply, in which case monitoring the Vcc pin would not reflect the actual declining battery voltage, but the regulated voltage instead. A scaled version of the unregulated voltage can be input into pin ROW1 if appropriately configured.

CHAPTER

5 SOFTWARE APPLICATIONS

5.1 SHUTDOWN MODE

Shutdown mode disables all synchronous and analog circuits to minimize power consumption in order to extend handset battery life. To use this mode, perform the following steps:

1. Set the Shutdown mode by programming UCCCTR[7] to 1.
2. Place the microcontroller in Idle mode by programming PCON[0] to 1 within 3.56 ms of programming UCCCTR[7].

Some optional actions may make system behavior more predictable. The following optional operations should be done either before setting the Shutdown mode bit or between setting the shutdown bit and programming the microcontroller for Idle mode:

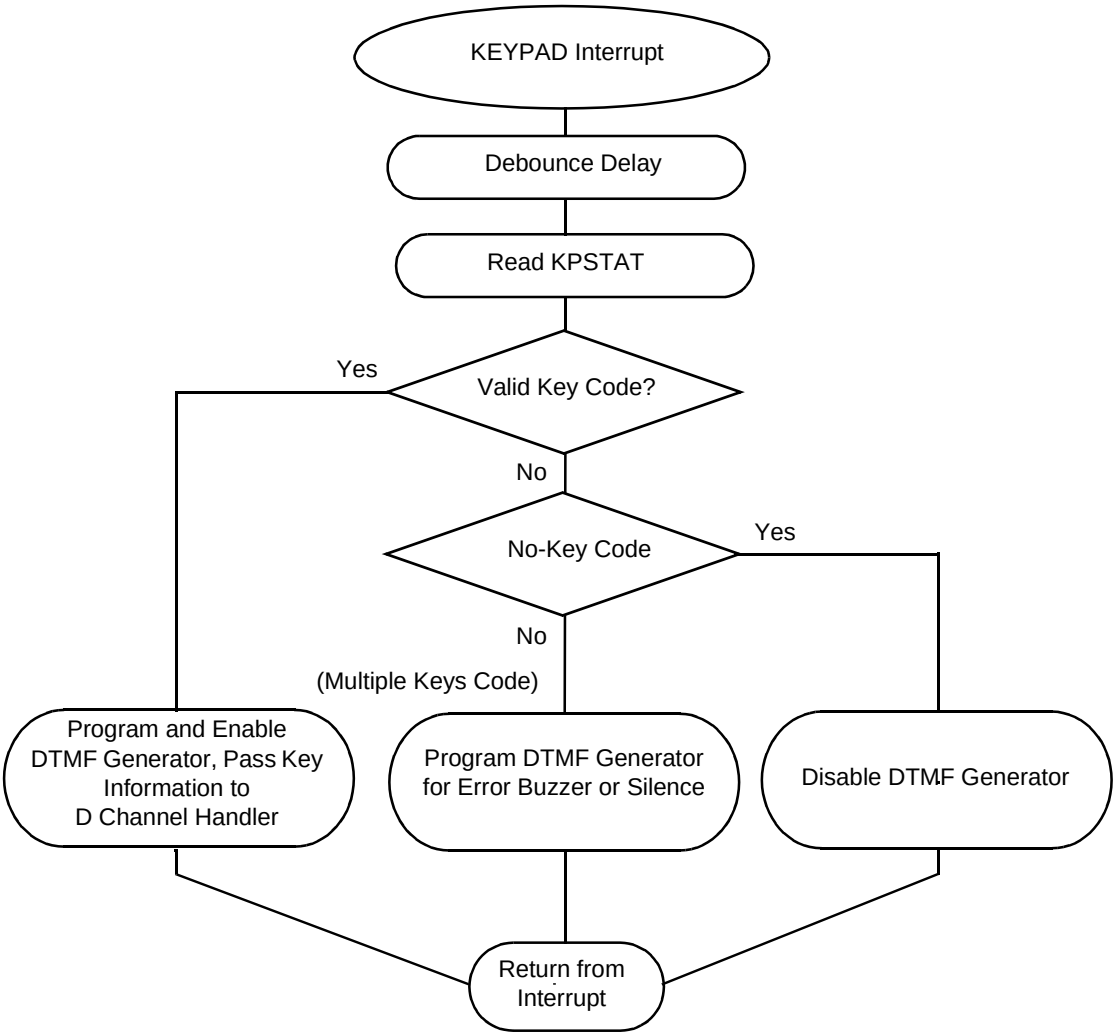
- Disable all blocks by clearing registers MECTR0 and MECTR1.
- Program the microcontroller auto speed-up feature in UCCCTR[6].
- Program the main interrupt masks, MIMSK0 and MIMSK1.
- Service the watchdog timer.

Any interrupt causes the chip to awaken from Shutdown mode and the microcontroller to exit Idle mode. The key scanner interrupt is automatically enabled during shutdown regardless of the MIMSK0 and MIMSK1 mask registers.

5.2 KEY SCANNER OPERATION

The key scanner requires software debouncing. Figure 5-1 shows an example flowchart.

Figure 5-1 Example Key Scanner Flow Diagram



5.3 DIGITAL FORMATTER PROGRAMMING HINTS

To program the Formatter, perform the following steps:

1. Enable the Digital Formatter in MECTR1 by setting MECTR1[3:2] = 11.
2. Program for CFP or CPP by setting DEVMODE.
3. If the device is a CPP, enable timing recovery by setting RXTMG = 0x01.
4. Program the modem delay, if applicable.
5. Release receiver synchronization by writing the SYNCTR command.
6. Disable the transmitter by setting TXDISAB = 0x01.
7. Set the SYNCD pattern by setting SYNCDC = 0x01.
8. Ignore D channel receive until SYNCD is received, then write the RDATAC command.
9. Disable B channel by setting BVALID = 0x00.
10. Program other Digital Formatter registers as necessary.
11. Enable interrupts.
12. Program transmission/reception multiplex by setting TXMUX and RXMUX.

5.3.1 SYNCD Register

If using single buffering, always be sure to write the SYNCDC register to the desired state before loading the transmit buffer.

5.3.2 Transmitting MUX2 or MUX3

To transmit MUX2 or MUX3, the TXDISAB and SYNCTR addresses, if written, have to be written after loading the TXBUF buffer; the other registers need to be written before loading the transmit buffer registers.

5.4 T0 AND T1 TIMER/COUNTERS

Bit 1 of MECTR0 enables the common 18 kHz signal, which is routed to both the T0 and T1 inputs of the microcontroller. The timer/counter circuits in the 8032 must be programmed as event counters in order to recognize the 18 kHz signal. There are also limitations on how slow the 8032 clock rate can be before the event counters fail to correctly count T0 and T1 transitions. Clock rates below 576 kHz do not accurately count the T0 and T1 timer/counter inputs because the sampling rate is too low.

Note that timer interrupts do not activate the PhoX controller auto speed-up feature; therefore, the time to service the interrupt depends on the microcontroller clock speed.

5.5 P1 INTERRUPTS

Interrupts caused by transitions of the P1 port pins are grouped into three interrupt sources. In general, the P1 port is used for input and output. If the inputs and outputs are arranged such that only one P1 input exists per P1 interrupt source register (P1SRC0, P1SRC1, P1SRC2), then locating the cause of the interrupt is simplified because the P1 source register need not be examined.

It is possible to cause a false interrupt indication without the P1 input actually changing if the P1TRIG register is changed while the interrupt is unmasked. Therefore, the interrupt should be masked while the P1TRIG is written.

5.6 SERIAL PORT SERVICE

SIOWR and SIORD are service routines for writing to and reading from the EXEL Microelectronics 93C46 serial EEPROM. The example drives the 93C46 active High chip select from port P1.1. The EEPROM device has a 16 bit data field and a 6 bit address field. It requires a start bit, an opcode, and a dummy bit during transmission. It has active High clocks and read data should be sampled on the positive-going clock edge.

```
; ###############################################################

MAIN:

; Write to and read from the 93C46 Serial EEPROM device

      acall    INIT     ; initialize the serial port registers

; Write the 16-bit value 0123 to address 1A.

      setb     P1.1     ; set active high chip select

      mov      R1, #03H ; R1 holds the transmit length argument, 3 in
                        ; this example

      mov      R2, #05H ; R2 holds the data argument
                        ; 1 0 1 = start bit + 01 ("write" op code)

      acall    SIOWR    ; send the start bit plus the two-bit write
                        ; op-code

      mov      R1, #06H ; length = 6 bits

      mov      R2, #1AH ; address to be sent= 1AH = 01 1010 binary

      acall    SIOWR    ; send the 6-bit address field, address = 1A.

      mov      R1, #00H ; length = 8 bits

      mov      R2, #01H ; data to be sent = 01H

      acall    SIOWR    ; send the most significant data byte, data = 01

      mov      R1, #00H ; length = 8 bits

      mov      R2, #23H ; data to be sent = 23H

      acall    SIOWR    ; send the least significant data byte, data = 23

      clr      P1.1     ; clear the active high 93C46 chip select,
; finishing the write

; Read back the value written to address 1A

      setb     P1.1     ; set active high chip select

      mov      R1, #03H ; length = 3 bits

      mov      R2, #06H ; data to be sent is 1 1 0 = start bit + 10 (“read”
                        ; op code)

      acall    SIOWR    ; send the start bit plus the two-bit read op-code

      mov      R1, #06H ; length = 6 bits

      mov      R2, #1AH ; Load EEPROM address argument, 1AH

      acall    SIOWR    ; send the 6-bit address field, address = 1A,
```

```
        mov     R1, #01H ; This device needs a "dummy" bit between transmit
        mov     R2, #00H ; and receive, so send 1 bit (data is actually a
                         ; don't-care)

        acall   SIORD    ; send the dummy bit and begin reception

                         ; Data returned in DATA1 and DATA2 RAM

                         ; locations

        clr     P1.1     ; clear the active high 93C46 chip select and end
                         ; the read

loop1:

        ajmp    loop1    ; infinite loop

; ###################################################################

INIT:

        clr     P1.1     ; disable the 93C46 chip select

        mov     DPTR, #MECTR0

        movx    A, @DPTR

        orl     A, #10H

        movx    A, @DPTR ; enable the serial port by asserting MECTR0[4]

        mov     DPTR, #MIMSK1

        movx    A, @DPTR

        orl     A, #04H

        movx    @DPTR, A ; enable serial port interrupt by asserting
                         ; MIMSK1[2]

        mov     DPTR, #SPTMG

        mov     A, #03H

        movx    @DPTR, A ; set serial port clock rate to 288 kHz in SPTMG

        RET

; ###################################################################

SIOWR:

; inputs: auxiliary register                R1 = Transmit length

;                                           R2 = Transmit data

        mov     dptr, #SIOMODE

        mov     A, #08H

        movx    @DPTR, A ; SIOMODE <- 08H. Mode = write only, active high
                         ; clocks

        mov     dptr, #SIOTBL

        mov     A, R1

        movx    @DPTR, A ; SIOTBL <- R1. Write transmit length register
```

```
      mov     dptr, #SIOTB
      mov     A, R2
      movx    @DPTR, A ; SIOTB <- R2. Write transmit data
      mov     dptr, #SIOMASK
      mov     A, #02H
      movx    @DPTR, A ; enable transmit buffer empty interrupt in
                       ; SIOMASK[1]
      clr     test.0
wait1:
      jnb     test.0, wait1; wait until transmit buffer is empty
      RET
; ###################################################################
SIORD:
;   inputs: auxiliary register      R1 = Transmit length
;                                   R2 = Transmit data
      mov     dptr, #SIOMODE
      mov     A, #0DH
      movx    @DPTR, A ; mode = active high clock, + edge receive,
                       ; 16-bit receive length, write-then-read
      mov     dptr, #SIOTBL
      mov     A, R1
      movx    @DPTR, A ; SIOTBL <- R1. Write transmit length register
      mov     dptr, #SIOTB
      mov     A, R2
      movx    @DPTR, A ; SIOTB <- R2. Write transmit data
      mov     dptr, #SIOMASK
      mov     A, #01H
      movx    @DPTR, A ; enable receive buffer full interrupt by setting
                       ; SIOMASK[0]
      clr     test.0
wait2:
      jnb     test.0, wait2; wait until receive buffer is full(1st byte)
      mov     A,#TEMP
      mov     #DATA1, A; store first received byte in RAM
      clr     test.0
```

```
wait3:
      jnb      test.0, wait3; wait until receive buffer is full (2nd byte)
      mov      A,#TEMP
      mov      #DATA2, A; store second received byte in RAM
      RET
; ###################################################################
ISR1:
; Interrupt Service Routine for INT1, assuming serial port is the only
; interrupt source
      mov      DPTR, #SIOSRC
      movx     A, @DPTR
      rrc      A
      jnc      TXINT    ; read SIOSRC to determine if interrupt is
                        ; from the transmitter or the receiver
      mov      DPTR, #SIORB
      mov      A, @DPTR ; Read receive buffer. Leave data in accumulator.
      mov      #TEMP, A ; temporary RAM storage of read data
TXINT:
      mov      dptr, #SIOMASK
      mov      A, #00H
      movx     @DPTR, A ; clear interrupt mask
      setb     test.0   ; terminate the wait loop
      RETI              ; return from interrupt
; ###################################################################
```

CHAPTER

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –65 to +150°C
Ambient Temperature with power applied . . . . . –40 to +85°C
Supply voltage to ground potential, continuous . . . . . 0 to 3.6 V
Lead Temperature (10 s hot-bar soldering) . . . . . 300°C
Lead Temperature (Reflow) . . . . . 107°C
Maximum power dissipation . . . . . 1.5 W
Voltage from any pin to Vss: . . . . . V_{SS} –0.3 V to V_{CC} +0.3 V
DC input/output fault current . . . . . 30 mA

Note: *Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

6.2 OPERATING RANGE

Operating Vcc range:
Referenced to Vss . . . . . 2.7 to 3.6 V

Ambient temperature:
Commercial (C) . . . . . 0 to +70°C

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

6.3 DIGITAL I/O DC CHARACTERISTICS

Table 6-1 is applicable over the operating range, unless otherwise specified, and applies to all pins except RSSI, TXI, TXQ, MREF, IREF, CFILT, AI2, AO2, AO3, and MCLK.

Table 6-1 Digital Pin DC Characteristics

Param	Parameter Description	Test Conditions	Min	Typ	Max	Unit
C_I	Pin input capacitance	Temp = 25°C, freq = 1 MHz		10		pF
C_O	Pin output capacitance	Temp = 25°C, freq = 1 MHz		15		
C_{L1}	Load capacitance (except TRI0_OUT10, TRI1)				40	
C_{L2}	Load capacitance, TRI0_OUT10, TRI1 pins				50	
I_{CC}	Supply current	V_{CC} = 3 V, shutdown standby [1] active [2]		0.036 4.05 8.06		mA
I_L	Input leakage, output high Z leakage	$V_{SS} < V_{IN} < V_{CC}$ $V_{SS} < V_{OUT}$ (high Z) < V_{CC}			±10	µA
I_{OH}[5]	Output current drive, driving 1 (Port 1)	V_{OH} = 2.4 V, V_{CC} = 3 V[3] V_{OH} = 2.6 V, V_{CC} = 3 V[3]	–42 –60			
I_{OH}[5]	Output current drive, driving 1 (except Port 1)	V_{OH} = 2.4 V, V_{CC} = 3 V[3] V_{OH} = 2.6 V, V_{CC} = 3 V[3]	–7 –5			mA
I_{OL}[5]	Output current drive, driving 0	V_{OL} = 0.4 V, V_{CC} = 3 V[3] V_{OL} = 0.7 V, V_{CC} = 3 V[3]	7 12			
R_{KO}	Keypad open circuit resistance, row to column pin		150			kΩ
R_{KS}	Keypad short circuit resistance, row to column pin				2	
R_{L1}	Resistance to V_{SS}/V_{CC} for logic 0/1 (TRI0_OUT10, TRI1)				50	Ω
R_{L2}	Leakage to V_{SS} or V_{CC} for logical mid-supply (TRI0_OUT10, TRI1)		250			kΩ
V_{IH}	Input high voltage		2.3V[4]		V_{CC}+0.3	V
V_{IL}	Input low voltage		–0.3		0.8 V	
V_{OH}	Output high voltage (except reset)	I_{OH} = –1 mA	2.4			
V_{OL}	Output low voltage	I_{OL} = 2 mA			0.5 V	

1. *MCLK driven at 12.8 MHz, microcontroller clock = 576 kHz, Digital Formatter, RSSI A/D, and key scanner on; all other modules off.*
2. *I/Q modulator, codec, handset I/O, Digital Formatter, key scanner, RSSI A/D modules on; microcontroller clock = 1.152 MHz, serial port on at 36 kHz clock rate.*
3. *These parameters apply to all digital outputs when they are actively driven. Microcontroller port 1 and 3 pins are actively driven High for two cycles of the CPUCLK, and then held High by a weak "keeper" transistor.*
4. *Does not apply to COL5_OUT6 and COL6_OUT7 (Keyscan/IOPad), which are designed with higher thresholds.*
5. *The test conditions represent V_{OH} and V_{OL} quiescent voltage levels for determining the I/O drive current. Transient conditions (on heavily loaded I/O) during normal operation cause some variation in the V_{OH} and V_{OL} levels. See V_{OH} and V_{OL} specifications below for maintaining logic levels across the operating ranges. These pins are not designed to source these current levels continuously.*

6.4 AUDIO CHARACTERISTICS

6.4.1 Audio Pin Characteristics

Table 6-2 Audio Analog Pin Characteristics

Applies to IREF, CFILT, AI2, AO2, AO3.

Param.	Parameter Description	Test Conditions	Min	Typ	Max	Unit
C_{CFILT}	External CFILT capacitance to AV_{SS}			11		µF
C_L	Load capacitance to AC ground				100	pF
I_L	High-Z output leakage (AO2, AO3)			< 10		µA
R_{IREF}	External IREF resistance (±1%) to AV_{SS}			62.5		kΩ
R_{L2}	Load resistance, AO2 to ground	Must be AC-coupled	13			W
R_{L3}	Load resistance, AO3 to ground	Must be AC-coupled	160			
V_{DC1}	Self-bias voltage (AI2)			0.5 • V_{CC}		V_{DC}
V_{DC2}	Self-bias voltage (AO2, AO3)			0.5 • V_{CC}		
V_{FSI}	Full scale input swing	AI2, AI2CTR gain = 3B		±0.36		V
V_{FSO2}	Full scale output swing (AO2, AO3)	$R_{L2} \geq 13\ \Omega$ $R_{L3} \geq 160\ \Omega$		±1.0		
Z_I	Input impedance (AI2)	I_{OL} = 5 mA	10			kΩ

6.4.2 dBm0 Reference-Level and Digital Full Scale

A 0 dBm0 digital signal level is nominally equivalent to a 0.25 Vrms tone. Digital full scale is +3.14 dBm0 for tones.

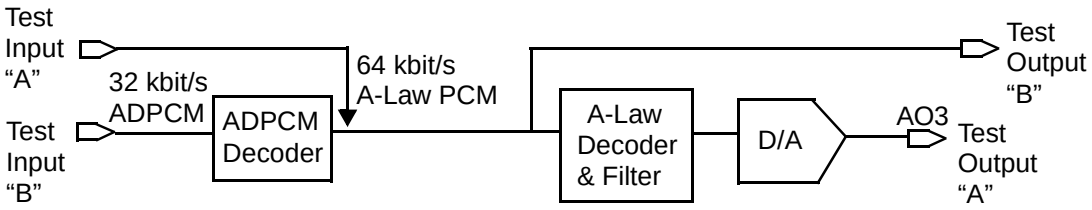
6.4.3 Audio Performance

The ADPCM transcoder is fully compliant with CCITT Recommendation G.721.

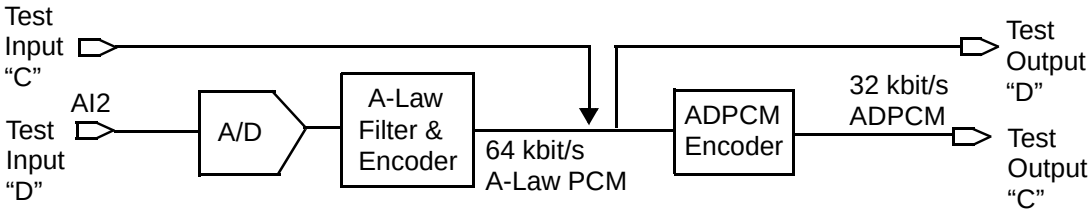
The codec is designed to meet CCITT Recommendation G.714 requirements for signal to distortion, gain tracking, frequency response, and idle channel noise specifications as defined in Table 6-3. Verification of conformance to G.714 is by device characterization. Production testing of individual parts includes only those parameters consistent with the testing requirements, shown in Table 6-4. Test paths A-A (Test Input A to Test Output A) and D-D of Figure 6-1 apply to the receive and transmit half-channel specifications (Table 6-3), respectively. Table 6-4 applies to both analog outputs of AO2 and AO3.

The half-channel parameters are specified in Table 6-3 for the transmit path from the AI2 audio input pin to an intermediate A-law test output (Test Output “D”) with +3 dB analog gain programmed. The parameters for the receive path from the codec A-law serial data input (Test Input “A”) to the AO3 audio output pin are specified for a 0 dB programmed analog attenuation. The parameters apply for A-law PCM conversion and assume psophometric filtering.

Figure 6-1 Audio Performance Test Paths



a. Receive Half-Channel Test Points



b. Transmit Half-Channel Test Points

Table 6-3 Transmit and Receive Half-Channel Transmission Characteristics

Parameter Description	Test Conditions	Min	Max	Unit
Frequency response (attenuation vs. frequency, relative to 1020 Hz)	–10 dBm0 input 50 Hz ≤ f ≤ 60 Hz (transmit only) ≤ 300 Hz 300 Hz < f ≤ 3 kHz 3 kHz < f ≤ 3.4 kHz 3.4 kHz < f ≤ 3.6 kHz 3.6 kHz < f ≤ 3.9 kHz 3.9 kHz < f < 4.0 kHz	 20 –0.25 –0.25 –0.25 –0.25 0.0 5.0	 0.25 0.90 	dB
Group delay vs. frequency	–10 dBm0 input 500 Hz ≤ f ≤ 600 Hz 600 Hz < f ≤ 1 kHz 1 kHz < f ≤ 2.6 kHz 2.6 kHz < f < 2.8 kHz		 750 380 130 750	µs
Gain Tracking, CCITT Method 2	1020 Hz input +3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	 –0.3 –0.6 –1.6	 0.3 0.6 1.6	dB
Signal to total distortion, CCITT Method 2	1020 Hz input 0 to –30 dBm0 –40 dBm0 –45 dBm0	 35 29 24		
Idle channel noise	Transmitter Receiver		–70 –75	dBm0p
Absolute gain tolerance	1020 Hz at 0 dBm0	–0.5	+0.5	dB
Transmitter out-of-band signal rejection, relative to 1 kHz	4.6 kHz at –25 dBm0 8.0 kHz at –25 dBm0	30 40		
Receiver spurious noise	0 dBm0, 300 Hz ≤ f ≤ 3.4 kHz		–35	dBm0p

Transmit half-channel programmable gain is 0 dB from AI2 Pin; receive half-channel programmable gain is 0 dB at the AO3 Pin. The 8032 processor has a 1.152 MHz clock rate.

Table 6-4 Audio Path Performance Specifications

Parameter Description	Test Conditions and Notes	Min	Max	Unit
Idle Channel Noise	Receive: ADPCM → AO3 Transmit: AI2 → ADPCM Audio mux (all analog): AI2 → AO2		–75 –70 –70	dB
Signal to total distortion, 1 kHz tone at –10 dBm0	Receive: ADPCM → AO3 Transmit: AI2 → ADPCM Audio mux (all analog): AI2 → AO3	35 35 35		
Absolute gain error, 1 kHz tone at –10 dBm0	Receive: ADPCM → AO3 Transmit: AI2 → ADPCM Audio mux (all analog), 0 dB: AI2 → AO3	–1 –1 — –1	+1 +1 — +1	
DTMF absolute gain error	DTMF generator→ analog AO3	–1	+1	
DTMF frequency deviation	DTMF generator→ analog AO3	–1	+1	%
DTMF signal to total distortion	DTMF generator→ AO3 Normal mode, 0 dB gain: DTMF-only mode: f < 1650 Hz f ≥ 1650 Hz	— 31 — 31 n/a		dB
Tone ringer absolute gain error	Tone ringer → AO2, AO3	–1	+1	

Test conditions: analog outputs AO2 and AO3 unloaded, 8032 processor running at 1.152 MHz clock rate.

6.5 RSSI CHARACTERISTICS

Table 6-5 applies to the RSSI pin. Inputs above the full scale V_{FS} read as full scale. Inputs below the minimum code input voltage V_{ZERO} read as the minimum input code.

Table 6-5 RSSI Characteristics

Param.	Parameter Description	Test Conditions	Min	Typ	Max	Unit
ERR_{LIN}	RSSI A/D integral linearity error				±1	LSB
T_{CONV}	RSSI A/D conversion time			10		µs
V_{FS}	RSSI maximum code input voltage	Transition voltage between codes 11110 and 11111	1.188	1.250	1.313	V
V_{ZERO}	RSSI minimum code input voltage	Transition voltage between codes 00000 and 00001	0.236	0.244	0.248	

6.6 I/Q MODULATOR CHARACTERISTICS

All spectral characteristics apply to TXI and TXQ outputs referenced to MREF and filtered by single-pole, passive, low-pass filters with 3 dB frequency of 100 kHz. All dBV values are based on the assumption that –9 dBV at TXI and TXQ yields +10 dBm at the final RF output. Adjacent channel power and spurious emissions are measured during constant transmission of pseudo-random data. Spectral values are characterized for the device and are not production tested on each individual part.

Table 6-6 I/Q Modulator Characteristics (Applies to TXI, TXQ, and MREF pins)

Param.	Parameter Description	Test Conditions	Min	Typ	Max	Unit
C_L	Load capacitance to AC ground				100	pF
P_{ADJ}	Adjacent channel power	Random data integrated over a ±40 kHz band			–39	dBV
R_L	Load resistance on TXI or TXQ		1			kΩ
R_{OZ}	Disabled state output impedance			25		
SE1	Spurious emissions	150 kHz ≤ freq ≤ 2 MHz 2 MHz < freq ≤ 10 MHz			–65 –79	dBV
T_{DLY}	Absolute delay from digital input to analog output			15.1		µs
ΔV_{DC1}	Differential offset between TXI and TXQ				40	mV
ΔV_{DC2}	Differential offset between MREF and TXI or TXQ				30	
V_{FS}	Full-scale AC output at TXI or TXQ	Digital data input is all 0s or all 1s		0.5		V_{AC}
V_{MREF}	MREF output voltage		0.475 • V_{CC}	0.5 • V_{CC}	0.525 • V_{CC}	V_{DC}
V_O	Output level at TXI or TXQ	Driving full scale sinusoid	–10	–9	–8	dBV
V_{OI}/ V_{OQ}	Relative levels of TXI and TXQ	Digital data input is all 0s or all 1s	–0.5		0.5	dB

6.7 NRZ OUTPUT CHARACTERISTICS

All specifications in Table 6-7 apply to the TXI and TXQ pins in NRZ mode referenced to MREF.

Table 6-7 NRZ Output Characteristics

Param.	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{MREF}	MREF output voltage		0.475 • V_{CC}	0.500 • V_{CC}	0.525 • V_{CC}	V_{DC}
V_{OH}	Output High level	Referenced to MREF	0.475	0.500	0.525	V
V_{OH}	Output Low level	Referenced to MREF	–0.475	–0.500	–0.525	

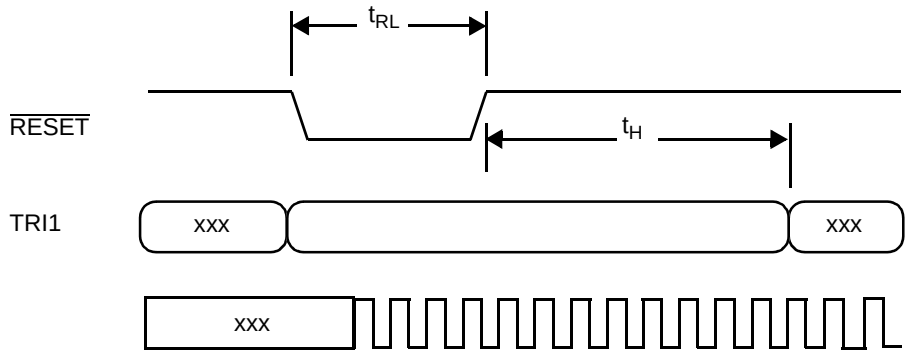
6.8 RESET

Table 6-8 refers to Figure 6-2. The parameter t_H assumes the active oscillation on the MCLK pin.

Table 6-8 Reset Timing

Parameter	Parameter Description	Min	Typ	Max	Unit
t_H	TRI1 holds after reset, in presence of MCLK clock	4.0			ms
t_{RL}	Reset pulse width (low): input output	100	 1.78		µs ms

Figure 6-2 Reset Timing



6.9 MICROCONTROLLER AND ADDRESS DECODER SWITCHING CHARACTERISTICS

Table 6-9 Am79C432A Microcontroller (80C32T2) and Address Decoder Switching Characteristics

All units are in nanoseconds unless otherwise specified.

No.	Param.	Parameter Description	Variable Clock Rate Min	Variable Clock Rate Max	9.216 MHz Min	9.216 MHz Max
t1	1/TCLCL	CPUCLK frequency	0 MHz	9.216 MHz		
t2	TLHLL	ALE pulse width	2TCLCL – 40		177	
t3	TAVLL	Address Valid to ALE Low	TCLCL – 55		53	
t4	TLLAX	Address hold after ALE low	TCLCL – 35		73	
t5	TLLIV	ALE Low to Valid Instruction In		4TCLCL – 100		334
t6	TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low†	TCLCL – 40		68	
t7	TPLPH	$\overline{\text{PSEN}}$ pulse width†	2TCLCL – 45		280	
t8	TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In†		3TCLCL – 105		220
t9	TPXIX	Input instruction hold after $\overline{\text{PSEN}}$	0		0	
t10	TPXIZ	Input instruction float after $\overline{\text{PSEN}}$		TCLCL – 25		83
t11	TAVIV	Address to valid instruction in		5TCLCL – 105		437
t12	TPLAZ	$\overline{\text{PSEN}}$ low to address float†		10		10
t13	TRLRH	$\overline{\text{RD}}$ pulse width	6TCLCL – 100		551	
t14	TWLWH	$\overline{\text{WR}}$ pulse width	6TCLCL – 100		551	
t15	TRLDV	$\overline{\text{RD}}$ low to valid data in		5TCLCL – 165		377
t16	TRHDX	Data hold after $\overline{\text{RD}}$	0		0	
t17	TRHDZ	Data float after $\overline{\text{RD}}$		2TCLCL – 70		147
t18	TLLDV	ALE low to Valid Data In		8TCLCL – 150		718
t19	TAVDV	Address to Valid Data In		9TCLCL – 165		811
t20	TLLWL	ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	3TCLCL – 50	3TCLCL + 50	275	375
t21	TAVWL	Address valid to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	4TCLCL – 130		304	
t22	TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	TCLCL – 60		48	
t23	TQVWH	Data Valid to $\overline{\text{WR}}$ high	7TCLCL – 150		609	
t24	TWHQX	Data hold after $\overline{\text{WR}}$	TCLCL – 50		58	
t25	TRLAZ	$\overline{\text{RD}}$ low to address Float		0		0
t26	TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	TCLCL – 40	TCLCL + 40	68	148
t27	TRWCS	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to $\overline{\text{CS}}$ High	TCLCL – 30	TCLCL + 10	78	118

† *Variable Clock Rate values apply to all CPUCLK rates other than 9.216 MHz. These parameters perform differently with slower clock rates due to power consumption considerations.*

Table 6-10 Am79C432A Emulation Mode Address Decoder Switching Characteristics

All units are in nanoseconds unless otherwise specified.

No.	Param.	Parameter Description	Min	Max
t2	TLHLL	ALE pulse width	30	
t3	TAVLL	Address Valid to ALE Low	30	
t4	TLLAX	Address hold after ALE low	10	
t13	TRLRH	RDL pulse width	230	
t14†	TWLWH	WRL pulse width	greater of 2TCLCL + 30 ns *or* 230 ns	
t15†	TRLDV	RDL low to Valid Data out		230
t16	TRHDX	Data hold after RDL	0	
t17	TRHDZ	Data afloat after RDL		50
t20	TLLWL	ALE low to RDL or WRL low	30	
t22	TQVWX	Data valid to WRL low	30	
t24	TWHQX	Data hold after WRL	30	
t25	TRLAZ	RDL low to Address float		0
t26	TWHLH	RDL or WRL high to ALE high	30	

† *t14 and t15 are clock dependent because the DSP synchronizes the read and write access to the 9.216 MHz DSP clock when it is enabled.*

Figure 6-3 Microcontroller External Program Memory Read Cycle

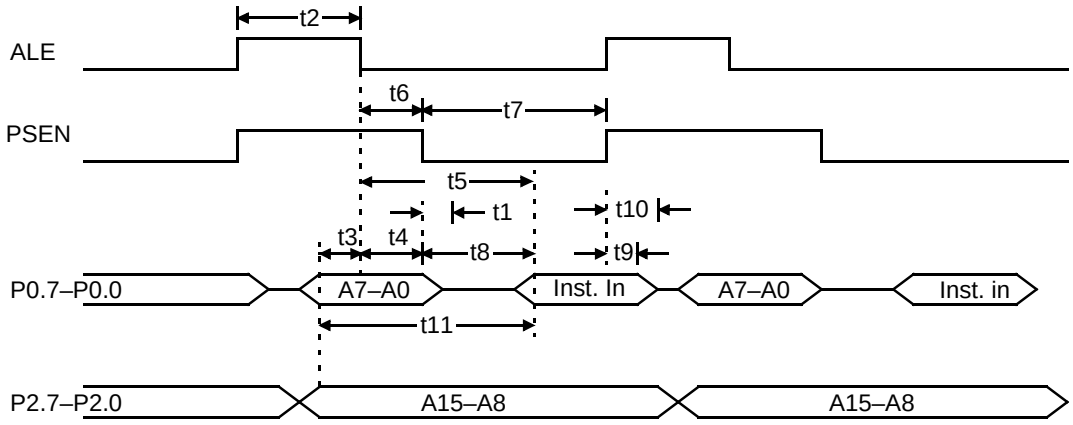


Figure 6-4 Microcontroller External Data Memory Write Cycle

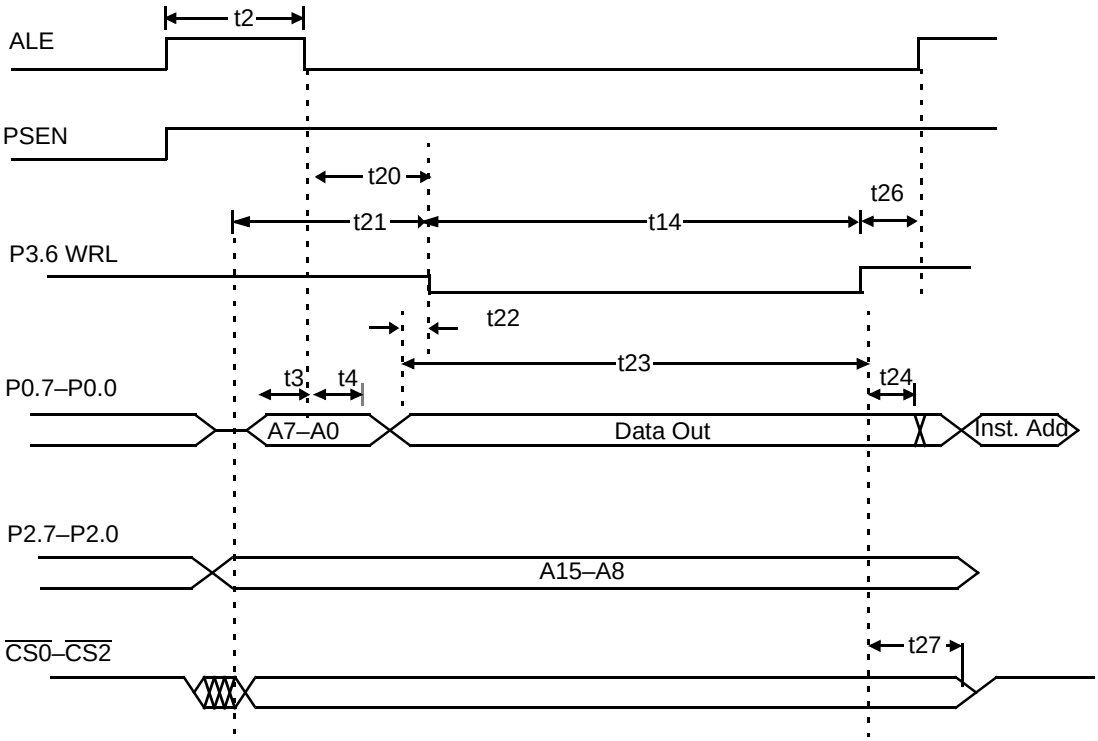
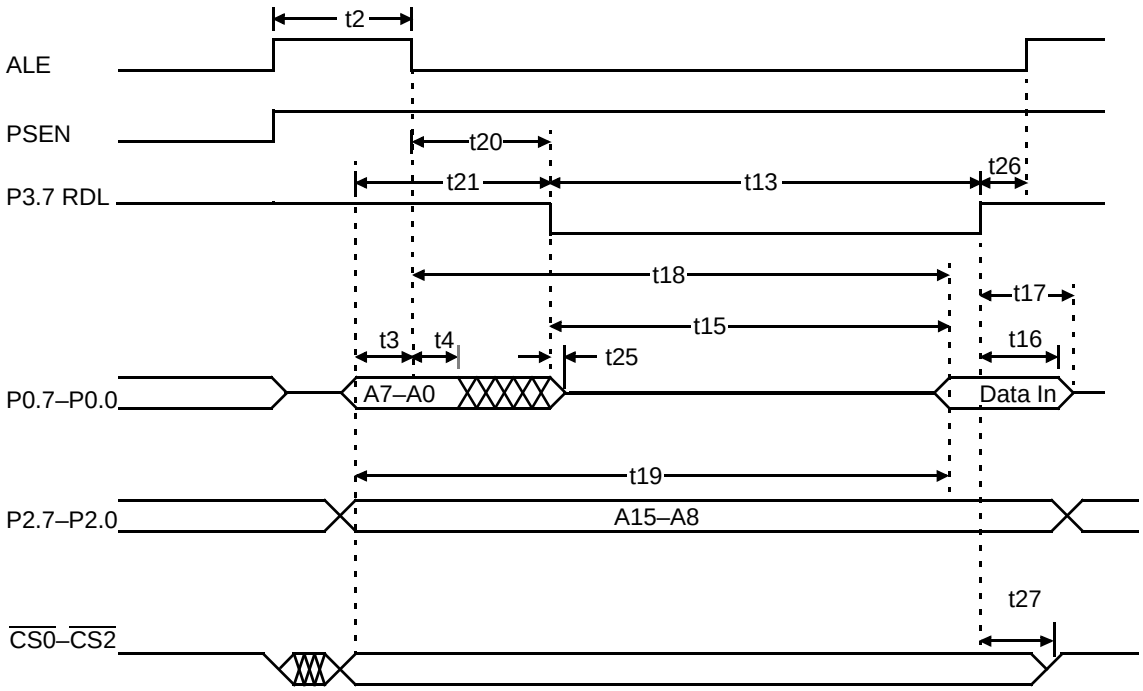


Figure 6-5 Microcontroller External Data Memory Read Cycle



6.10 DIGITAL FORMATTER SWITCHING CHARACTERISTICS

Figure 6-6 shows timing of the TXEN, RXEN, and SHCTR signals, relative to the receive and transmit data. Values are tabulated for the various multiplexes in Table 6-11. One bit period is nominally 13.89 µs (1/72 kHz).

Figure 6-6 RF Interface Control Signal Timing

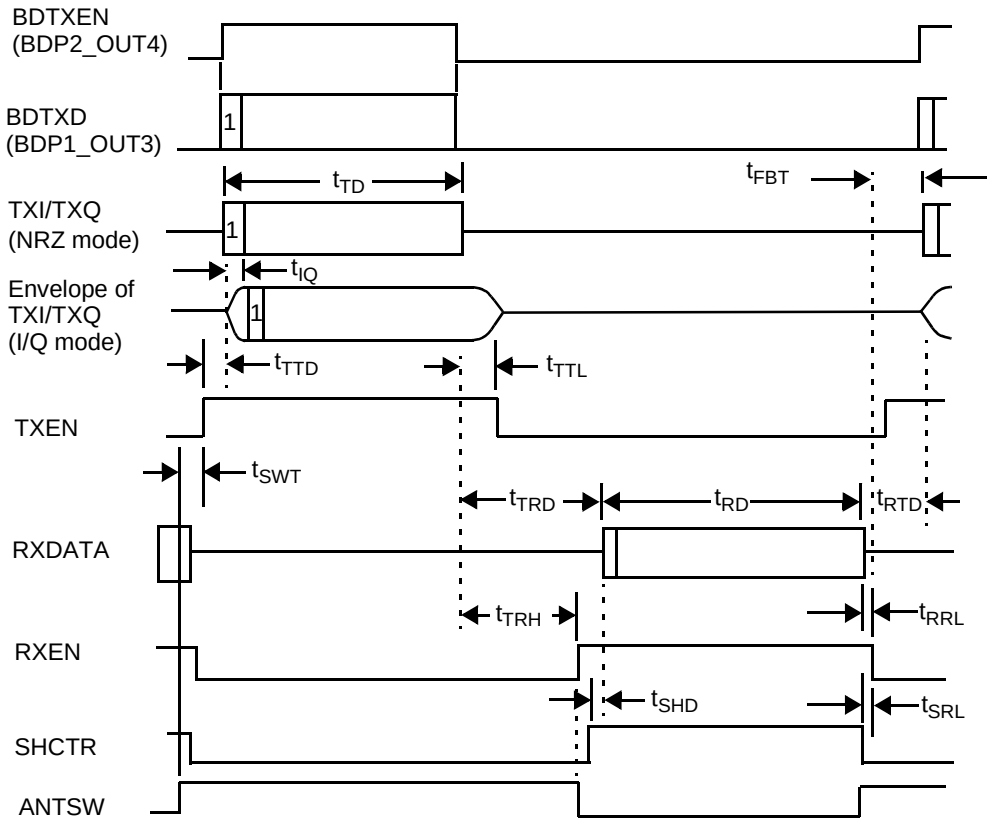


Table 6-11 RF Interface Control Signal Timing

All values are typical. (T_{MDM} = modem delay measurement adjustment)

Parameter	Description	MUX1.2, MUX 2	MUX1.4	MUX3
t_{IQD}	I/Q modulation delay	15.1 µs	15.1 µs	15.1 µs
t_{RD}	Receive data length	66 bits	68 bits	CPP: 288 bits CFP: 720 bits
t_{RRL}	End of valid data to RXEN Low	6.9 µs	6.9 µs	N/A
t_{RTD}	Receive data to transmit data	CFP: 6.5 – T_{MDM} CPP: 5.5 – T_{MDM}	CFP: 4.5 – T_{MDM} CPP: 3.5 – T_{MDM}	CFP: 6.5 – T_{MDM} CPP: 5.5 – T_{MDM}
t_{SHD}	SHCTR High to Receive Data	7.8 µs	7.8 µs	7.8 µs
t_{SRL}	SHCTR Low to RXEN Low	6.9 µs	6.9 µs	6.9 µs
t_{SWT}	ANTSW High to TXEN High	6.9 µs	6.9 µs	6.9 µs
t_{TD}	Transmit data length	66 bits	68 bits	CPP: 720 bits
t_{TRD}	Transmit data to receive data	CFP: 5.5 + T_{MDM} CPP: 6.5 + T_{MDM}	CFP: 3.5 + T_{MDM} CPP: 4.5 + T_{MDM}	CFP: 5.5 + T_{MDM} CPP: 6.5 + T_{MDM}
t_{TRH}	End of transmit data to RXEN High	11.3–87.6 µs 49.5 µs (default)	11.3–87.6 µs 49.5 µs (default)	11.3–87.6 µs 49.5 µs (default)
t_{TTD}	TXEN High to valid transmit data	0.868–32.1 µs 4.3 µs (default)	0.868–32.1 µs 4.3 µs (default)	0.868–32.1 µs 4.3 µs (default)
t_{FBT}	Time of fall before transmit	16.5–68.6 µs 68.6 µs (default)	2.6–54.7 µs 54.7 µs (default)	N/A
t_{TTL}	End of data to TXEN Low	4.3–36.0 µs 42.5 µs (default)	4.3–36.0 µs 42.5 µs (default)	4.3–36.0 µs 42.5 µs (default)

6.11 B CHANNEL ADPCM PORT SWITCHING CHARACTERISTICS

Figure 6-7 B Channel ADPCM Port Timing

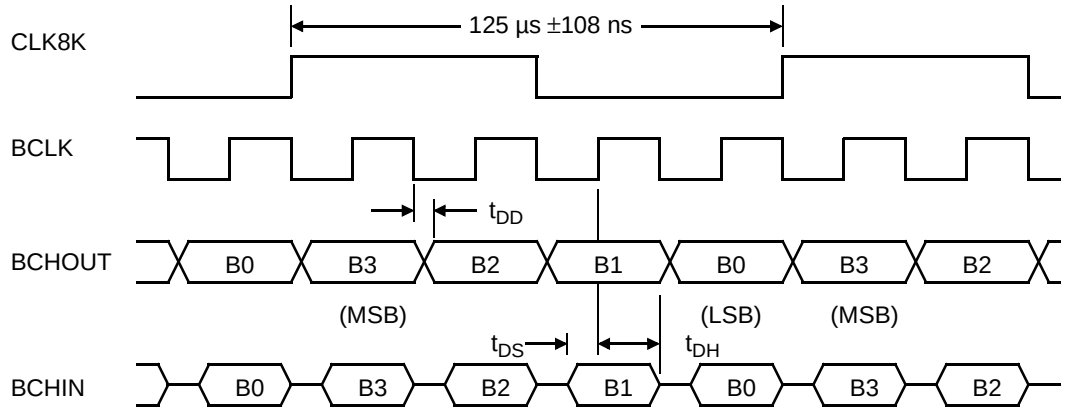


Table 6-12 B Channel ADPCM Port Timing

Parameter	Description	Min	Max
t_{DD}	BCLK low to output data valid	0 ns	100 ns
t_{DH}	Input data hold after BCLK High	0 ns	—
t_{DS}	Input data setup to BCLK High	150 ns	—

6.12 SERIAL PORT AND A-LAW PCM PORT SWITCHING CHARACTERISTICS

Table 6-13 Serial Port and A-Law PCM Switching Characteristics

Parameter	Description	Min	Max
t_D	SCLK low to output data valid	0 ns	100 ns
t_H	Input data hold after SCLK edge	0 ns	—
t_{SU}	Input data setup to SCLK edge	150 ns	—

Figure 6-8 Serial Port Timing (SIOMODE[2] = 0)

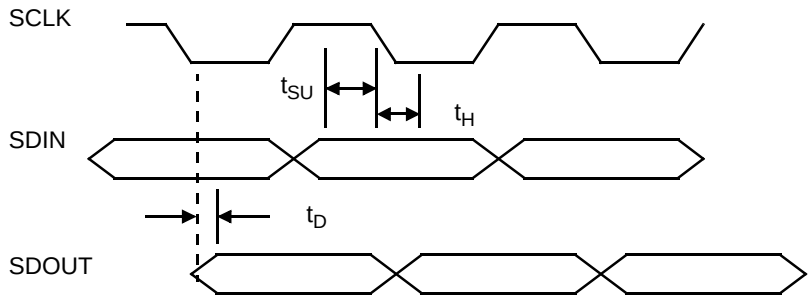
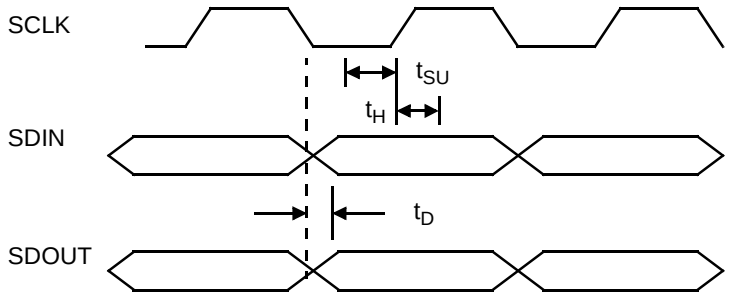


Figure 6-9 Serial Port Timing (SIOMODE[2] = 1)



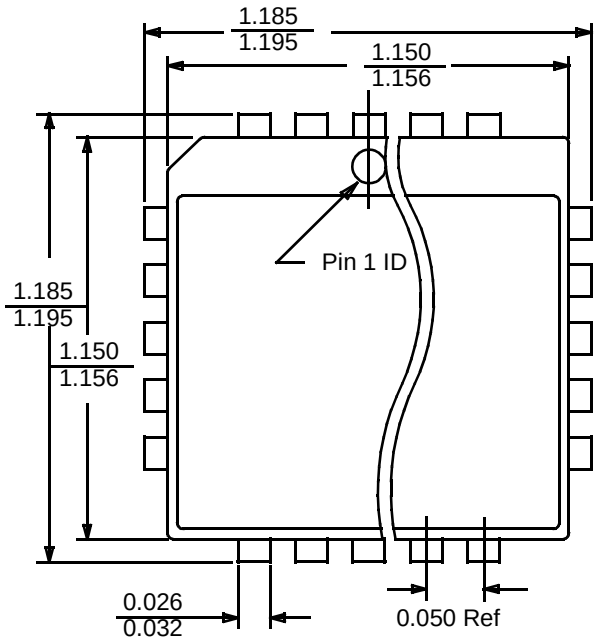
6.13 BATTERY-LEVEL DETECTOR

Battery-level detector absolute error . . . . . ±5% max

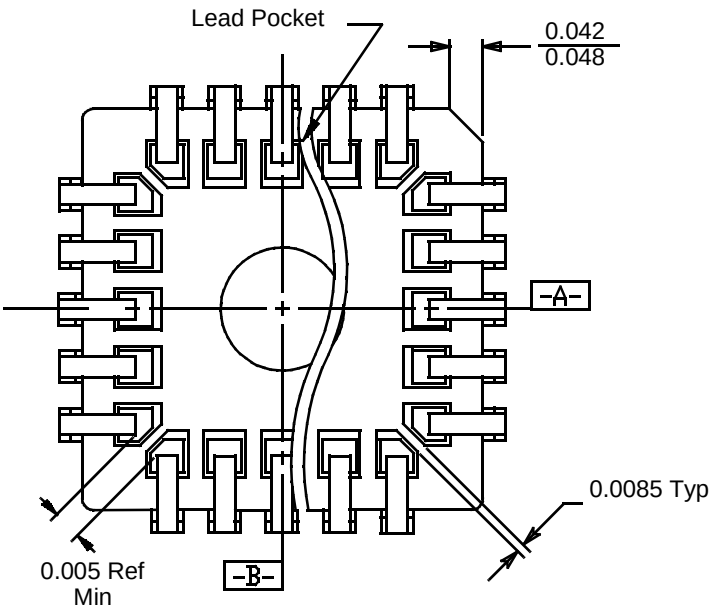
7 PACKAGE DIMENSIONS

7.1 PL 84/ PLH 84

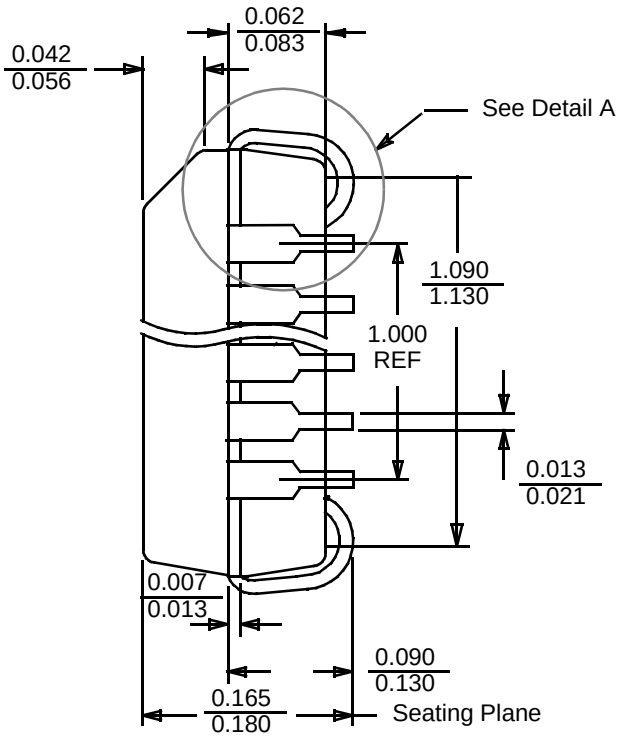
All measurements in inches.



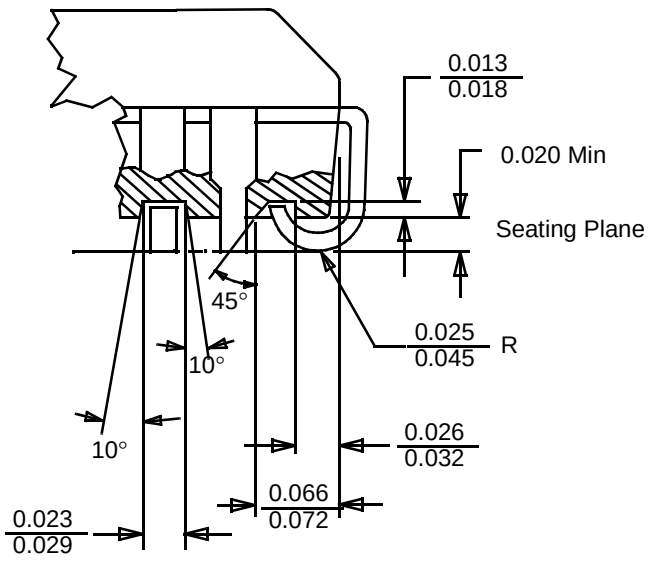
Top View



Bottom View



Side View



Detail A